Contribution to digital PFC controllers in HID lamps electronic ballast applications

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Abstract— Utility voltage fluctuations not compensated by the low frequency voltage loop of the power factor correction (PFC) stage cause a perceptible variation in the light emitted by lamps, unpleasant for the human eye and known as flicker effect. A novel extension of the digital control for PFC stages analyzes the input voltage, detects the fluctuations in the range of human flicker sensitivity and modifies the PFC output voltage controller to avoid their propagation to the dc bus. The purpose of the controller is to make the PFC compatible with any second stage lamp driver, assuring the mitigation of the lamp light variation caused by utility disturbances in consistency with the human eye perception. The controller is implemented in a Field Programmable Gate Array (FPGA). A constant lamp luminance is achieved with this digital controller with no dependence of the next ballast stage.

1 Introduction

Nowadays, the power conversion systems leverage the digital control capabilities to introduce more flexible power conversion strategies and increase the reliability. A detailed analysis of the benefits of using digital control-based controllers in power electronics and drive applications is found in [1]-[8]. Designers have the choice between two main families of digital device technologies for fast prototyping. The first family [1]-[4] is associated to microcontrollers and Digital Signal Processor (DSP) controllers. These components integrate a performing microprocessor core along with several peripherals. The

alternative family is the Field Programmable Gate Arrays (FPGAs) technology [9], [10]. These devices consist of predesigned elementary cells and interconnections that are fully programmable by the end user.

In DC/DC conversion, it is common that digital controllers pay close attention on the voltage regulation with improved dynamic performance under input voltage and load transients [11], [12].

Key properties of High Intensity Discharge (HID) lamps include higher energy efficiency, compact size, good colour rendering, whiter light (higher colour temperature), and longer lifetime [13]-[19]. Typical applications range from car headlamps, greenhouse lighting, interior lighting, industrial sector and urban lighting applications. Since the urban lighting consumption represents a non-negligible part of the total energy amount consumed on Earth, improvements of the supply, efficiency and light quality are investigated. Digital control is a key technology to provide higher performance [14]-[16] to the ballast system. In Fig. 1.a, a typical two – stage electronic ballast solution is shown including a power factor correction (PFC) [20] and an inverter. On the other hand, the same system is depicted in Fig. 1.b with a digital controller.

Light emitted by HID lamps is very sensitive to voltage supply fluctuations, producing an effect on the human visual perception, known as flicker [21]-[26]. Flicker is a very uncomfortable effect, which would cause a lot of human physiological effects as it is indicated in [24] and [25]; so it is addressed as a safety and health issue at work. These fluctuations can be caused by the connection and disconnection of important loads (high-power motors, PFC bank capacitors, etc…), compressors, resistive welding machines or arc furnaces. Flicker frequency can be perceived by the eye-brain set, when it is within a range of frequency that extends from 0.5 to 25 Hz [23]; and the maximum flicker perception occurs at around 10 Hz [26].

In two-stage electronic ballast, where the inverter may operate in open loop, the PFC outer loop and its output bulk capacitor, *C*, are the elements that attenuate the propagation of the utility voltage fluctuation to the dc bus and then contribute to reduce the light variation in HID lamps. This work presents an extension of the PFC control technique presented in [11] and [12] specifically adapted to prevent the lamp flickering. This extension can also be applied to digital PFC controllers that use input current sensor to improve the performance in lamp driver applications. The present work has precedents in the conference papers [23], [27], [28]. The update over those works includes a more detailed presentation of the signals acquisition circuit, identification of the conventional voltage regulator, the additional regulator to prevent

the lamp flickering and the hardware connection to achieve a consistent operation. A novel algorithm to detect the fluctuations over the nominal incoming voltage level and select the condition to activate the additional controller to prevent the lamp flickering is presented in this work. Also, experimental results have been updated including frequency response oscillograms. The amplitude of the low frequency PFC output ripple voltage caused by the fluctuation of the utility voltage is attenuated by increasing the PFC output capacitance. This technique can also be applied to attenuate the propagation of the utility disturbances that cause flickering, but a larger capacitor increases the volume and size of the converter and as long as the electrolytic capacitor cannot be replaced by other technology, the circuit lifetime is penalized [29]-[32]. An alternative is the implementation of a wide bandwidth controller in the inverter stage [19]. In [33], two control algorithms are presented for Distribution STATic synchronous COMpensator (DSTATCOM) to mitigate voltage fluctuation caused by electric arc furnace loads. Representative works on utility voltage detections are [34] and [28], where a technique to monitor voltage fluctuations in the power system with a least-squares-Kalman optimization technique for fundamental frequency voltage phasor estimation and an input instantaneous voltage detection algorithm, under ideal utility mains, are presented respectively.

The proposed digital compensation of the voltage fluctuation does not modify the original PFC output voltage controller if low frequency fluctuations of the input voltage are not detected. When these fluctuations appear, the proposed controller changes the voltage loop dynamic response to minimize the dc voltage ripple at the fluctuation frequency assuring a constant light luminance in the lamp and avoiding the optical flicker perception. No extra cost and no extra analog components are introduced whenever the FPGA can host the small additional digital block. To clearly show the performance achieved, a practical application with a 150 W HPS (High Pressure Sodium) lamp supplied by an open loop resonant inverter as second stage (Fig. 1) is presented.

The objectives of this paper are: 1) to develop a universal voltage fluctuation detection method that fits the standard definition human perception range. 2) To use the lowest PFC output capacitance, *C*, by extending the capabilities of the digital output voltage loop, and 3) to minimize the flicker perception for the human eye caused by the utility disturbances.

For further hardware simplification of the lamp driver oriented PFC controller, the implementation has been carried out as an extension of the digital control technique presented in [11] and [12], which requires neither current sensor nor high speed analog-to-digital converter.

The paper is organized in five sections. After introduction, the proposed digital PFC controller is presented in Section 2; with a first subsection about the input current control and a second subsection with the digital outer voltage loop. In Section 3, the voltage fluctuations detection algorithm is shown. In Section 4, experimental results with a HID lamp are presented, finalizing with conclusions.

2 The digital PFC controller

A. *Inner current loop*

Some advantages that motivate the use of digital control in PFC stages include: reduction of discrete components, ease of controller implementation and extension of its performance limits, reduction of size and reduction of sensitivity to parameter tolerances, [35], [36], [37].

The principle of operation of the digital current control to achieve power factor correction used in this work, and depicted in Fig. 2, has been presented in [11], [12], [35], [36] where an input current (i_{in}) estimator removes the need for current A/D conversion and input and output voltages are measured using the analog-to-digital converters (ADCs) represented in green in Fig. 2. Avoiding the current measurement means a step-forward with respect to analog controllers, which also helps to increase efficiency and reduce the total cost and complexity. Input and output voltages measurements (v_{inADC} and v_{oADC}) are used to estimate the input current digitally (i_{inreb}). As ADCs, first order *ad-hoc* sigma-delta converter with a low quantity of analog components (an RC filter and a comparator) [11] is used in the output voltage measurement. A commercial ADC is used for the input voltage A/D conversion. The analog circuitry used to substitute the current sensing circuit is presented in blue.

Drain-to-source MOSFET voltage is adapted as digital input signal (v_{ds}) in order to measure and compensate drive signal's delays. With this digital controller, a sinusoidal current waveshape is obtained, independently of the voltage or power conditions.

B. *Outer voltage loop*

In steady-state operation, the PFC output voltage loop has a low bandwidth (up to 10 Hz) so not to interfere with the inner loop that keeps the current shape proportional to the input voltage to comply with the IEC 61000-3-2 for class C equipment [20].

The action of the low bandwidth cannot reject the low-frequency fluctuations and they are propagated through the PFC and inverter stages, perturbing the lamp current and voltage, as is depicted in Fig. 3.a. The current fluctuation causes the lamp light variation, and then the flicker effect.

In order to attenuate this flicker effect, the capacitance of the output bulk capacitor (*C* shown in Fig. 2) in the PFC stage could be chosen higher than the calculated with (1), which determines the capacitance needed to limit the amplitude of the voltage ripple at twice the line frequency, ΔV_o, below a given value $\Delta V_o = V_o - V_{o,\min}$, supplying a power rate *P*, where V_o and $V_{o,min}$ are the average and minimum output voltage in steady state respectively, and T_u is the utility period.

$$C > \frac{PT_u}{V_o^2 - V_{o,\min}^2} \tag{1}$$

This solution needs electrolytic capacitors which limit the useful life of the ballast system.

Figure 3.b shows the target behaviour of the proposed control. During steady state, the output voltage loop has a low bandwidth and a current shape proportional to the input voltage and also has an extended bandwidth loop in the utility voltage fluctuations situation with current distortion. Standard IEC 61000-3-2 class C [20] is not applied in presence of these utility transients. A constant PFC stage output voltage (v_o) is achieved despite input voltage low frequency fluctuations. With this, constant lamp current (i_{lamp}), and then constant lamp light luminance are also achieved.

In previous work [27], the design of a small-signal model of the NLC (Nonlinear-Carrier) controlled boost rectifier and the analysis to obtain the control-to-output transfer function *G(s)* was presented following [39]. The output voltage control loop has been designed using the *G(s)*, whose expression is

$$G(s) = \frac{V_o(s)}{V_m(s)} = \left(\frac{V_{in,RMS}}{V_o}\right)^2 \frac{R}{3r_s} \frac{1}{1 + s\frac{RC}{3}}, \tag{2}$$

where r_s is the virtual current sensor resistor, R is the load and C the output capacitor as is shown in Fig. 4, while v_m is the NLC control voltage. Details of the sequence to obtain (2) are given in the Appendix.

A digital voltage loop is shown in Fig. 4.a, where a low bandwidth compensator, $C_{ss}(z)$ is implemented to assure that the output voltage that supplies the second stage follows the reference (v_{oref}). The block diagram of the proposed digital controller is presented in Fig. 4.b, where the block "*Current loop*" represents the NLC controller presented in Fig. 2. When utility disturbances appear, an utility voltage fluctuations detector, presented in Section III, activates the compensator $C_{fluc}(z)$ in order to extend the bandwidth of the PFC outer loop, avoiding their propagation to the lamp at the expense of increasing the utility current distortion. With this capability, a low C value can be utilized. The design of the controllers was presented in previous works [27-28], using the following sequence. 1) A proportional integral (PI) action is selected for both controllers as the right option to obtain high loop gain at very low frequency and around 90º phase lag at the cross-over frequency. At least 52º phase margin, *pm*, is desired to prevent transient oscillations. 2) $C_{ss}(z)$ is designed to set the loop gain crossover frequency, f_c, around 1Hz, thus avoiding line current distortion in steady-state [3]. 3) $C_{fluc}(z)$ is designed to set, f_c, around 100Hz, a decade above 10 Hz, which determines the upper flicker detection limit of the human eye. 4) To simplify the digital implementation in the FPGA, the coefficients of both controllers are approximated to powers of 2, verifying the resulting f_c and *pm* with Matlab- Sisotool ®. Table I shows the plant and the designed controllers in the z-domain.

3 Input voltage fluctuations detection algorithm

The utility peak voltage value ($v_{in,peak}$) is obtained, cycle by cycle, with a digital peak detector of the digital input voltage (v_{inADC}). With this value, the steady-state utility peak voltage and three different voltage levels are defined as is shown in Fig. 5.a. The algorithm defines the non-fluctuation band (called *"In"* in Fig. 5.a), with the steady-state utility peak voltage, $v_{in,peak}$ ±2%.

When the utility peak voltage is found outside this band, i.e. *"Above"* or "*Below"* in Fig. 5.a, the algorithm determines whether there is a fluctuation in the most sensitive frequency range of the human eye, between 0.5 to 25 Hz. It is assumed that fluctuation component of the utility voltage is approximately a symmetric function, i.e. it can be reflected around a specific time location. Consequently, if the fluctuation period is T_f, every $T_f/2$ the utility voltage envelope crosses the limits of the voltage band.

When the first change in the peak value is detected, the algorithm measures the time (T_i) throughout the peak voltages are maintained in each band. If T_i lasts between 0.02 s and 1 s (half period of a 25 and 0.5 Hz fluctuation, respectively), it is considered that there is a utility voltage fluctuation. Therefore, precise fluctuation frequency is only measured if it is in the 0.5 to 25 Hz range, where it produces an unpleasant optical flicker perception.

The input voltage fluctuation detection algorithm flowchart is shown in Fig. 5.b. The signal "*Fluctuation"* is set to "1" under flicker situation, and therefore the time during the wide bandwidth voltage loop has to be applied ($T_{wide\text{-}loop}$) is determined.

4 Experimental results

Laboratory experiments that illustrate the performance of the digital controller have been carried out with electronic ballast for a 150 W HPS lamp (LUCALOX). A boost converter has been used as PFC stage. Values of the components are: L = 3.2 mH, V_{in} = 230 V (50 Hz), f_{sw} = 73 kHz, V_o = 420 V and P_o= 150 W. The output bulk capacitance is 68 μF.

A *LCC* half-bridge resonant inverter (RI) is used as second stage. It provides the required ballast action at reduced cost and behaves as an input voltage-dependent power source. Since the compensation of the utility fluctuation is carried out by the PFC stage, it can be connected to other type of second stages and light sources [14], [15], [28] and [38].

The *LCC* resonant circuit is designed to have zero resonant current phase lag at the end of the lamp lifetime, and it works in a frequency window free of acoustic resonance, which is a valid solution for 150 W HPS lamps [14]. This inverter operates in open loop, so it is a system without capability for compensation of input voltage disturbances, being a good example to illustrate the performance of the proposed digital controller. ZVS is guaranteed in the resonant inverter along with a minimum reactive component in the resonant tank considering the whole life span of the lamp. Using the design sequence described in [14], the RI design is defined by $Z_p = R_{lamp}/Q_p$ = 170 Ω, L_r = 115 μH, C_p = 5.7 nF and C_s = 330 nF.

For laboratory test purposes, the digital control circuit is implemented in a Xilinx Spartan 3 family XC3s200e FPGA. In order to measure the behaviour of the system with the proposed digital control, an APDS-9007 ambient light photo sensor is used. This photo sensor has a spectral response close to the

standard photopic observer. The photo sensor is placed in front of the lamp to get an output voltage proportional to the brightness of the lamp light, according to what human eye perceives). An Agilent 6813B AC programmable power source is used to supply the HID lamp power supply.

Figure 6.a shows the PFC stage input current (i_{in}) and the input voltage (v_{in}) waveforms in steady-state situation. Despite not measuring the input current, power factor correction is successfully achieved. The measured power factor was 0.991 with 168 W input power (P_{in}).

In Fig. 6.c, the Fast Fourier Transform (FFT) on the input current in comparison with the IEC 61000-3-2 class-C limits shows that all current harmonics are below the limits recommended by the standard.

Figure 6.b shows the PFC stage input current (i_{in}) and the input voltage (v_{in}) waveforms during utility fluctuation with the wide bandwidth outer loop. In this case, the power factor is 0.91. The input current is distorted because of the faster dynamic response. Figure 6.d, shows that the harmonic content of the input current does not comply with the IEC 61000-3-2 class C limits, but in the utility fluctuation case the mentioned standard does not apply [20].

The phase margin and the crossover frequency are 73º and 0.61 Hz for the reduced bandwidth voltage loop (Figs. 6.a and 6.c), and 78.8º and 149 Hz for the wide bandwidth loop (Figs. 6.b and 6.d). Output voltage reference is the same for both controllers; in this case 420 V_{dc}. Fig. 7 shows the Bode diagrams of the extended bandwidth (blue) and the reduced bandwidth (green) outer loops.

The PFC stage dc output voltage (v_o), the lamp light lux level measured by the photo sensor (lx_{LAMP}) and the input voltage (v_{in}) to the PFC stage under a 10% fluctuation (ΔV) in the input voltage (programmed in the AC power source) are shown in Fig. 8.a when the PFC uses the slow PFC outer loop, and in Fig. 8.b when the PFC uses the fast PFC outer loop to compensate the fluctuation.

Fluctuation frequency has been set close to the maximum level of human eye flicker perception, i.e. 10 Hz. Figure 8 shows the same input voltage and the differences on lx_{LAMP} and v_o waveforms between applying or not the extended bandwidth outer loop. In Fig. 8.a, the lx_{LAMP} signal has a fluctuation of 10 Hz (added to the output voltage 100 Hz fluctuation, imperceptible by the human eye). On the other hand, in Fig. 8.b this fluctuation is highly attenuated, because the wide bandwidth voltage loop is applied. In this case, lamp light variation and flicker perception disappear.

Figure 9 shows the behaviour of the input voltage fluctuation detection algorithm. Figure 9.a displays the signal "*Fluctuation*" under different utility voltage conditions. At first, a 230 V_{rms} (325 V peak) utility voltage is applied. After 27 seconds, a step down of 30 V_{rms} is applied; and then, after 30 seconds, 210 V_{rms} (297 V peak) input voltage is applied. In this situation, a 10 % and 10 Hz fluctuation is imposed (210 – 189 V_{rms}).

The algorithm determines the steady-state peak voltage and defines the ±2% *"In"* band. When the fluctuation is detected, the signal "*Fluctuacion*" turns to "1". The extended bandwidth voltage loop is applied during the time $T_{wide\text{-}loop}$. Figure 9.b demonstrates the result of the algorithm behaviour at the end of the fluctuation. It can be seen that a 1 second period is necessary to determine that the fluctuation has finished.

5 Conclusions

A digital controller for power factor correction circuits applied to HID lamp electronic ballast has been proposed. This controller, implemented in a FPGA, makes the utility current to meet the IEC 61000-3-2 class C limits in steady-state and rejects input voltage fluctuations to avoid lamp flicker [20].

The proposed controller extension, specific for ballast application, is applied to a PFC controller which requires no current sensor to shape the input current. The input current of the ballast system is estimated from the input and output voltages of the PFC stage. Avoiding the current measurement is a significant advantage with respect to other controllers because it eliminates a hot spot in the circuit and improves the noise immunity of the control circuit.

A voltage fluctuations detection algorithm is used to avoid the propagation of the fluctuations to the lamp. The algorithm measures the steady-state utility peak voltage and detects low frequency voltage fluctuations in the most sensitive frequency range of the human eye. Depending on the detected disturbances, the digital controller modifies the voltage-loop speed of the PFC-stage, reducing the light flicker emission within the frequency band of human perception of the flickering. The proposed digital controller is a valid solution even though the higher bandwidth (149 Hz) voltage loop distorts the input current. This is compatible with the IEC 61000-3-2 standard because the essay to define the standard compliance is defined in steady-state and the utility voltage level fluctuation implies a transient state.

A two stage ballast system (Boost PFC + Resonant Inverter) that supplies a 150 W HPS lamp has been subjected to low frequency utility fluctuations. These fluctuations have been programmed with an AC power electronic source in order to produce a variation on the light emitted close to the maximum level of human eye flicker perception, emulating an industrial environment under grid disturbances.

A constant light luminance in the lamp is achieved despite frequency utility mains fluctuations and without extra components external the digital circuit. Moreover, the size of the PFC output capacitor is reduced, decreasing the volume and cost, and increasing the lifetime of the converter.

Appendix

The implemented non-linear controller (inner current control) defines d by comparing $(i_L(t_0)+i_L(t))/2$ multiplied by a real or artificial sensor resistance r_s with the carrier signal $v_m(1-(t-t_0)/T)$ in each switching period. The variable v_m is the control variable that will be provided by the outer voltage loop. The function $i_L(t)$ represents the current through the inductor in the time domain and $i_L(t_0)$ is the current through the inductor at the beginning of a given switching period. Therefore, the condition

$$\frac{i_L(t_0)+i_L(t)}{2} r_s = v_m\left(1-\frac{t-t_0}{T}\right) \tag{a.1}$$

results in

$$\frac{i_L(t_0)+i_L(t_0+dT)}{2} r_s = v_m\left(1-\frac{dT}{T}\right) \tag{a.2}$$

Assuming that the computed value is the current trough the inductor averaged over the switching period, T, $\langle i_L \rangle_T$, the previous expression can also be rewritten for each switching period as

$$\langle i_L \rangle_T r_s = v_m(1-d) \tag{a.3}$$

Assuming also high switching frequency in comparison with the dynamics of the averaged variables this equation can be defined in the time-domain

$$\langle i_L \rangle_T r_s = v_m(t)\frac{\langle v_{in} \rangle_T}{\langle v_o \rangle_T} \tag{a.4}$$

The quasi-static approximation, which assumes ac line variations much slower than the converter dynamics, reveals that the non-linear controller shapes the current to be proportional to the input voltage when the ripple of the output voltage is low, as desired for the power factor correction application, justifying the proposed non-linear controller.

Perturbing the control variable v_m around a given operation point defined by the DC output voltage, V_o inductor current, I_L, and control signal, V_m values with $V_o = \frac{V_{in}}{1-D}$, $I_L = \frac{V_o}{R(1-D)}$ and $I_L r_s = V_m(1-D)$, the following transfer function is obtained

$$I_L(s) = V_m(s)\frac{V_{in}}{r_s V_o} - V_o(s)\frac{V_m V_{in}}{r_s V_o^2} \tag{a.5}$$

From $<i_L>_T$ in (a.4), the averaged current through the *RC* load, i.e. the load resistor *R* and the output filter capacitor *C* shown in Fig. 4.b, in the switching period, $<i_{RC}>_T$, is obtained as,

$$\langle i_{RC}\rangle_T = \langle i_L\rangle_T(1-d) = \langle i_L\rangle_T \frac{\langle v_{in}\rangle_T}{\langle v_o\rangle_T} \tag{a.6}$$

Assuming sinusoidal input voltage and using the notation $\langle i_L\rangle_{T,\max}$, $\langle v_{in}\rangle_{T,\max}$, for the averaged input current and voltage at the ac utility angle π/2, the output voltage results from averaging the converter operation over half line period (T_u/2), and the transfer function that defines the plant is the response of the output voltage of the averaged over the utility period model, $\langle v_o\rangle_{Tu}$, to perturbations of v_m.

The quasi-static approximation with low output voltage ripple assumes $\langle v_o\rangle_T = \langle v_o\rangle_{Tu}$. Therefore, the current through the load averaged over the utility period is calculated as

$$\langle i_{RC}\rangle_{Tu} = \frac{1}{\pi}\int_{\omega t-\frac{\pi}{2}}^{\omega t+\frac{\pi}{2}} \frac{\langle i_L\rangle_{T,\max}\langle v_{in}\rangle_{T,\max}}{\langle v_o\rangle_T}\sin^2(\omega t)d(\omega t) = \frac{\langle i_L\rangle_{T,\max}\langle v_{in}\rangle_{T,\max}}{2\langle v_o\rangle_{Tu}} = \frac{\langle p\rangle_{Tu}}{\langle v_o\rangle_{Tu}} \tag{a.7}$$

From this result defined in the time-domain, a small-signal expression, in this case defined in the Laplace domain can be obtained, where the upper case notation without the Laplace complex argument *(s)* is used

for the DC values. Therefore, $I_{RC}(s)$, $I_{L,max}(s)$, $V_{in,max}(s)$ and $V_o(s)$ correspond to the small-signal perturbation of $<i_{RC}>_{Tu}$, $<v_{in}>_{T,max}$ and $<v_o>_{Tu}$ respectively $V_{in,max}$, $I_{L,max}$, V_o and R define the DC operation point

$$I_{RC}(s) = I_{L,\max}(s)\frac{V_{in,\max}}{2V_o} + V_{in,\max}(s)\frac{I_{L,\max}}{2V_o} - V_o(s)\frac{1}{R} \tag{a.8}$$

The plant to be controlled by the outer loop is obtained by introducing (a.5) into (a.8), and using V_m(s) as the only input, i.e. $V_{in,max}$(s) = 0.

$$I_{RC}(s) = V_m(s)\frac{V_{in,\max}^2}{2r_s V_o^2} - V_o(s)\frac{2}{R} \tag{a.9}$$

$$V_o(s) = I_{RC}(s)\frac{R}{1+sRC} \tag{a.10}$$

The use of a resistance as the small-signal load is justified because here it is considered the case of the next section, i.e. the inverter, operating in open loop and the range of the small-signal perturbation frequency is low. A closed loop controlled inverter would modify its small-signal behaviour as a load.

$$G(s) = \frac{V_o(s)}{V_m(s)} = \left(\frac{V_{in,RMS}}{V_o}\right)^2 \frac{R}{3r_s}\frac{1}{1+s\frac{RC}{3}} \tag{a.11}$$

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References

[1] E. Monmasson, L. Idkhajine, M.N. Cirstea, I. Bahri, A. Tisan and M.W. Naouar, "FPGAs in Industrial Control Applications," IEEE Trans. Ind. Informat., vol. 7, no. 2, May 2011, pp. 224-243.

[2] E. Monmasson and M. Cirstea, “Guest editorial special section on field programmable gate arrays (FPGAs) used in industrial control systems,” IEEE Trans. Ind. Electron., vol. 54, no. 4, Aug. 2007, pp. 1807–1809.

[3] D. Maksimovic, R. Zane and R. Erickson, "Impact of digital control in power electronics," Proc. IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD 2004), 24-27 May 2004, pp. 13- 22.

[4] M. P. Kazmierkowski, M. Jasinski, and G. Wrona, "DSP-Based Control of Grid-Connected Power Converters Operating Under Grid Distortions," IEEE Trans. Ind. Informat., vol. 7, no. 2, May 2011, pp. 204 -211.

[5] L. Idkhajine, A. Prata, E. Monmasson, K. Bouallaga and M. W. Naouar, "System on Chip controller for electrical actuator," Proc. IEEE International Symposium on Industrial Electronics (ISIE 2008), June 30 2008-July 2 2008, pp. 2481-2486.

[6] J. M. Guerrero, F. Blaabjerg, T. Zhelev, K. Hemmes, E. Monmasson, S. Jemei, M.P. Comech, R. Granadino and J.I. Frau, "Distributed Generation: Toward a New Energy Paradigm," IEEE Ind. Electron. Mag., vol. 4, no. 1, March 2010, pp. 52-64.

[7] A. Malinowski and Hao Yu, "Comparison of Embedded System Design for Industrial Applications," IEEE Trans. Ind. Informat., vol. 7, no. 2, May 2011, pp. 244-254.

[8] Man Ho Kim, Suk Lee and Kyung Chang Lee, "Kalman Predictive Redundancy System for Fault Tolerance of Safety-Critical Systems," IEEE Trans. Ind. Informat., vol. 6, no. 1, Feb. 2010, pp. 46-53.

[9] E. Monmasson, L. Idkhajine and M.W. Naouar , "FPGA-based Controllers," IEEE Ind. Electron. Mag., vol. 5, no. 1, March 2011, pp. 14-26.

[10] J. J. Rodriguez-Andina, M. J. Moure and M. D. Valdes, "Features, Design Tools, and Application Domains of FPGAs," IEEE Trans. Ind. Electron., vol. 54, no. 4, Aug. 2007, pp. 1810-1823.

[11] F. J. Azcondo, A. de Castro, V. M. Lopez and O. Garcia, "Power factor correction without current sensor based on digital current rebuilding", IEEE Trans. Power Electron., vol. 25, no. 6, Jun 2010, pp. 1527-1536.

[12] V. M. Lopez, F. J. Azcondo, F. J. Diaz and A. de Castro, "Autotuning digital controller for current sensorless power factor corrector stage in continuous conduction mode", Proc. IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2010), University of Colorado, Boulder, Colorado, USA, June 2010.

[13] J. de Groot and J. Van. Vliet, The High-Pressure Sodium Lamp. Philips Technical Library, Macmillan Education, 1986.

[14] F. J. Azcondo, F. J. Díaz, R. Casanueva and C. Brañas, "Microcontroller Power Mode Stabilized Power Factor Correction Stage for High Intensity Discharge Lamp Electronic Ballast," IEEE Trans. Power Electron., Part Special Section on Lighting Applications, vol. 22, no. 3, May 2007, pp. 845-853.

[15] F. J. Diaz, F. J. Azcondo, R. Casanueva, C. Branas, and R. Zane, "Digital control of a Low-Frequency Square-Wave electronic ballast with Resonant Ignition," IEEE Trans. Ind. Electron., vol. 55, no. 9, Sep. 2008, pp. 3180-3191.

[16] B. Divakar, K. Cheng, D. Wang, D. Ping, and K. Kwok, "Implementation of a Voltage Multiplier Integrated HID Ballast Circuit With Dimming Control for Automotive Application," IEEE Trans. Ind. Electron., vol. 56, no. 7, Jul. 2009, pp. 2479-2492.

[17] R. Orletti, M. Co, D. Simonetti, and J. de Freitas Vieira, "HID Lamp Electronic Ballast With Reduced Component Number," IEEE Trans. Ind. Electron., vol. 56, no. 3, Mar. 2009, pp. 718-725.

[18] R. Sanchez, N. Vazquez, C. Hernandez, E. Rodriguez, S. Pinto, and M. Juarez, "Electric Dynamic Modeling of HID Lamps for Electronic Ballast Design," IEEE Trans. Ind. Electron., vol. 57, no. 5, May 2010, pp. 1655-1662.

[19] C. Brañas, F. J. Azcondo and R. Zane, “Power-mode control of multiphase resonant electronic ballast,” IEEE Trans. Ind. Electron., vol. 59, no. 4, April 2012, pp. 1770-1778.

[20] Standards on Electromagnetic Compatibility (EMC), Part 3, Section 2: Limits for Harmonic Current Emissions, IEC 61000-3-2 Edition 2:2000, Jan. 2004.

[21] CENELEC, EN 50160. Voltage Characteristics of Electricity Supplied by Public Distribution Systems. 2001.

[22] R. Cai, J. F. G. Cobben, J. M. A. Myrzik, J. H. Blom and W. L. Kling, "Flicker responses of different lamp types," IET Generation, Transmission & Distribution, vol. 3, no. 9, Sept. 2009, pp. 816-824.

[23] F. J. Azcondo, M. Mañana, A. Ortiz, F. J. Díaz, C. Brañas, C. Renedo, S. Pérez, F. Delgado and R. Casanueva, "Voltage Fluctuations in Lamps and Ballasts," IEEE Ind. Appl. Mag., vol. 17, no. 5, Sept.-Oct. 2011, pp. 45-52.

[24] A.E. Emanuel, and L. Peretto, “A simple lamp-eye-brain model for flicker observation,” IEEE Trans. Power Del., vol. 19, no. 3, July 2004, pp. 1308-1313.

[25] L. Peretto, L. Rovati, G. Salvatori, R. Tinarelli and A. E. Emanuel, "Investigation on the Response of the Human Eye to the Light Flicker Produced by Different Lamps," Proc. IEEE Instrumentation and Measurement Technology Conference (IMTC 2006), April 2006, pp. 37-42.

[26] IEC, IEC 61000-4-15. Electromagnetic Compatibility (EMC) - Part 4: Testing and Measurement Techniques - Section 15: Flickermeter - Functional and Design Specifications. 2003.

[27] F. J. Diaz, V. M Lopez, F. J. Azcondo, “New specification for the PFC controller in HID lamps electronic ballast”, Proc. IEEE Industrial Electronics Annual Conference (IECON 2010), pp. 2595-2600, Nov. 2010.

[28] F. J. Diaz, V. M Lopez and F. J. Azcondo, “Anti-flicker Digital PFC controller for HID Lamps Electronic Ballast”, Proc. IEEE Industrial Electronics Annual Conference (IECON 2011), Nov. 2011, pp. 2901-2906.

[29] J. Ho, T.R. Jow and S. Boggs, "Historical introduction to capacitor technology," IEEE Electr. Insul. Mag., vol. 26, no. 1, January-February 2010, pp. 20-25.

[30] A. Lazaro, A. Barrado, M. Sanz, V. Salas and E. Olias; , "New Power Factor Correction AC-DC Converter With Reduced Storage Capacitor Voltage," IEEE Trans. Ind. Electron., vol. 54, no. 1, Feb. 2007, pp. 384-397.

[31] F. Tomm, A. Seidel, A Campos, M. Dalla Costa and R. Prado, “HID Lamp Electronic Ballast Based on Chopper Converters,” IEEE Trans. Ind. Electron., vol. 59, no. 4, April 2012, pp. 1799-1807.

[32] D. G. Lamar, J. Sebastian, M. Arias and A. Fernandez, “On the Limit of the Output Capacitor Reduction in Power Factor Correctors by Distorting the Line Input Current,” IEEE Trans. Power Electron., vol. 27, no. 3, March 2012, pp. 1168-1176.

[33] K. Anuradha, B. P. Muni and A. D. R. Kumar, “Modeling of Electric Arc Furnace & Control Algorithms for Voltage Flicker Mitigation Using DSTATCOM,” Proc. IEEE International Power Electronics and Motion Control Conference (IPEMC 2009), May 2009, pp. 1123-1129.

[34] I. Sadinezhad, and V. Agelidis, “Frequency Adaptive Least-Squares-Kalman Technique for Real-Time Voltage Envelope and Flicker Estimation,” IEEE Trans. Ind. Electron., vol. 59, no. 8, Aug. 2012, pp. 3330-3341.

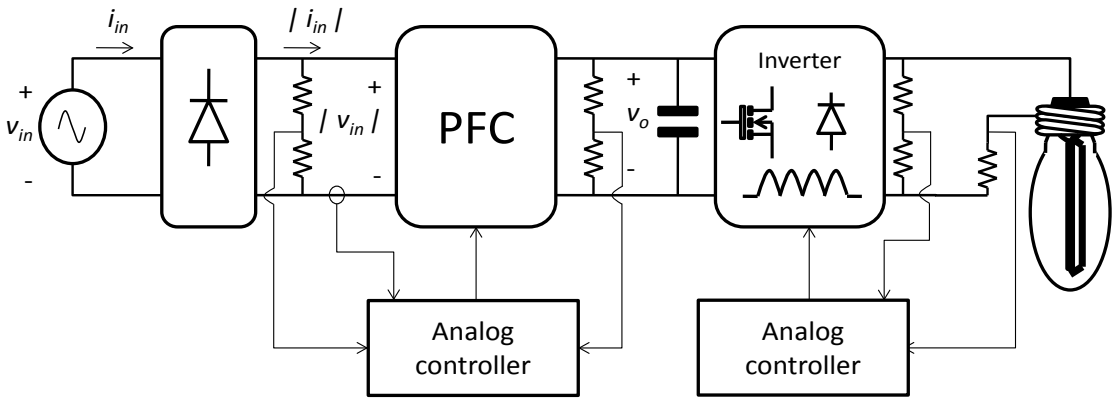
[35] V. M. Lopez-Martin, F. J. Azcondo and A. de Castro, “Current Error Compensation for Current-sensorless Power Factor Corrector Stage in Continuous Conduction Mode,” IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL), June 2012, pp. 1-8.

[36] V. M. Lopez-Martin, F. J. Azcondo and A. de Castro, “High-resolution Error Compensation in Continuous Conduction Mode Power Factor Correction Stage without Current Sensor,” 15th International Power Electronics and Motion Control Conference (EPE/PEMC), Sept. 2012, pp. 1-8.

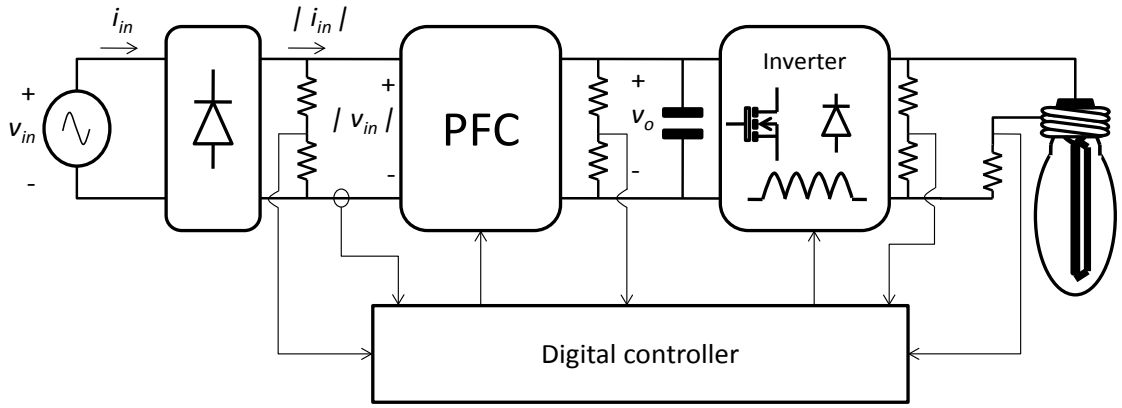
[37] J. T. Su and C. W. Lin, "Auto-tuning Scheme for Improved Current Sharing of Multiphase DC-DC Converters," IET Power Electronics, vol. 5, no. 9, Nov. 2012, pp. 1605-1613.

[38] Zhuang Zuo, Dianguo Xu, Xiangjun Zhang, Hankui Liu, “Design of a Novel Low-Frequency Square-Wave Digital Electronic Ballast for HID Lamps,” IEEE Power Electronics Specialists Conference (PESC), June 2007, pp. 3112-3116.

[39] D. Maksimovic, Y. Jang, R.W. Erickson, "Nonlinear-carrier control for high-power-factor boost rectifiers," IEEE Trans. Power Electronics., vol. 11, no. 4, Jul. 1996, pp. 578-584.



(a)



(b)

Fig. 1 *Two power stages ballast circuit with: (a) An analog PFC and inverter controllers, (b) digital controllers integrated in a single device.*

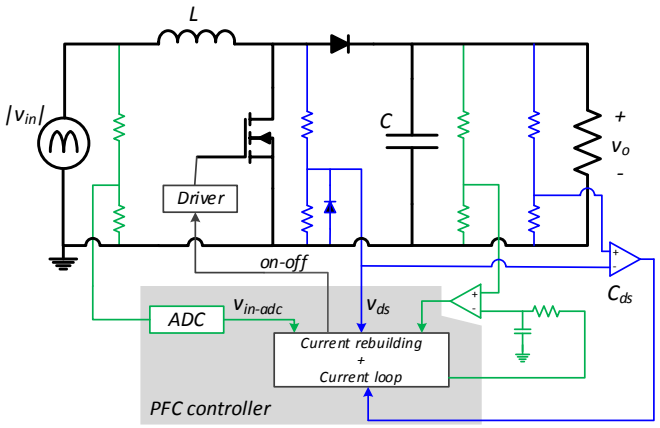
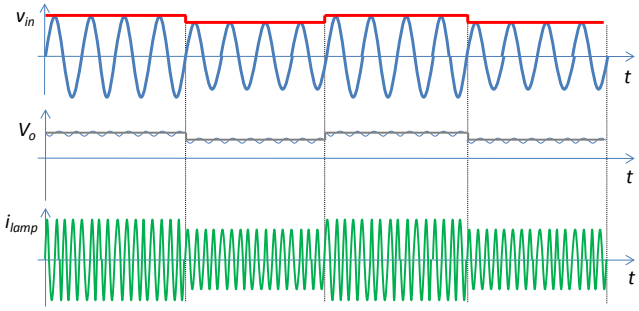
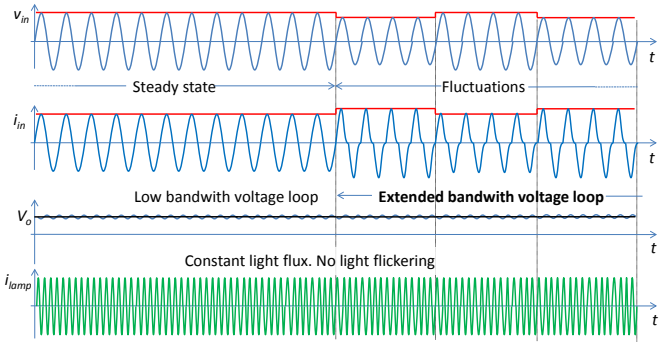


Fig. 2 *PFC circuit and digital controller block diagram.*

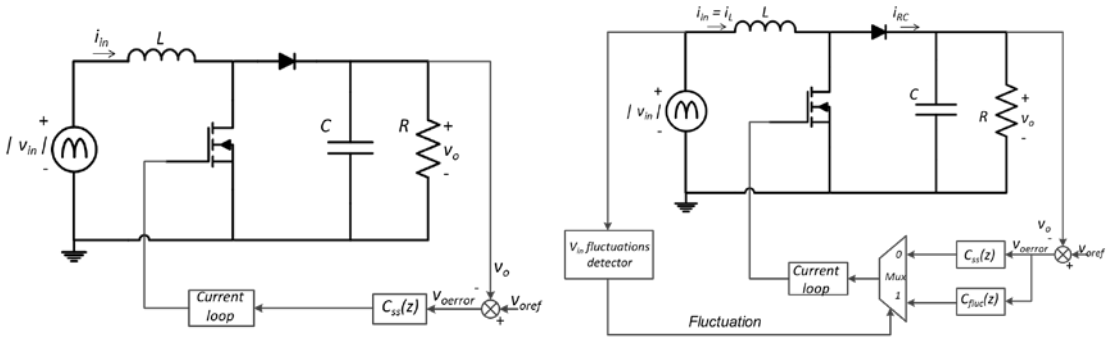


(a)



(b)

Fig. 3 *Waveforms: (a) under voltage fluctuations situation: Utility voltage, v_{in}, PFC stage output voltage, V_o, and lamp current, i_{lamp}. (b) v_{in}, V_o, i_{lamp} and utility current, i_{in}, changing the voltage loop: Low bandwidth loop during steady state and extended bandwidth loop under utility voltage fluctuation*



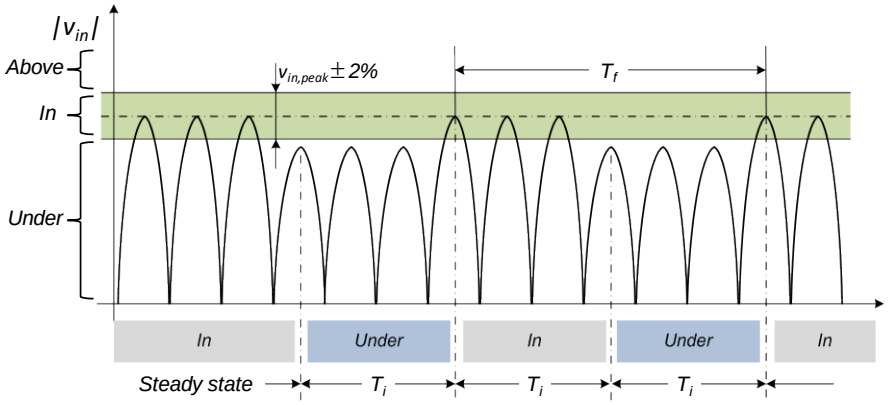
(a) (b)

Fig.4 *PFC stage and digital controller implementation: (a) Traditional digital voltage control loop, (b) proposed digital control loop.*

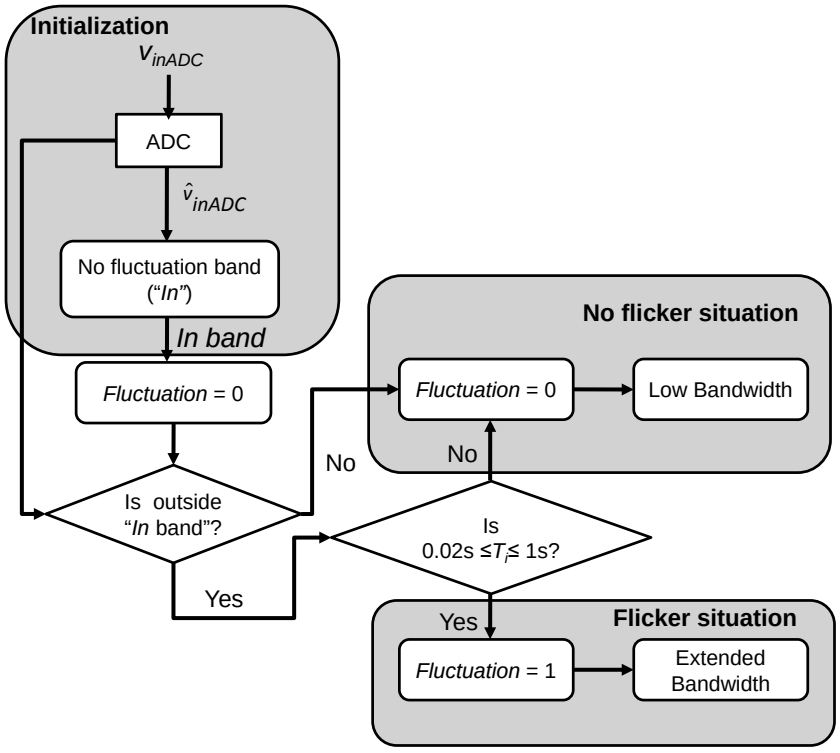
TABLE I

PFC STAGE AND CONTROLLER TRANSFER FUNCTIONS FOR THE SITUATIONS CONSIDERED IN THE UTILITY

C	$G(z)$	$C_{SS}(z)$	$C_{FLUC}(z)$
$68\ \mu F$	$\frac{1.99510^{-7}}{z-0.9998}$	$0.75\frac{z-0.9375}{z(z-1)}$	$4096\frac{1}{(z-0.9375)}$



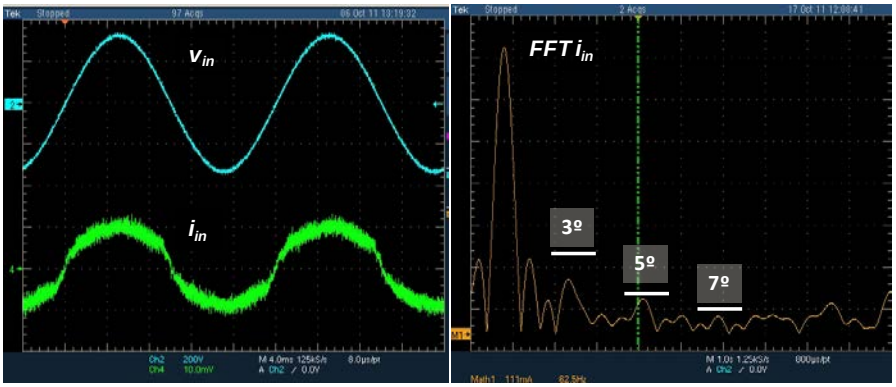
(a)



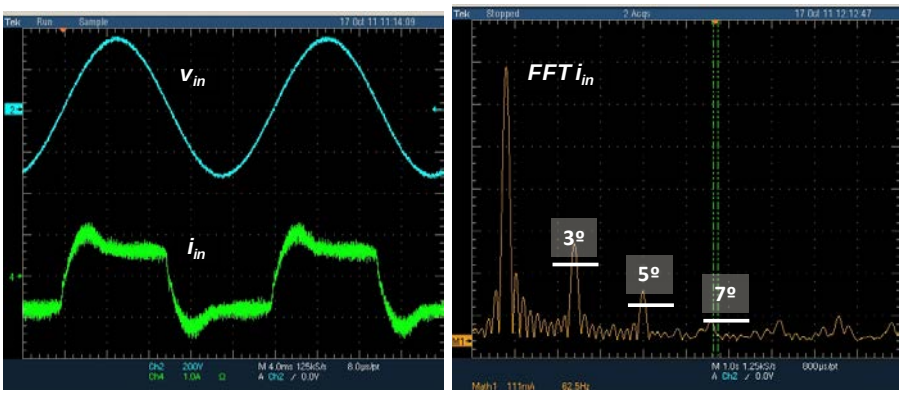
(b)

Fig. 5. *Detection of the fluctuation: (a) Voltage levels defined to detect the utility voltage fluctuations.*

(b) Input voltage fluctuation detection algorithm flowchart



(a) (c)



(b) (d)

Fig. 6 *PFC stage input waveforms and power. Low bandwidth outer loop. Input voltage v_{in}, and input current i_{in}. V_{in} = 230V_{rms}, 50 Hz. Ch2 input voltage, 200 V/div, Ch4 input current, 1 A/div: (a) Low bandwidth outer loop and (b) wide bandwidth outer loop. M1 Input current Fast Fourier Transform (FFT i_{in}) and IEC 61000-3-2 class C limits: (c) Low bandwidth outer loop with I_1 = 0.680 A and PF = 0.991. M1, vertical scale 111 mA/div, horizontal scale 62.5 Hz/div, and (d) wide bandwidth outer loop with I_1 = 0.680 A and PF = 0.91. M1, vertical scale: 111 mA/div, horizontal scale: 62.5 Hz/div.*

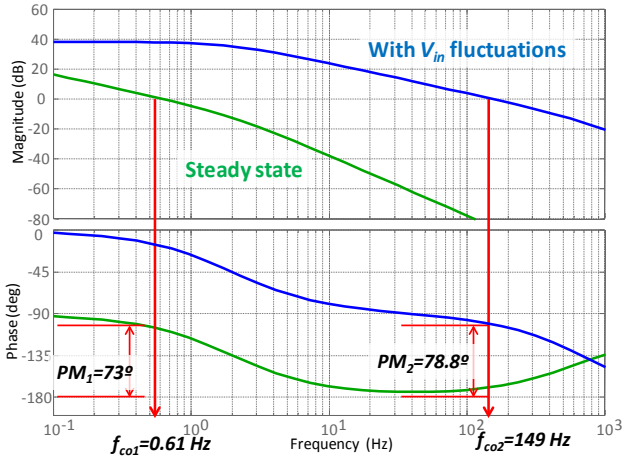
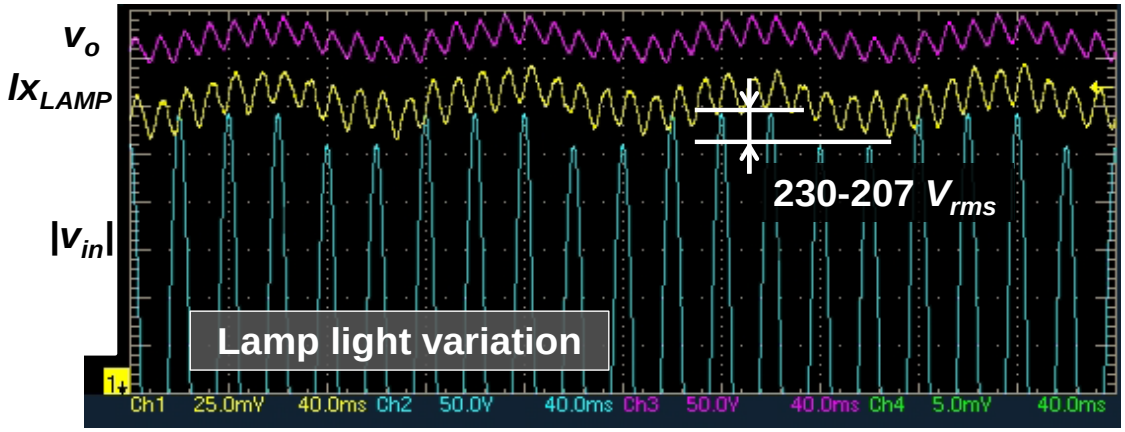
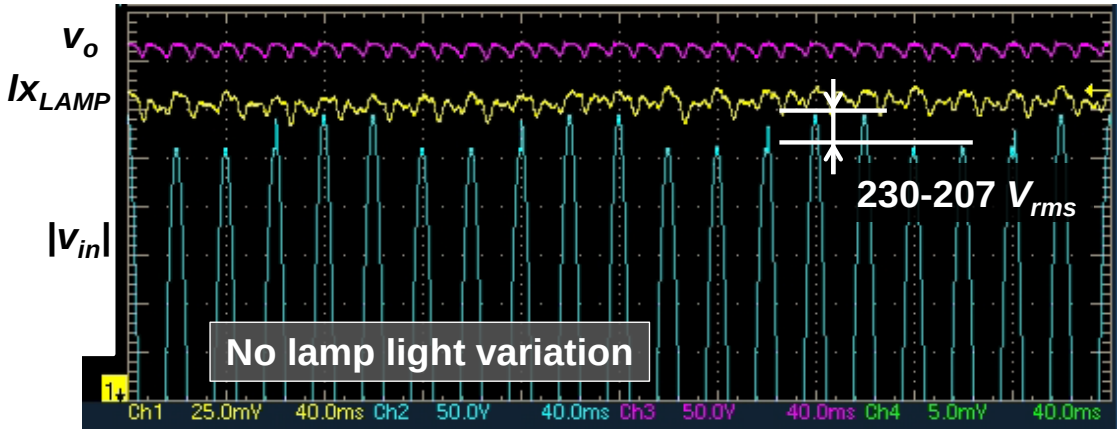


Fig. 7 *Bode plots of the different voltage loops. Green: Bode plot for steady-state condition with reduced bandwidth. Blue: Bode plot for transient state during fluctuation of the input voltage with wider bandwidth.*

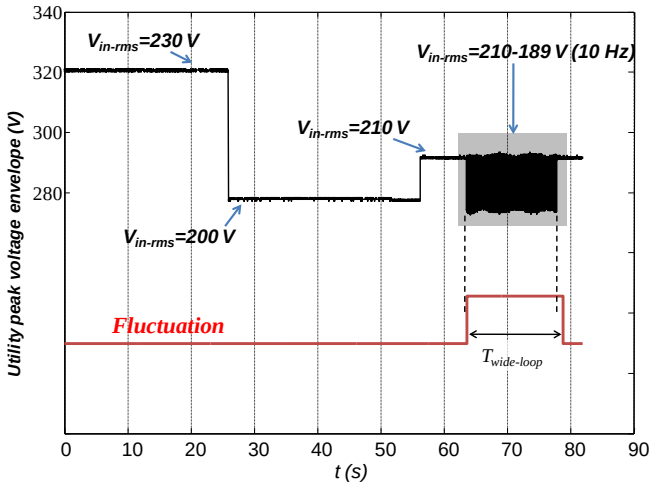


(a)

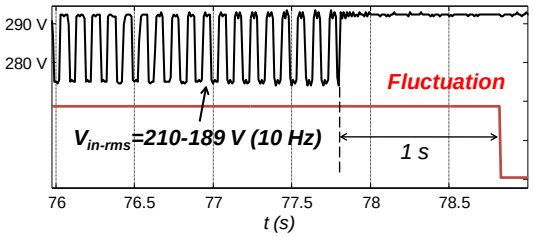


(b)

Fig . 8 *The PFC stage output voltage (v_o), the lamp light lux level measured by the photo sensor (lx_{LAMP}) and input voltage ($|v_{in}|$) under 10% V_{inRMS} and 10 Hz fluctuation. V_{in} = 230 – 207 V_{rms}, 50Hz, V_o = 420 V_{dc}, P_{in} = 150 W and C = 68 µF output capacitor: (a) With a reduced voltage loop bandwidth and (b) with a wide voltage loop bandwidth. Ch2 input voltage, 50 V/div, Ch1 lamp light flux. Ch3 output voltage 50 V/div. Time scale: 40 ms/div.*



(a)



(b)

Fig. 9 *Fluctuation signal: (a) Behaviour of the input voltage fluctuation algorithm under different utility voltage conditions. Utility peak voltage envelope (blue) and "Fluctuation" signal which indicates if a fluctuation is detected (red). (b) Time required for determining the steady-state condition after a utility voltage fluctuation.*