UNIVERSIDAD DE CANTABRIA

Departamento de Ingeniería de Comunicaciones

Tesis Doctoral

Analysis and Design Techniques for GaAs MMIC Circuits for Space Applications

Técnicas de Análisis y Diseño de Circuitos MMIC Basados en Transistores PHEMT de AsGa para Aplicaciones Espaciales

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HACE CONSTAR:

Que el trabajo titulado "*Analysis and Design Techniques for GaAs MMIC Circuits for Space Applications*" presentado por D. Marco Detratti , para optar al título de Doctor por la Universidad de Cantabria, Programa de Doctorado en Ingeniería de Comunicaciones, ha sido realizado en el Departamento de Ingeniería de Comunicaciones de la Universidad de Cantabria bajo su dirección y que reúne las condiciones exigidas a los trabajos de Doctorado.

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Abstract

The present work has been conceived with two main objectives in mind. The first one being to summarize part of the research and development activities carried out at the Department of Communication Engineering at the University of Cantabria in the field of GaAs Monolithic Microwave Wave Integrated Circuits (MMICs) design and implementation. This thesis presents in fact many newly developed MMICs covering the implementation of diverse functions and applications. All the circuits are described in detail together with the associated design flow, with emphasis both on its theoretical justification and its practical application.

The second objective is to serve as a guide and a supporting tool for future designs with the aim of facilitating the work of the MMIC designer, by presenting in detail the approach followed to ensure the correct functionality of the implemented circuits. Some new analysis methodologies will be also proposed with the potential to simplify and speed-up the design of complex circuits to ease and make more reliable the work of the microwave circuit designer in support of a *first-time-right* MMIC implementation.

The Thesis covers both scientific and technological aspects with direct industrial application in the space sector. Part of the developed technologies and designs, assembly and characterization information have been in fact transferred to the space industry in order to manufacture and commercialize a new generation of S-Band Transponder currently in use in more than 10 space missions.

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Acronyms and Abbreviations

ADS	Advanced Design System
AG	Auxiliary Generator
ASC	Auxiliary Subharmonic Circuit
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
CAD	Computer Aided Design
CDMA	Code Division Multiple Access
CL	Confidence Level
CMOS	Complementary Metal Oxide Semiconductor
CQFP	Ceramic Quad-Flat Package
DC	Direct Current
DCFL	Direct Coupled FET logic
Dff	D-Type Flip-Flop
ECL	Emitter-Coupled Logic
ECSS	European Cooperation for Space Standardization
E/D	Enhancement/Depletion mode
EO	Earth Observation
ESA	European Space Agency
ESD	ElectroStatic discharge
FET	Field Effect Transistor
GEO	Geostationary Earth Orbit
GNSS	Global Navigation Satellite System
GPS	(NAVSTAR) Global Positioning System
GSM	Global System for Mobile Communications
HB	Harmonic Balance

IC	Integrated Circuit
IF	Intermediate Frequency
IMF	Image (rejection) Filter
IP_x	x-dB Input Intercept Point
LEO	Low Earth Orbit
LHP	Left Hand Poles
LNA	Low Noise Amplifier
LO	Local Oscillator
LTI	Linear Time Invariant
LTV	Linear Time Variant
MCMM	Multi Chip Multifunction Module
MEO	Medium Earth Orbit
MIMO	Multiple Input Multiple Output
MMIC	Monolithic Microwave Integrated CIrcuit
MPA	Medium Power Amplifier
NF	Noise Figure
NFmin	Minimum Noise Figure
OIP_x	x-dB Output Intercept Point
OQPSK	Offset-QPSK
PA	Power Amplifier
PCB	Printed Circuit Board
PDF	Probability Distribution Function
PHEMT	Pseudomorphic High Electron Mobility Transistor
PLL	Phase Lock Loop
PM	Phase Modulation
PRB	Pseudo Random Binary
PSK	Phase Shift Keying
P1dB	Output 1dB Compression Point
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHP	Right Hand Pole
RX	Receiver

SAW	Surface Acoustic Wave
SCFL	Source Coupled FET Logic
SISO	Single Input Single Output
TAS-E	Thales Alenia Space- España
TC	TeleCommand
TDRSS	Tracking and Data Relay Satellite Services
TM	TeleMetry
T/R	Tranceiver
TT&C	Telemetry Tracking and Control
TX	Transmitter
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
VSWR	Voltage Standing Wave Ration
V_{ds}	(transistor) drain to source voltage
V_{gs}	(transistor) gate to source voltage
V_t	Threshold Voltage
WCDMA	Wideband Code Division Multiple Access

Resumen

El presente trabajo de tesis se ha concebido con dos objetivos fundamentales. El primero, resumir buena parte de las actividades de investigación y desarrollo llevadas a cabo por el autor en el Departamento de Ingeniería de Comunicaciones (DICOM) de la Universidad de Cantabria en el campo del diseño de circuitos MMICs basados en AsGa.

El segundo objetivo, no por ello menos relevante, es servir como guía y herramienta de apoyo para nuevos diseños, con la meta de facilitar el trabajo de futuros diseñadores de MMICs presentando en detalle el procedimiento seguido para asegurar el funcionamiento correcto de los circuitos implementados. Al mismo tiempo y a través de la experiencia ganada en el diseño de múltiples funciones circuitales empleando prácticamente todas las herramientas de simulación disponibles, se han propuesto nuevas metodologías de análisis con el potencial de simplificar y acelerar el diseño de circuitos MMICs complejos.

Los circuitos y las correspondientes técnicas de diseño que serán objeto del presente trabajo tienen en común los siguientes aspectos:

- Se apoyan en la misma tecnología de fabricación (AsGa)
- Se han desarrollado orientadas al campo de aplicación de las comunicaciones vía satélite (dando lugar, en algunos casos, a componentes calificados para espacio)
- Su diseño e implementación se basan en procesos muy complejos

Debido principalmente a los estrictos requisitos espaciales, los grados de libertad del diseñador quedan muy reducidos, lo que representa un reto para el diseñador ya que la creatividad y capacidad de encontrar nuevas soluciones están limitadas por restricciones de diseño, no usuales en las tareas de investigación y desarrollo, que tienen prioridad sobre los requisitos de funcionamiento, penalizando por tanto la consecución del "estado del arte".

El diseño de MMICs fiables ha de apoyarse en la inclusión, dentro del flujo de diseño, de una serie de pasos enfocados a asegurar la robustez del proceso de fabricación ante variaciones de los parámetros del proceso o variaciones de la temperatura. Es importante subrayar que estos aspectos no pueden ser evaluados a posteriori, pero deben constituir una etapa en el proceso de análisis y diseño.

Por esta razón el trabajo se focaliza en establecer unas directrices de diseño de MMICs para la implementación de diversas funciones y aplicaciones, con especial énfasis en su justificación teórica, su aplicación práctica y la validación de los circuitos resultantes de la implementación correcta ya en la primera serie de fabricación.

Los circuitos que serán descritos (que son una parte de todos los que se han desarrollado a lo largo del tiempo de esta tarea; se hará referencia en el último capítulo a algunos de los restantes) combinan la implementación de funciones lineales (amplificadores) y no lineales (divisores de frecuencia, mezcladores). En los últimos casos, debido a las dificultades encontradas a la hora de simular de manera eficiente el comportamiento de los circuitos a través de las herramientas de simulaciones disponibles (CAD), las mismas técnicas de simulación han sido objeto de un estudio teórico que ha llevado a cabo el desarrollo de interesantes aplicaciones de las herramientas de simulación que pueden explotarse como metodología general de diseño para su aplicación a circuitos no lineales.

La tesis cubre tanto aspectos científicos como tecnológicos, orientados a concretas aplicaciones industriales en el sector espacial. De hecho, parte de los resultados conseguidos ha permitido, en el marco de la contribución del grupo de investigación de diseño de MMICs del Departamento de Ingeniería de Comunicaciones de la Universidad de Cantabria, el desarrollo de una nueva generación de transpondedores en banda S que se encuentra en uso en más de 10 misiones espaciales (Anexo I).

Contenidos de la tesis

La descripción de las tareas que han fundamentado la consecución de los objetivos mencionados anteriormente se ha organizado del siguiente modo:

El primer capítulo presenta el contexto y los objetivos clave de esta tesis doctoral, focalizándose en el diseño y las técnicas de análisis de circuitos integrados de AsGa a medida y específicamente para aplicaciones espaciales.

El segundo capítulo describe el primero de los circuitos diseñados e implementados (un amplificador de ganancia variable: VGA) y la metodología de diseño asociada para este tipo de circuito. La metodología está fundamentada analíticamente y permite el diseño de VGAs compactos con control lineal en dB y un amplio rango dinámico, así como una buena adaptación entrada y salida en todas las condiciones de ganancia.

El tercer capítulo cubre el diseño y la implementación de un MMIC multifunción orientado a la generación coherente de las múltiples frecuencias necesarias para la implementación de funciones específicas de Radio Frecuencia en módulos transmisores y receptores de sistemas por satélite. Se pondrá especial énfasis en el diseño de un divisor frecuencial digital cuyo funcionamiento ha sido cuidadosamente explicado y su implementación circuital muy detallada para facilitar el diseño de este tipo de funciones complejas.

El cuarto capítulo se centra en el diseño e implementación de un divisor frecuencial de doble módulo, como evolución del divisor frecuencial de razón fija descrito en el capítulo anterior. Se ha propuesto una nueva topología de divisor frecuencial de doble módulo que resuelve parte de los inconvenientes de los divisores de doble módulo convencionales. Adicionalmente se ha propuesto y validado una descripción analógica del funcionamiento de los divisores digitales de frecuencia a través de la extensión del concepto de "oscilador de anillo conmutado", que permite configurar divisores de razón variable de cualquier orden. El modelo analógico del divisor frecuencial se ha aplicado también a las herramientas de simulación, normalmente limitadas a divisores analógicos, con el potencial de acelerar y simplificar el diseño de circuitos complejos con gran número de no linealidades, proporcionando información adicional como la respuesta de ruido de fase del circuito.

El quinto capítulo describe el diseño, implementación y test de un conjunto de MMICs de RF orientado a la producción industrial de una nueva generación de traspondedores multimodo en banda S reconfigurables en órbita para telecontrol y telecomando (TT&C).

Además de los circuitos presentados previamente, se presentan dos nuevos circuitos (un amplificador de bajo ruido y un amplificador driver de potencia con ganancia variable). El conjunto desarrollado demuestran como la metodología de diseño que ha

sido seguida, junto con las técnicas de análisis aplicadas ha resultando en una familia de MMICs actualmente en uso en una pluralidad de misiones espaciales.

El sexto capítulo presenta en detalle una metodología propuesta para determinar la estabilidad de un circuito no lineal de tres puertas basado en la generalización del factor de estabilidad μ de un circuito de tres puertas lineal, aplicado a parámetros S linealizados en gran señal y obtenidos bajo bombeo de gran señal. La técnica de análisis ha sido validada aplicándose a un mezclador MMIC de AsGa, que, aunque no estaba directamente relacionado en su aplicación con las otras implementaciones de MMICs presentadas en la tesis, podía ser igualmente utilizable en otros circuitos MMIC de los que componen la familia de esta tesis.

Finalmente el último capítulo presenta las conclusiones que pueden ser extraídas del trabajo llevado a cabo en el amplio periodo de actividad investigadora que recoge esta tesis y que ha dado lugar a diversas publicaciones y ponencias. Se mencionarán también otras publicaciones que han derivado posteriormente del bagaje de técnicas de análisis y diseño descrito en este trabajo.

1 . Introduction

1.1 MMIC CIRCUIT DESIGN AND ANALYSIS

A MMIC is a Monolithic Microwave Integrated Circuit. Monolithic…microwave…integrated…circuit…four words which entail a lot of fascination. For the majority of the people these words does not mean anything (even if unconsciously his daily life relies on them…), for us (designers and engineers) they mean something that is at the basis of our everyday work. They enable the translation into performance of end-user specifications (how better are computers today when compared to 30 years ago…) and the implementation of ideas into smart and compact systems otherwise impossible to implement, at the same time boosting the performance.

In a MMIC, passive elements and interconnects are fabricated on the same semiconductor substrate as the active devices. All the critical, microscopic circuit elements are defined on-chip through photolithography from a scaled-up mask. This eliminates the parasitic associated with component packages, leads, and solder pads.

Other advantages of the MMIC approach are reduced mass and volume with respect to conventional circuit assemblies, highly repeatable performance, and low-cost fabrication in large-quantities. The MMIC approach does have its disadvantages too. Passive elements on a MMIC chip typically have lower Q than what is available in discrete packages or on other substrates and power handling capacity is reduced (even if progresses are being made with the advent of new IC semiconductor technologies). Post-fabrication tuning of circuit elements is almost impossible, requiring the more challenging circuit designs to go through multiple iterations before acceptable performance is achieved. Further, the complexity of MMIC fabrication leads to extremely long iteration times. A MMIC designer must often wait many months, before making revisions and checking performance of the proposed solution, hence ensuring

that the simulated performance matches as much as possible the measured one becomes of utmost importance.

MMIC are small circuits, yet they are complex and “fragile”, and there are not a lot of people doing this type of design work. In no way a single MMIC design is the same as another and high level of expertise and knowledge is thus required to develop functioning and high performance circuits, especially when targeting space and high reliability applications.

The implementation of a MMIC design involves a deep knowledge of circuits´ theory and a huge number of circuit simulations, layout, fabrication, and testing steps. The large number of variables involved in these steps makes it imperative that all facets of the implementation be documented to assure repeatability and improve the yield of the final product. Simplification of the analysis technique used in support of successful designs (ideally targeting “first-time-right” implementations) can greatly help a designer in his job and shorten the design lifecycle.

The system priorities and practical constraints underlying the implementation of an MMIC may be quite different. Differences in applications, functionalities, economic factors, manufacturability, and even the currently available test equipment may force the designer toward a completely different solution than would be appropriate for a similar microwave engineering project

.A well-documented and step-by-step MMIC design methodology ensures a much smoother and faster turnaround of circuits. Circuit designs along with information relating to layout, processing, and testing should be preserved and used for future applications, thereby eliminating duplication of effort and providing substantial time and cost savings. This also increases the probability of first-time success for new designs.

The use of Computer Aided Design (CAD) tools plays a pivotal role in first-time success and yield of a MMIC design. A proper analysis and yield optimization becomes especially relevant when considering the small quantity of MMIC required for space applications compared with those for commercial applications. Since the wafer cost is a fixed parameter, to optimize the yield with the minimum production it is necessary to reduce the circuit sensitivity with respect to the process variations.

The design and implementation of a custom MMIC must take into account the customer needs/requirements (translated into detailed circuit specifications), the technology, and the processing capabilities. Detailed understanding of the requirements is necessary to avoid attempts to force-fit a design into an unsuitable process or to require performance parameters that cannot be supported by the process, which can create substantial cost and schedule delays, low yield, and a product of suspect reliability. The following consideration must be addressed:

- Suitability of technology and process to design requirements;
- Availability of existing models and CAD simulation tools;
- Cost, schedule, and performance trade-off.

Several factors may have a direct or an indirect impact on circuit yield and reliability. Device parameter variations as a result of process limitations or level of control, raw material variations, and EM proximity effects all play roles in determining overall circuit reliability and yield. The approach for achieving a reliable design should take into account the following:

- Definition of realistic performance requirements in response to the design specifications;
- Selection of adequate topology;
- Use of adequate simulation and test tools.
- Devices and processing characterization and variation (analysis and simulation);
- Understanding of potential failure mechanisms.

The definition of realistic and achievable performance requirements and the selection of the adequate topology to meet design needs is probably the most important initial step in MMIC design. Pushing the design-performance boundaries may result low yield and may have an impact on the reliability of the selected components. When targeting commercial and space applications (as was the case of all the circuits which will be presented in this work) the main focus should be ensuring that the circuit would work properly and the room for circuit innovation is not much. The design should be based on the simplest possible configuration meeting the RF specs in order to keep the size of the MMIC as small as possible and to avoid simulation errors due to design.

In order to ensure a high rate of success, for every MMIC design it is important to follow a systematic approach and documented design methodology. A typical process flow is illustrated in Figure 1.1 where the required inputs for every step are also identified.

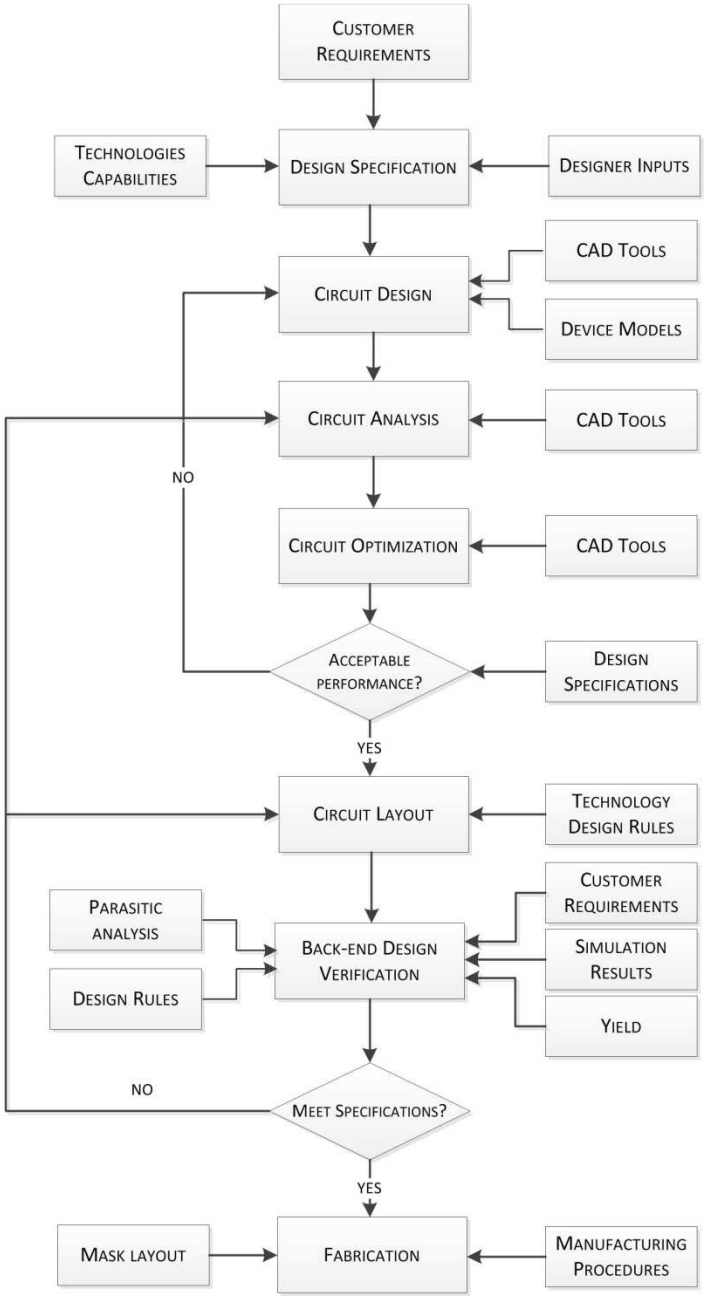

Figure 1.1: Typical MMIC circuit design and implementation flow

This approach has been followed for the implementation of the MMIC circuits which will be described in the following chapters. The most time consuming part of a circuit design is associated to the analysis and optimization, especially in the cases in

which complex non-linear functions are implemented. Specific emphasis has been put in order to ensure the most efficient analysis methodology aiming at saving as much as possible design life-cycle while at the same time preserving the usefulness of the results. In some cases this has resulted in the application of new methodologies, which may allow significant time reduction for future designs.

1.2 PURPOSE AND SCOPE OF THE WORK

The present work has been conceived with two main objectives in mind. The first one being to summarize part of the research and development activities carried out at the Department of Communication Engineering at the University of Cantabria in the field of GaAs MMIC circuit design. This thesis presents in fact many newly developed MMICs, both the chips themselves and systems that use them. The MMIC chips are described in detail, as is the role they play in the system in which they are used. Multi-chip modules are also presented with specific attention given to the practical details of MMIC packaging and multi-chip integration.

The second objective, not less important, is to serve as a guide and a supporting tool for future designs, with the aim of facilitating the work of new MMIC designers, by presenting in detail the approach followed to ensure the correct functionality of the implemented circuits. At the same time, exploiting the experience gained during the multiple designs and through the use of almost all the available simulation tools, some new analysis methodologies have been proposed with the potential to simplify and speed-up the design of complex MMIC circuits.

The circuits and techniques which will be object of the present work have the following commonalities:

- Rely on the same fabrication technology (GaAs)
- Have been developed with the target application field being satellite communication (in some cases resulting in space qualified parts)
- The design and implementation demands for complex and time consuming processes

All the problems associated to this type of applications, which affect enormously the design of any circuit implementing a specific functionality have been faced in the

development of the presented circuits. The degrees of freedom left to the designer, due mainly to the strict spatial requirements, were reduced to a minimum, representing a huge challenge for the designer himself in that its creativity and capacity to find novel solutions are blocked by the several obstacles in the design restrictions as several aspects, not normally contemplated in a pure R&D implementation, become the first priority in detriment of state-of-the art performance.

Designing of MMIC for reliability and robustness has to be supported by the inclusion, within the design and implementation flow, of a series of steps aiming at ensuring the robustness of the fabrication process towards process parameter and temperature variations. It is important to underline how these aspects could not be evaluated "a-posteriori" but should constitute an integral step of the analysis and design process.

For these reasons, this work aimed at establishing MMIC design guidelines for the implementation of diverse functions and applications, with special emphasis on its theoretical justification, its practical application and validation of circuits which have resulted in a first-time-right implementation.

The circuits which will be described (which do not constitute the totality of the circuits which have been developed during the research periods, some of which will be referenced as foreground in the last chapter of this thesis) encompass the implementation of both linear (e.g. amplifiers) and non-linear (e.g. frequency dividers, mixers) functionalities. In the latter cases, due to the difficulties faced for the efficient simulation of the circuits, the analysis techniques have been also object of theoretical research resulting in interesting applications of the available CAD simulation tools to be potentially exploited as generic analysis methodologies for non-linear circuits.

The implementation of the MMIC is accompanied by a detailed description (where possible) of the implementation, assembly and characterization of the circuit and, as a further support to the MMIC designer, the proposal for a MMIC package modeling which could be further extended to other microwave packages.

The Thesis covers both scientific and technological goals and with direct industrial application in the space sector. Part of achieved results has a concrete industrial application, since the research group from the Universidad de Cantabria, have contributed with these circuits' implementation to the development and

commercialization of a new generation of S-Band Transponder currently in use in more than 10 space missions (ANNEX I)

1.3 **WORK OVERVIEW.**

Because of the scope of this Thesis (and the many years of work summarized in this dissertation), it is worthwhile to provide an overview of the work as a whole before discussing the various chip designs, analysis techniques, implementation results and proposed innovations in the remaining chapters. The activities carried out in support to the achievement of the above mentioned objectives have been arranged as follows:

This first chapter present the context and the key objectives of this PhD. Thesis, focusing on the design and analysis technique of GaAs custom Integrated circuits with a specific focus of their use in space applications.

The second chapter describes the first circuit designed and implemented (a Variable Gain Amplifier, VGA) and an associated design methodology for such a type of circuits. The methodology is analytically supported and allows the design of compact VGAs with linear-in-dB gain control characteristic and wide dynamic range as well as good input/output match in all gain conditions.

The third chapter covers the design and implementation of a complex multi-function MMIC circuit targeting the coherent generation of multiple frequencies needed for the implementation of specific radio frequency functions in a transmit and receive modules of satellite systems. Special emphasis is given in the design of the digital divider which behaviour has been carefully explained and its circuital implementation detailed in order to ease the design of such complex circuits.

The fourth chapter deals with the design and implementation of a dual-modulus frequency divider circuit, as an evolution of the fixed ratio divider described in the previous chapter. A new dual-modulus frequency divider IC topology has been proposed which overcome some of the drawbacks of conventional dual-modulus dividers. Additionally, an analogue description of the functioning of digital dividers is

proposed and validated through the extension of the "*switched-ring oscillator*" concept to describe variable-ratio dividers, potentially serving as a design guide for any kind of multiple ratio frequency dividers. The analogue modelling is then applied to simulation tools whose utility is normally limited to analogue dividers with the potential of speed-up and simplify the design of complex digital circuits with a high number of non-linearities providing additional information, like phase noise response of the divider.

The fifth chapter describes the design, implementation and testing of a production-oriented RF chip-set to be used in a new generation of multi-mode and in-orbit reconfigurable S-band Satellite Transponders for TT&C. In addition to the circuits described in the previous chapters two additional circuits are presented demonstrating how the design methodology which has been followed, together with the analysis techniques applied, resulted in a family of MMICs currently in use in a plurality of space missions. Issues such as suitable circuit topology, efficient DC biasing, circuit area minimization, cost-oriented system design and advanced packaging techniques have been addressed during the design.

The sixth chapter presents in detail a particular methodology to determine stability in nonlinear three-port circuits based on a generalization of the three-port μ-stability factor applied to linearized S parameters under large-signal pumping. The analysis technique was validated using as example a designed and fabricated GaAs MMIC mixer, not directly related with the implementation of the previously described family of MMIC circuits (as the circuit was targeting a different application), by exploiting the different analysis and design techniques used for the development and characterization of the other GaAs circuits described in this work.

Finally, the latest chapter includes the conclusions which could be drawn from the work carried out during this extensive research work (which has led to different publications and papers) together with a mention of some additional foreground which have already directly benefit from the design and analysis techniques described in this work.

2 . Variable Gain Amplifier with input matching compensation

2.1 INTRODUCTION

Variable Gain Amplifiers (VGAs) with wide dynamic ranges are required in any wireless communication systems. Figure 2.1 shows, as an example, a traditional heterodyne transceiver used in mobile communications.

The VGAs need to fulfill two important functions. The first one is the provision of a variable dynamic range to compensate for input signal power variations as RF Front End components like Low Noise Amplifiers (LNA), Power Amplifiers (PA) and mixers have usually fixed gains. Therefore VGA has to provide most of the dynamic range of the system. Secondly, VGAs are used for controlling the transmission signal power or for adjusting the received signal amplitude and the gain-control characteristic should be linearly controlled in the dB scale for ease of transceiver design.

In a Wideband Code-Division Multiple Access (WCDMA) wireless communication systems [2.1], the VGA plays a fundamental role in optimizing system capacity. Since multiple users can share the same carrier frequency, the transmitter gain has to be regulated so that equal power is received at the base station from each user. In constant-envelop applications such as the GSM, output power control is usually implemented by adjusting the bias of the PA. However, this approach is not suitable for linear modulation systems such as WCDMA because bias variations strongly affect PA linearity. Therefore properly designed VGAs are necessary. At the same time they are used for adjusting the received signal amplitude in order to keep the signal to the A/D input constant.

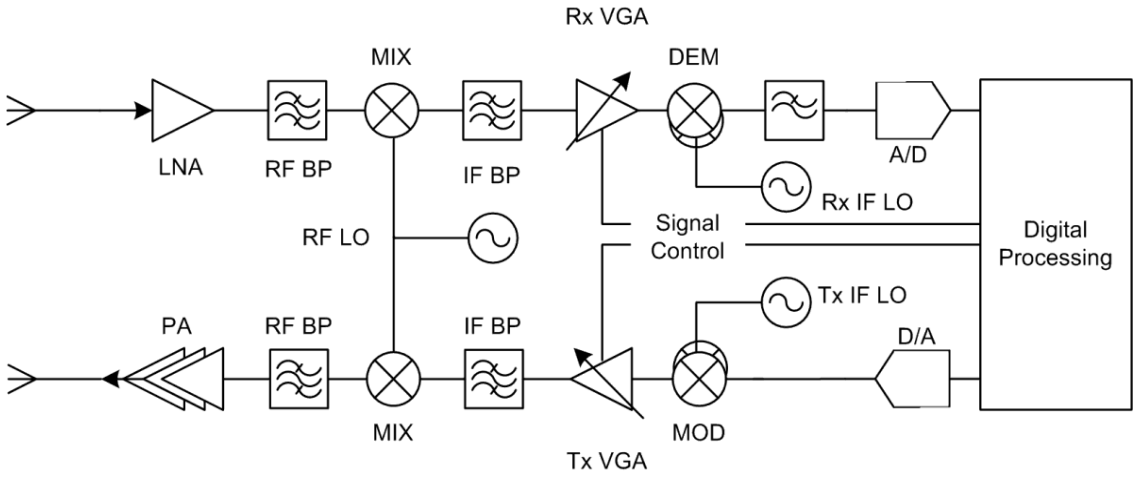

Figure 2.1: Conventional Receiver/Transmitter Front-end.

The use of FETs arranged in PI, TEE and bridged-T is quite common in the design of Voltage Controlled Variable Attenuators [2.2]. A combination of such kind of circuits with conventional amplifiers may results in VGA with good performance. The main problem is that, in general, due to the intrinsic non-linearity of the FETs, they do not allow a linear gain control characteristic [2.3]. A problem which can be resolved using an external linearizing circuitry [2.4], complicated control voltage schemes, or multiple control voltages [2.5]resulting in bigger and complex networks. Moreover, an aspect that usually is not taken into account is the need for maintaining simultaneous input and output match at all gain levels ([2.6], [2.7]) condition which is of outmost importance to ensure good power transfer. External matching networks or balanced solutions have been proposed [2.8], but this solution is inadequate to keep power consumption and layout area at the minimum.

The methodology proposed allows the design of compact VGAs with linear-in-dB gain control characteristic and wide dynamic range as well as good input/output match in all gain conditions, embedding in a straightforward manner series and parallel FET resistors in the amplifying chain.

The method is theoretically supported and has been validated with the design of a monolithic VGA using a commercially available GaAs PHEMT technology. Several VGAs have been tested and excellent agreement between the measured and predicted results has been achieved. The power handling capability of the fabricated circuit is also reported, showing that the proposed solution works well even when the circuit operates in minimum gain conditions, with the strongest signals at the input.

Originally designed to be inserted in a GaAs multifunction chip for use in satellite system [1], it showed performance suitable for its use even in WCDMA systems at 1.95GHz to directly drive the power amplifier.

2.2 DESIGN OBJECTIVES

The initial goal of the design was the development of a VGA for use in receive chains of S-band satellite transponders to control the signal power that enters the mixers for gain or input power variations compensation. Noise performance was to be maintained below reasonable levels around the maximum gain of the VGA. The design must assure good input/output VSWR and the lowest inter-modulation distortion in order to not degrade the power linearity of the system.

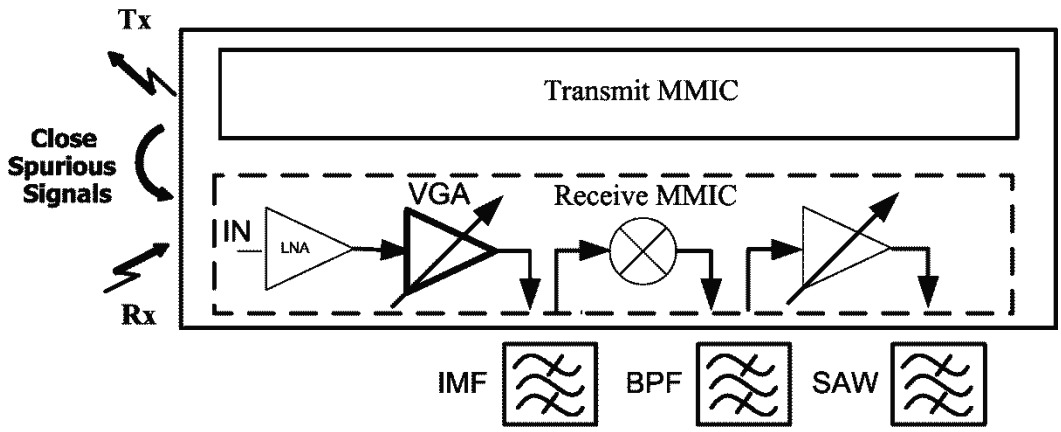

Figure 2.2: Simplified block diagram of the RF circuitry in a satellite transponder.

In Table 2.1 are summarized the initial specifications for the circuit.

As the circuit will be placed after the input LNA, Noise figure values up to 7dB can be tolerated given the relatively high gain of the VGA. Despite the input signal power level for which the VGA is intended is low, a spurious signal with a level of up to –10dBm is always present at the input due to transponder frequency planning and can be eliminated only after the SAW filter (Figure 2.2). This situation requires good power handling capability with an input 1dB compression of at least –10dBm at each gain

[1] Project ref. number TIC2000-0459-P4-03 "Módulos de Radiofrecuencia Monolíticos para equipos embarcados (MORFEO)"

value. Design targets were an output P1dB over 10dBm and OIP3 over 20dBm at maximum gain with minimum degradation when gain is varied. At least 30 dB of dynamic range was specified with good matching (VSWR <1.4) in all the conditions.

Table 2.1: VGA Design specifications

Id	Characteristic	Value			Units	Conditions
		Min.	Typ.	Max.		
V_{cc}	Power Supply		3.5		V	
I_d	Current			40	mA	
F_o	Center Freq.		2.07		GHz	
BW	BandWidth		200	400	MHz	@maxgain
Z_{in}	Input Impedance		50		Ω	
Z_{out}	Output Impedance		50		Ω	
RL_{in}	Input return loss		15		dB	@maxgain
RL_{out}	Output return loss		15		dB	@maxgain
ISOL	Isolation	35	40		dB	
G_{max}	Max. Power gain	17			dB	@$V_{ACG(L)}$
G_{flat}	Gain flatness		1		dB	in BW
G_{slope}	Gain slope		0.03		dB/MHz	in BW
NF	Noise Figure			7	dB	
GCR	AGC Dynamic Range	30			dB	$V_{ACG(H)}$ to $V_{ACG(L)}$
OIP_3	Output intercept point		20		dBm	@maxgain
OP_{1dB}	Output 1dB Compression		10		dBm	@maxgain
IP_{1dB}	Input 1dB Compression	-10			dBm	@ all gain
T	Temperature	-30	25	70	ºC	

2.3 CIRCUIT DESIGN METHODOLOGY

2.3.1 Amplifier Design

The first step carried out was the design of a an amplifier with a fixed gain in excess over the specification, to compensate the inevitable losses introduced by the attenuator network that would be embedded with the proposed methodology in a second step.

The amplifier was designed to provide around 22dB gain with a two stage configuration. Each of the two stages has been optimized for low-noise and uses parallel feedback to guarantee stability at all frequencies. The widths of the first and second stage transistor were chosen to give an output power better than +12dBm and a sufficiently high OIP3 of more than 22dBm.

2.3.2 **Gain Control Circuit**

Once designed the amplifier, the objective was to embed in the circuit a network capable of providing a linear-in-dB gain control mechanism with enough dynamic range, maintaining good matching and without affecting the power handling capabilities of the amplifier at every gain value. The solution should be compact in order to reduce occupied area, and with a simple and reliable configuration to cope with the spatial environment requirements. The initial idea was to use a zero-biased FET as a variable attenuator controlled by the gate voltage [2.9] connected in parallel with the input of the amplifier.

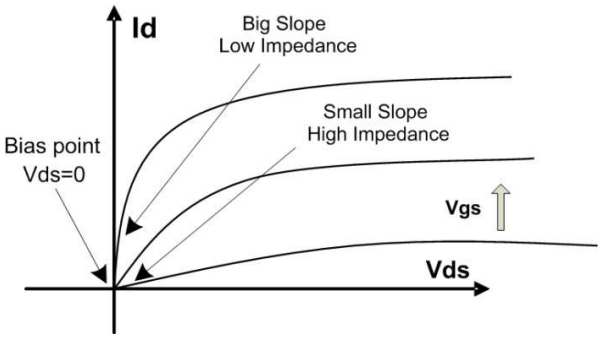

Figure 2.3: Functioning principle of a zero-biased FET used as variable impedance

As the gate voltage is varied, the impedance presented to the network is changed, hence implementing a gain control mechanism through a variable resistor. Doing so, the slope of the I_d/V_{ds} curve is modified, and the FET (depending on its size) presents towards external circuitry impedance values ranging from few Ω up to KΩs (Figure 2.3).

In a shunt configuration the series resistance is kept at minimum, so reducing the insertion losses of the attenuator network. As the value of FET-resistance decreases (at maximum gain the transistor is in OFF state and the resistance behaves almost as an open circuit) the level of attenuation increases. A bigger amount of signal is derived on

the resistor, thus preventing the degradation of distortion characteristics in low-gain conditions.

This solution (Figure 2.4) presents two problems. Firstly, the gain control curve of a single shunt FET results in only 12-16 dB dynamic range (depending on transistor width), not sufficient to meet system requirements.

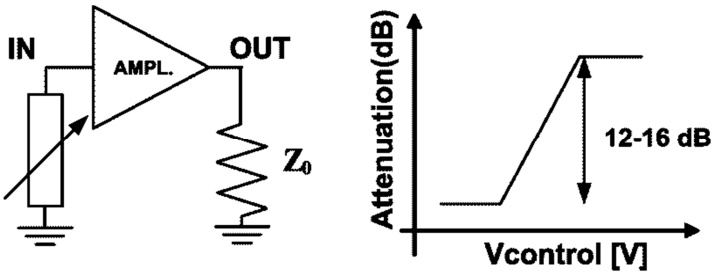

Figure 2.4: Shunt attenuator and his gain control range (Z_0=50Ω) as a function of the control voltage

The second problem is the mismatching originated when the attenuation level changes. One shunt FET corresponds to only one degree of freedom and only one condition can be imposed on the resulting network. This is the reason for which to simultaneously achieve attenuation and matching, a common solution is to add a conventional attenuator circuit at the input of the amplifier. A TEE network is in general preferred because of its better high frequency performance [2.2]. Actually, to implement the gain control scheme is not necessary to add both series variable resistors. With only one series device, it is possible to obtain the same results but with reduced size and lower insertion losses. To maintain good input match at all attenuation levels (the output match is assured by the amplifier design and is not affected by the input network, given sufficient reverse isolation and gain) a second FET could be added in a "half-tee" configuration (Figure 2.5).

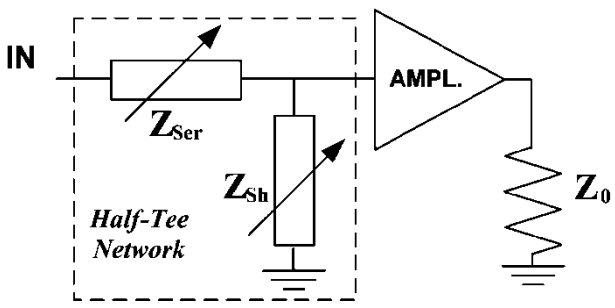

Figure 2.5: Topology of the half-tee network.

The ABCD matrix of the proposed attenuator network is given by:

$$\begin{bmatrix} 1+\dfrac{Z_{Ser}}{Z_{Sh}} & Z_{Ser} \\ \dfrac{1}{Z_{Sh}} & 1 \end{bmatrix} \tag{2.1}$$

Where Z_{Ser}, Z_{Sh} represent the series and shunt impedance of the variable resistors. Given the scattering matrix of the designed amplifier:

$$[S_a] = \begin{bmatrix} S11 & S12 \\ S21 & S22 \end{bmatrix} \tag{2.2}$$

And the scattering/transmission matrix transformations [2.7]:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{A+B/Z_0-C/Z_0-D}{A+B/Z_0+C/Z_0+D} & \dfrac{2(AD-BC)}{A+B/Z_0+C/Z_0+D} \\ \dfrac{2}{A+B/Z_0+C/Z_0+D} & \dfrac{-A+B/Z_0-CZ_0+D}{A+B/Z_0+C/Z_0+D} \end{bmatrix} \tag{2.3}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \dfrac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} & Z_0\dfrac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \\ \dfrac{1}{Z_0}\dfrac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} & \dfrac{(1-S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \end{bmatrix} \tag{2.4}$$

By using equations (2.1)-(2-4) and transmission matrix properties, it is possible to calculate the scattering matrix of the network built up by the half-tee and the amplifier $[S_{tot}]$ which is function of the amplifier scattering parameters and the (complex) values Z_{Ser} and Z_{Sh}:

$$[S_{11}]_{tot} = \frac{1}{\Delta} Z_{Ser}Z_{Sh}(S11-1) - Z_0(Z_{Ser}+2Z_{Sh}) - Z_0 S11(Z_{Ser}+Z_0)$$

$$[S_{12}]_{tot} = -\frac{1}{\Delta} 2Z_0 Z_{Sh} S21$$

$$[S_{21}]_{tot} = -\frac{1}{\Delta} 2Z_0 Z_{Sh} S12$$

$$[S_{22}]_{tot} = \frac{1}{\Delta} Z_0(Z_{Ser}+Z_0)(S12 \cdot S21 - S11 \cdot S22 - S22) - Z_{Ser}Z_{Sh}(S22 - S11 \cdot S22 + S21 \cdot S21) - 2Z_0 Z_{Sh} S22$$

$$\Delta = Z_{Ser}Z_{Sh}(S11-1) - Z_0(Z_{Ser}+2Z_{Sh}) - Z_0 S11(Z_{Ser}+Z_0)$$

Now, the conditions to be imposed are:

$$\begin{aligned} S_{11tot} &= 0 \\ S_{21tot} &= A \end{aligned} \tag{2.5}$$

Where A is a real value, such that $G_{\_dB}=20\log_{10}(A)$ is the desired gain in dB, ideally ranging from the amplifier gain to 0. It was experimentally verified that the effect of a non-zero value for the phase of S_{21} was negligible at the frequencies of interest (and in general below 3GHz), therefore for simplicity its value has been fixed to zero. Solving equations (2.5) with respect to the complex variables Z_{Ser} and Z_{Sh} the relationship between Z_{Ser}, Z_{Sh} and the amplifier parameters to meet the matching condition and provide the desired gain (or attenuation) can be established:

$$\begin{aligned} Z_{Ser} &= \frac{(S21 - A \cdot S11 - A)\cdot Z_0}{S21} \\ Z_{Sh} &= \frac{A \cdot Z_0 \cdot (1+S11)}{(S21 + A \cdot S11 - A)} \end{aligned} \tag{2.6}$$

Solution of (2.6) gives two complex impedance values (Z=R+iX). With the help of a circuital simulator (ADS), it has been checked (Figure 2.6), that the use of the real part of the solutions (which for clarity we will indicate with R_{Ser} and R_{Sh} respectively) represents a good first order approximation at low frequencies.

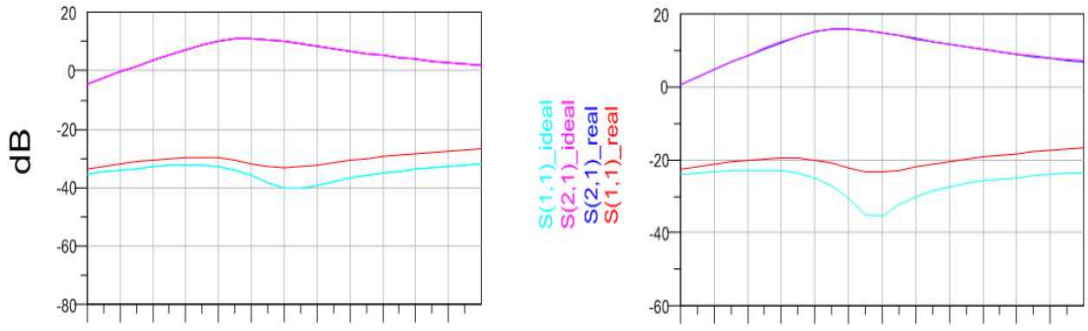

Figure 2.6: Comparison between exact (ideal) solution and real part approximation for two gain values ($G_{\_dB}$=10dB left, $G_{\_dB}$=15dB right)

The gain of the circuit in both cases is the same and the slight variation in the complex part does not prevent maintaining the input match below 20dB. Moreover, taking into account that (2.6) is solved at a single frequency and that during the design process the circuit will undergo to optimization to match with the performance in the whole band, the approximation was deemed acceptable for the design stage.

At higher frequencies, when the effects of the complex part of the solution become non-negligible, this approximation is no longer valid, and the problem should be solved by means of more complex external linearizing networks. Substituting the values of R_{Ser} and R_{Sh} obtained from (2.6), with two of ideal resistor in the *half-tee* configuration, and simulating the network coupled with the designed amplifier, values always better than 20dB for the input match were obtained at any gain level. As far as the gain is concerned, from Figure 2.7 it can be observed that ideally it should be possible to obtain almost an arbitrary value of gain reduction if the resistors were able to span the entire resistive range. In particular the series resistor should vary from 0 to 50Ω while the shunt resistor from a high impedance value (ideally an open circuit) to 0Ω.

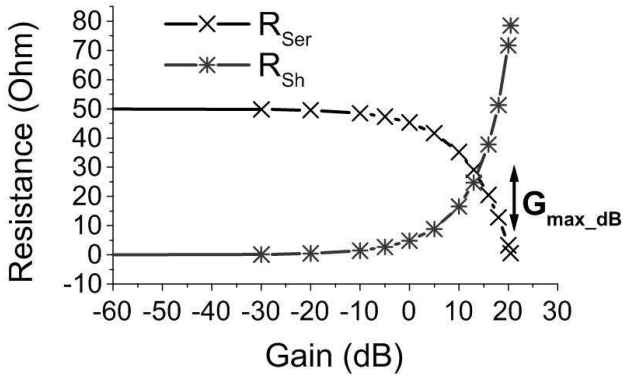

Figure 2.7: Dependence of attenuation level of the half-tee circuit on the values of the series and shunt resistor (G_{max_dB} is the gain of the sole amplifier)

Even if generally the electrical characteristics of each FET resistor can be modeled as a parallel combination of R and C, at the frequencies of interest the effect of the capacitor can be neglected in the design stage, and the approximation of a FET with a simple resistor fits well with the actual behavior.

The resistive range which can be covered by a zero-biased FET is limited by its physical parameters. The bigger the transistor gate width, the lower will result the open channel resistance (R_{min}), while at the same time the parasitic effects will increase. The lowest possible R_{min} would be required to minimize insertion losses of the resistive network (which contribute directly to the circuit noise figure and can severely degrade amplifier maximum gain), however trade-offs are needed to avoid too high values for the parasitic capacitance.

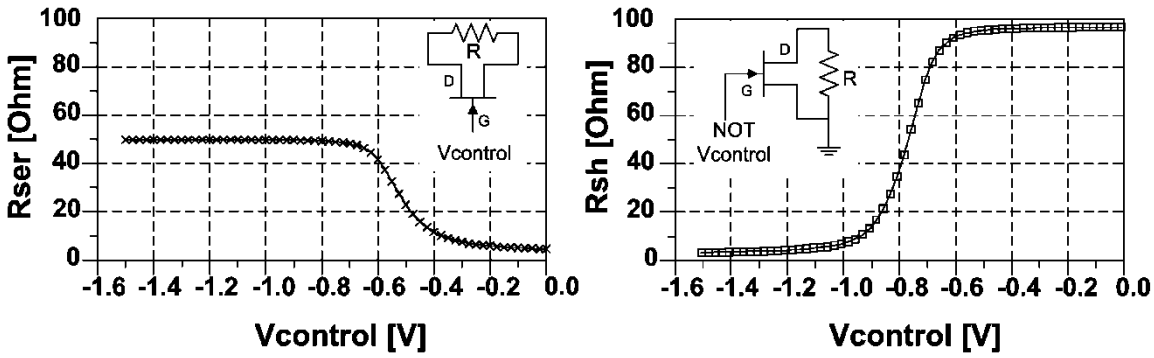

Figure 2.8: Series FET (gate width=240μm, R=100Ω) and shunt FET (180μm, 1kΩ) resistance as a function of the control voltage

In Figure 2.8 the behaviors of the series and shunt resistors associated to the selected FETs are plotted as a function of the applied gate control voltage. In both cases a resistor placed between drain and source has been used to DC-short circuit each transistor and to fit the resistive range with the desired behavior (Figure 2.7).

Care must be taken in the choice of this resistor in the series device, because it has to limit the overall series arm resistance to 50Ω when the control voltage is lower than the pinch-off voltage (V_t), situation in which the FET resistance is much higher than the required 50Ω. In the case of the shunt FET, at pinch-off it has to approach to a high resistance value and this is easily guaranteed by the high channel resistance in the off state.

A single voltage ($V_{Control}$) is used to control the bias of the two FETs, however the voltage applied to the two transistors is not the same. As the behaviour of the two FETs must be complementary, in the same way have to behave the relative control voltages. For the series FET V_{Series} (=$V_{Control}$) varies between 0 and –1.5 V around the pinch-off value (V_t=-0.9V for the chosen technology), while for the shunt FET its complementary V_{Shunt} should range from –1.5 to 0 V. Thus the two voltages are not independent, but constitute a complementary pair of the form:

$$V_{Shunt} = -1.5 - V_{Series} \tag{2.7}$$

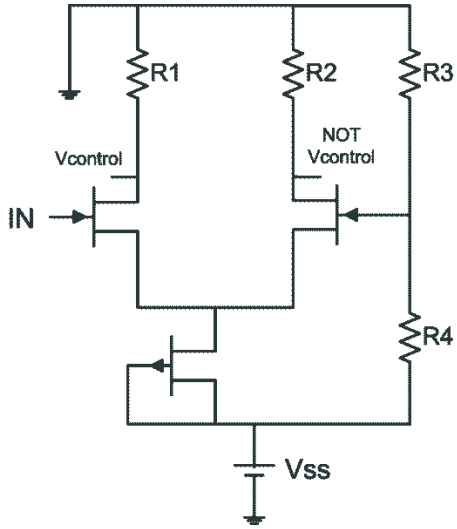

Figure 2.9: Complementary voltage generator

The generation of such signals from a single control voltage is relatively easy and can be implemented in a straightforward manner using the inverting circuit of Figure 2.9. Depending on the specific application R1 to R4 values can be selected to map an appropriate input signal into the required control voltages (source follower stages can be employed at the $V_{Control}$ nodes to obtain additional level shift).

Comparing the results obtained in Figure 2.8 with the ideal behavior of Figure 2.7, the proposed circuit approximation fits well in the $V_{Control}$ range between –0.4V and –1.5V. The final half-tee attenuator was designed using pHEMT FET transistors with gate widths of 240 and 180 μm for the series and shunt element, respectively.

Simulated performance showed a 3.0 dB insertion losses and 25dB control range over a wide bandwidth. This was still not sufficient to achieve the required minimum 30

dB dynamic range. A solution to this problem was found though the insertion of a second shunt FET between the first and second stage to provide the additional amount of attenuation. The gate width of the device (60μm) was optimized to achieve an overall dynamic range of 40dB. In this case the transistor has been DC-short circuited through an inductor, which was also used as part of the inter-stage matching network and to compensate for any parasitic effects of the FET. With this solution, the insertion of this switch between the two amplifying is almost transparent to the circuit behaviour and the only effect is a net increase the overall control range. This second shunt FET can be controlled by the same voltage that leads the first shunt circuit. The resulting circuit topology is sketched in Fig. 2.10 (bias circuitry is not included).

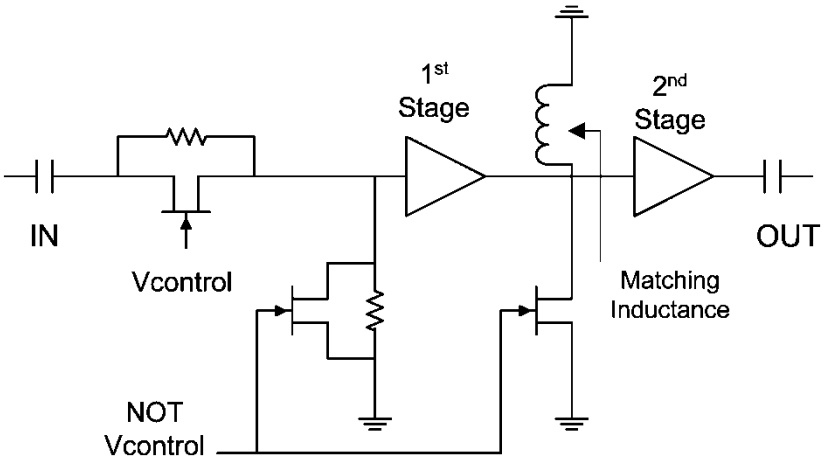

Figure 2.10: Simplified diagram of the VGA.

2.4 CIRCUIT IMPLEMENTATION

2.4.1 Electrical Schematic

Following the above guidelines the design of the circuit has been carried out with ADS and by using the component design models provided by the technology manufacturer. Figure 2.11 shows the final schematic of the circuit including all the components.

Both stages of the amplifiers are biased through properly sized on-chip inductors. Input/output decoupling capacitors and stabilizing networks have been also placed on chip to prevent out-of-band oscillations at high frequencies.

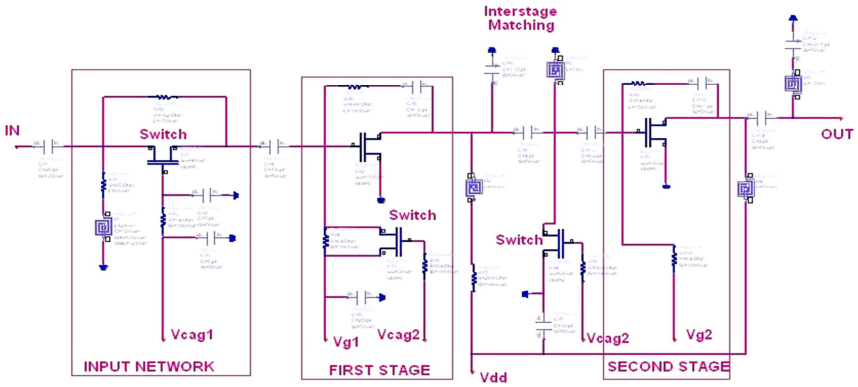

Figure 2.11: Electrical schematic of the VGA

2.4.2 **Layout**

The complete layout of the resulting circuit is shown in Figure 2.12.

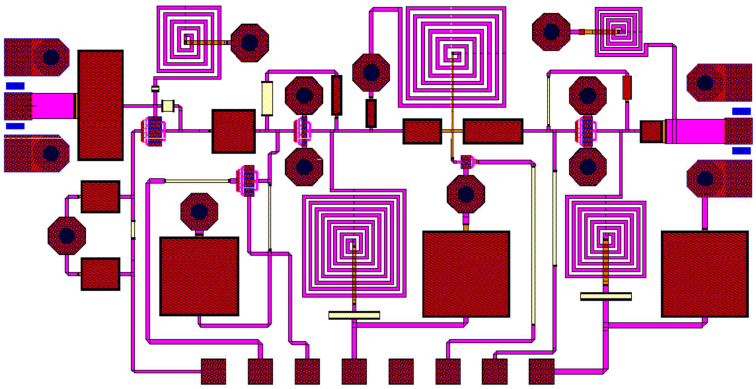

Figure 2.12: Layout of the VGA

Input/Output coplanar test points have been inserted to facilitate direct on-wafer circuit characterization. Also DC-bias and control voltage pins have been distributed within the chip to match with the available DC-probes.

2.5 **SIMULATIONS**

A summary of the simulations which have been carried out before circuit fabrication are presented in this section. In all the cases the input and output impedance are set equal to 50Ohm. The nominal (room) temperature is 25ºC, but tests at -30ºc and 70ºC have been made for thermal stability checks. All the results include the effects of the

input/output (600µm) and biasing (1mm) bonding wires (by using the model provided by the simulator).

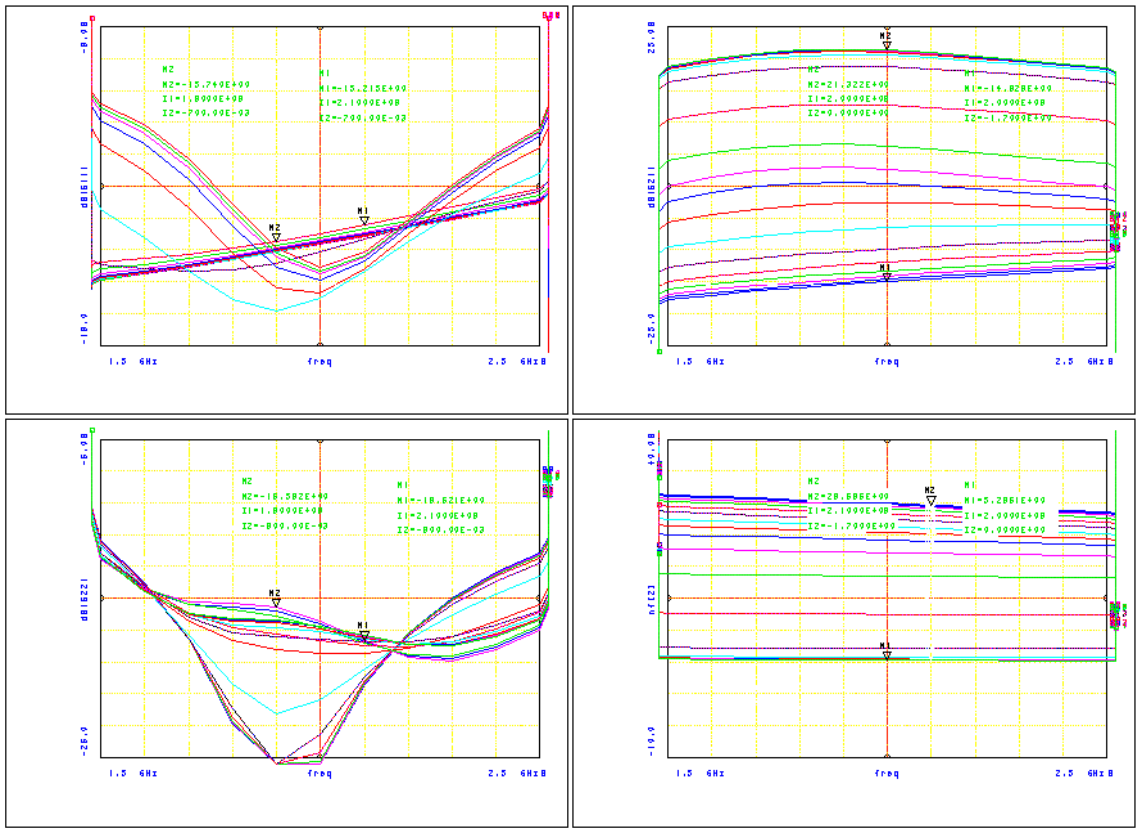

Figure 2.13: Scattering and Noise figure simulations as a function of V_c at room temperature

The control voltages $V_{cag1}=V_{series}$ and $V_{cag2}=V_{shunt}$, are linked by the following relationship:

$$V_{cag2}=-1.5-V_{cag1} \tag{2.8}$$

Only the value of V_{cag1} is used (V_c) is used in the graphs. Details of each simulation are described in the relative figure caption. Simulated results give a dynamic range wider than 35dB from 1.8GHz to 2.15GHz with an average maximum gain of 20dB within the operating bandwidth (Figure 2.13) maintaining good input matching in all conditions (despite a worsening in correspondence of the pinch-off voltage of the transistors used as switch which is associated to the strong nonlinear behaviour of the devices in such situation).

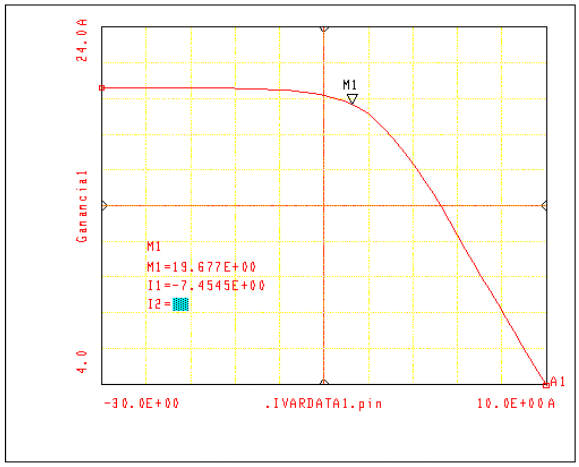

Figure 2.14: P1dB simulation at maximum gain (V_c=0). P1dB(output)≈ 12.2dB

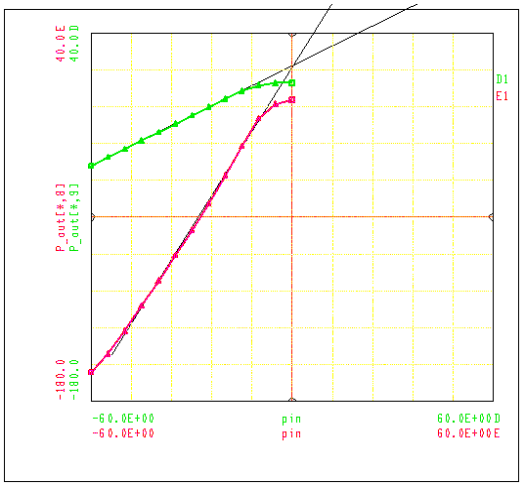

Figure 2.15: Simulated Output Third Order Intercept point at maximum gain (V_c=0). OIP3≈24.7dB.

2.6 MEASUREMENTS

The S-band MMIC VGA was fabricated with the commercial foundry process ED02AH from OMMIC (http://www.ommic.com). All the components were realized on chip occupying a layout area of 1.4x1.9 mm^2. Figure 2.16 shows a microphotograph of the circuit.

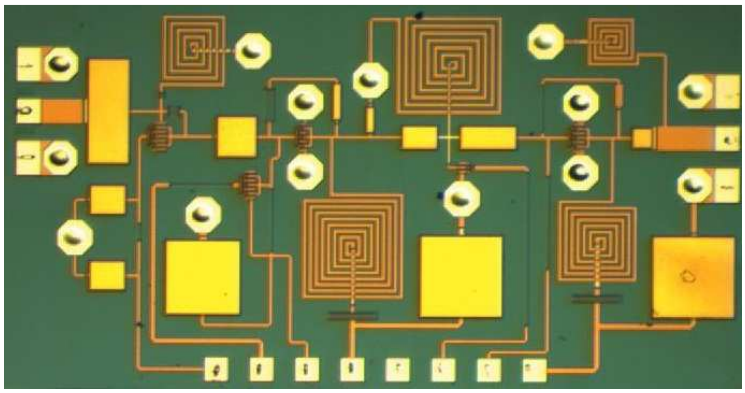

Figure 2.16: Microphotograph of the fabricated circuit. Layout area is 0.95 mm x 1.9 mm.

The circuit draws 34mA from a 3.5Vsupply voltage at the nominal temperature of 25ºC. All the results are plotted as functions of the control voltage $V_c = V_{Series}$ (V_{Shunt} is set accordingly to (2.8)).

The small signal characteristic of the VGA at different control voltages were measured on a Vector Network Analyzer with an input power of –20dBm. In Figure 2.17 is plotted the small signal gain at minimum, maximum and intermediate attenuation level compared with the corresponding simulation. A dynamic range of approximately 40 dB is achieved in a 20% bandwidth around 1.9 GHz. The excellent agreement between predicted and measured results of the first prototype demonstrates the accuracy of the method (as well as confirming the accuracy of the models).

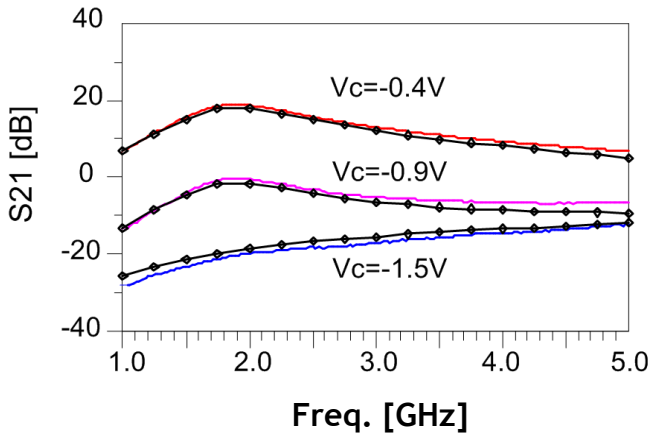

Figure 2.17: Magnitude of S_{21} as a function of frequency at different control voltages compared with the simulations (dotted lines).

Figure 2.18 and Figure 2.19 illustrate S_{11} and S_{22} variation over the same gain-control range. Both input and output match remains well below –10dB at all gain level. Noise figure was also measured, and a maximum value of 6.5 dB was measured at maximum gain (in line with simulated results).

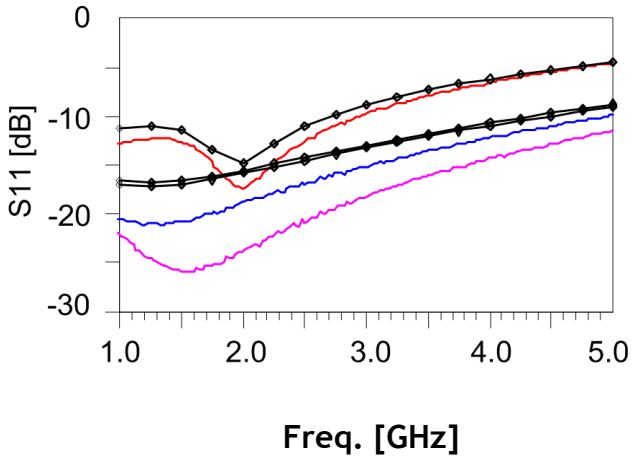

Figure 2.18: Curve of S_{11} at different control voltages versus simulation (dotted).

The gain control characteristic at 1.95GHz, showed in Figure 2.20, varies from –21dBm to +18.8dBm with a deviation from linearity of only ± 1.5dB in the voltage control range from –0.4V to –1.5V.

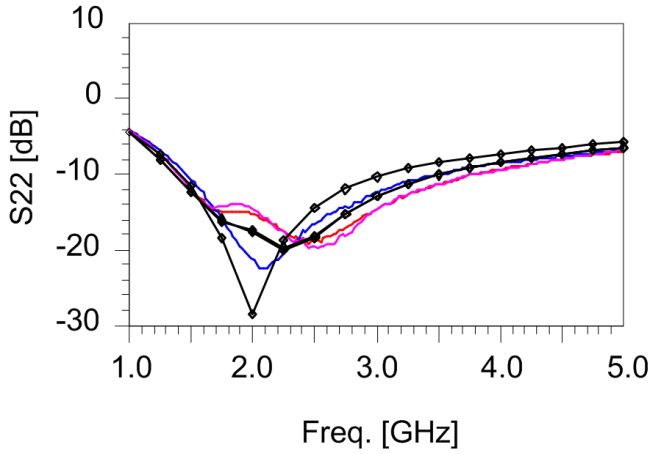

Figure 2.19: Curve of S_{22} at different control voltages versus simulation (dotted).

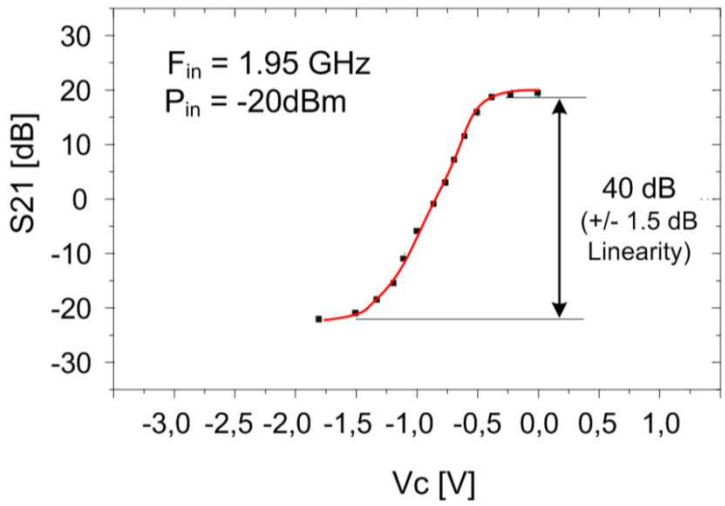

Figure 2.20: Gain control characteristic as a function of the control voltage

Multiple circuits were assembled and tested on wafer, and the results compared with the simulation at maximum and minimum gain (Figure 2.21) demonstrate the robustness of the design. The observed variations in the gain have to be associated to the fabrication process parameter variations (mainly g_m and V_t).

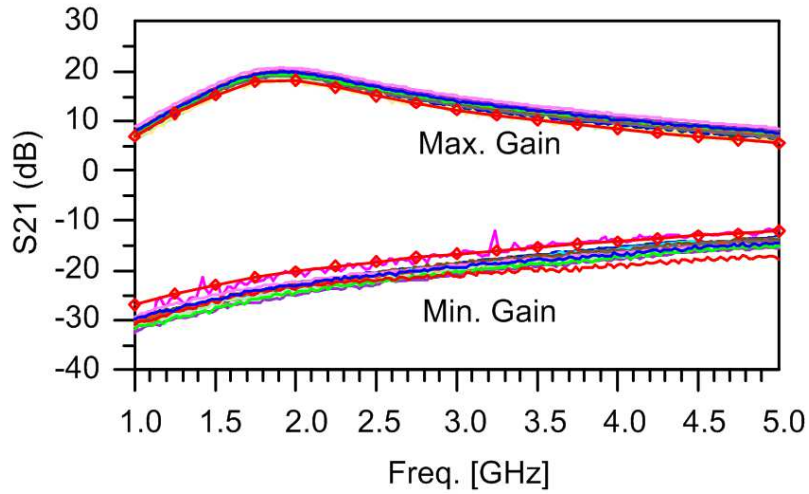

Figure 2.21: Measured maximum and minimum gain for 15 different VGA. Vs Simulation (Dotted lines)

The output 1dB compression point was also measured on wafer at the different control voltages, and the results are shown in Figure 2.22. Output P1dB of 12 dBm is obtained in the case of maximum gain with a saturate output power of +13.5dBm. In the same condition, third order intercept point was measured to be equal to +22.1dBm.

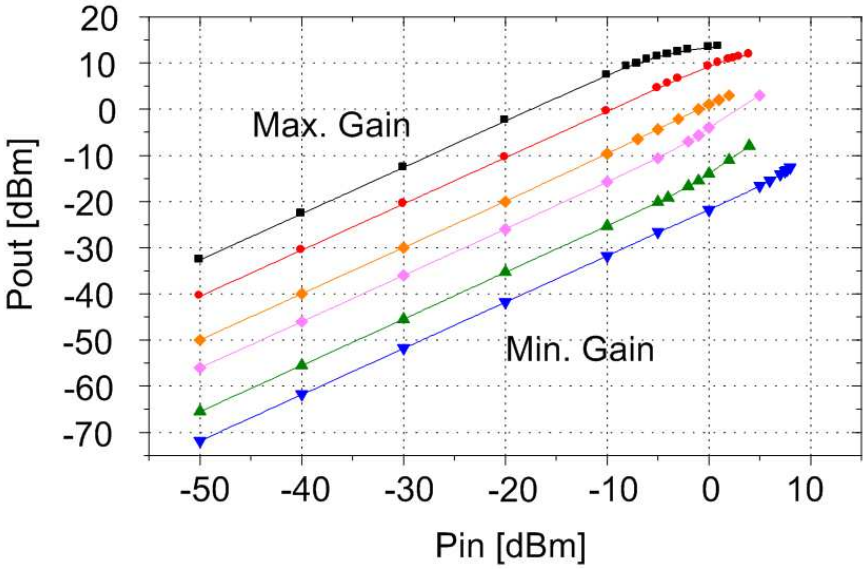

Figure 2.22: Measured output 1dB compression point at different control voltages.

According to the system requirements, the variation of input P1dB as a function of the control voltage was also monitored. As can be noticed the input P1dB decreases abruptly around the pinch-off voltage of the series FET however remaining always well below the desired level of –10dBm (Figure 2.23).

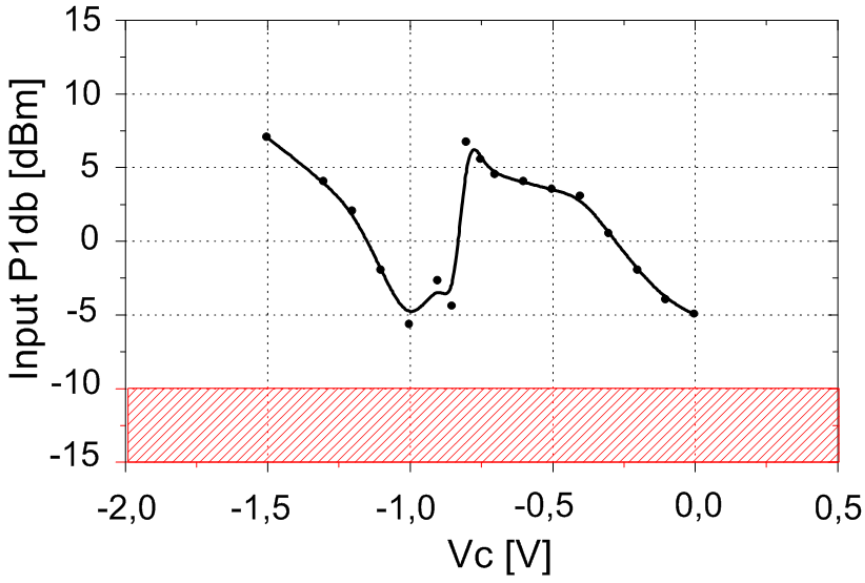

Figure 2.23: Input P1dB as a function of the control voltage.

This behavior has to be associated to the highly non-linear behavior of the input switch in that configuration which would need to be compensated.

Having observed a good large signal and inter-modulation behavior of the amplifier, and taking into account that the working frequency and relative bandwidth are also used in WCDMA systems, Adjacent Channel Power Ratio (ACPR) measurements have been carried out.

ACPR is an important test parameter for characterizing the distortion of subsystems and the likelihood that a given system may cause interference with adjacent channels. ACPR is a measures of the adjacent and alternate channel leakage power. Value for ACPR are set by the standard under consideration, which generally set high demands on the adjacent and alternate channel power ratio in order to ensure as much as possible interference free communications. The aim of the measurement was to evaluate if the proposed gain-control methodology was able to provide an inter-modulation distortion sufficiently low to be used even in cellular WCDMA systems. ACPR measurements are normally specified at two frequency offsets from the carrier (885 KHz and 1.98 MHZ, adjacent and alternate channel respectively) and a measurement bandwidth of 30 KHz.

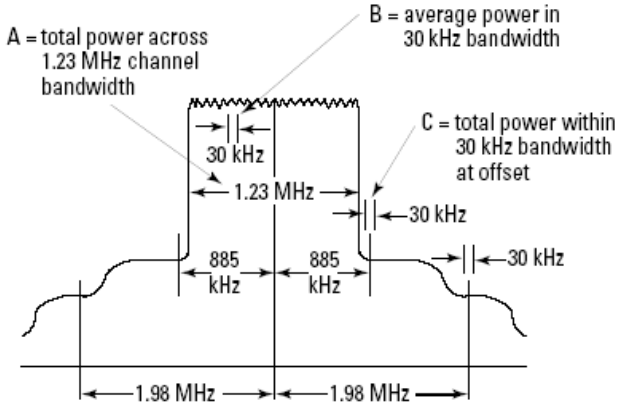

Figure 2.24: ACPR specification

The adjacent channel power-ratio method compares the power in the specified adjacent-channel bandwidth to the total power of the carrier across the same bandwidth. From Figure 2.24, the +885 kHz ACPR result would be C dBc (relative to A). Several signal analyzers today offer an automatic method for measuring ACPR, and for this scope we have used an Agilent 8560E Spectrum Analyzer coupled with a microwave signal generator.

The ACPR performance of the s-band VGA amplifier was evaluated using a QPSK digitally modulated signal at 1.95 GHz with 1.23MHz bandwidth. Figure 2.25 shows the output power and ACPR at 885 KHz and 1.98 MHz at maximum gain as a function

of the input power. The measured level of ACPR at 885KHz is better than –45dBc and at 1.98MHz is better than –70dBc at an output power up to +10dBm, meeting with margin the standard specifications.

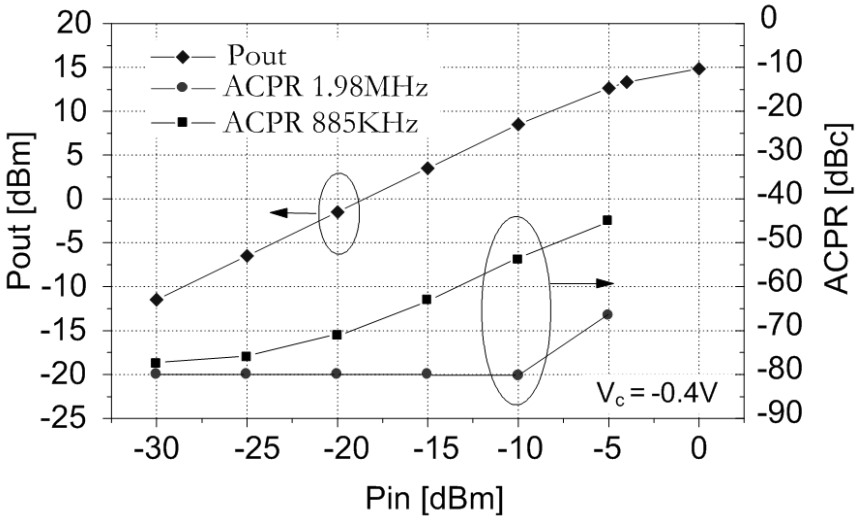

Figure 2.25: Output power, ACPR at 885KHz and at 1.98MHz offset from the 1.95GHz carrier as a function of the input power (V_c = -0.4V).

Figure 2.26 illustrates the ACPR characteristics of 885 KHz and 1.98 MHz offset from the carrier as a function of V_c with –10dBm input power.

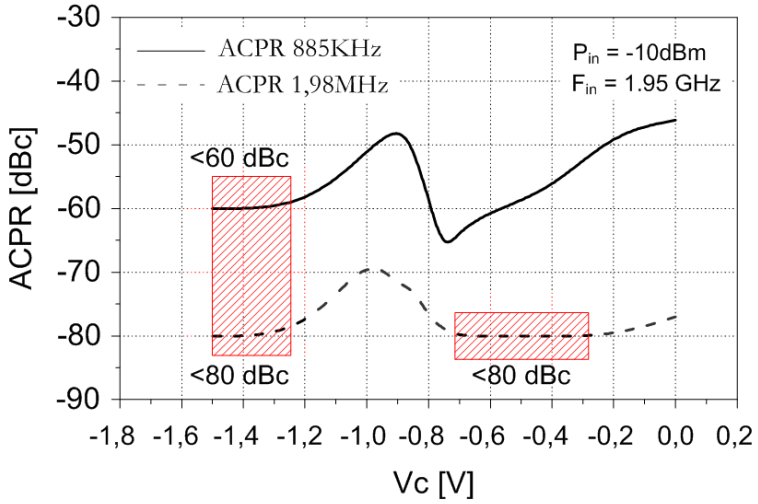

Figure 2.26: ACPR characteristic of the VGA at 885 KHz and at 1.98MHz offset from the 1.95GHz carrier as a function of the control voltage

Shaded regions indicate that the measure reached the minimum sensitivity of the spectrum analyzer (note that the values are expressed in dBc relative to the carrier

amplitude, so in lower gain conditions the signal amplitude is very small). Reasonably, the real value should be lower. Even if in the intermediate V_C range, where the transition of the series switch through the pinch-off region causes an increase in the ACPR value due to the strong non-linearity of the device (as was in the case of the power compression measurements) the ACPR level is always lower than –48dBc which greatly exceeds the linearity requirement of WCDMA (-35dBc). At maximum gain (V_C = -0.4V) the output power is +8.5dBm, power gain 18.5dB, 885-KHz offset ACPR is –55dBc and 1.98-MHz offset ACPR is better than –80dBc. With these performances the amplifier could be used to directly drive the power amplifier in a WCDMA system.

A summary of the measured performance is presented in table 2.2. These results, if compared with previously designed VGAs ([2.4], [2.6], [2.7], [2.11]) demonstrate the effectiveness of the proposed gain control technique.

Table 2.2*: Summary of the measured performance*

Id	Characteristic	Value			Units	Conditions
		Min.	Typ.	Max.		
V_{cc}	Power Supply		3.5		V	
I_d	Current			34	mA	
F_o	Center Freq.		2		GHz	
BW	BandWidth	1800		2200	MHz	
$RL_{in/out}$	return loss	-14			dB	@all gain
ISOL	Isolation	40			dB	
G_{max}	Max. Power gain	18			dB	@$V_{ACG(L)}$
G_{flat}	Gain flatness			1.5	dB	in BW
G_{slope}	Gain slope		0.01		dB/MHz	in BW
NF	Noise Figure			6.5	dB	
GCR	AGC Dynamic Range			40	dB	$V_{ACG(H)}$ to $V_{ACG(L)}$
OIP_3	Output intercept point	20			dBm	@maxgain
OP_{1dB}	Output 1dB Compression		12		dBm	@maxgain
IP_{1dB}	Input 1dB Compression	-5			dBm	@ all gain
$ACPR_{885}$	Adj. Channel Power ratio	-55			dBc	@885KHz offset
$ACPR_{1.98}$	Adj. Channel Power ratio	-80			dBc	@1.98MHz offset

2.7 FINAL IMPLEMENTATION

Once confirmed through measurement the proper behavior of the first prototype and the reliability of the models (this was the first design carried out by the department at these frequencies with this technology), next step was the implementation of the final circuit. A slight modification in the specification which was requested by the customer due to a change in the transceiver frequency planning forced to shift the center frequency from 2.0 to 2.2GHz. However, the full set of simulations carried out on the updated circuit is not reported as the behavior of the circuit was substantially the same as the previous implementation.

The circuit topology was maintained and the only significant changes were related to the overall layout (Figure 2.27) and the values of the input and output networks to compensate for the effects of the package selected for MMIC assembly (Detailed procedures followed for the characterization of the package will be described in chapter 5). Additional Electrostatic Discharge (ESD) protection resistors have been placed between all the DC and control pins to minimize circuit stress during manipulation and assembly.

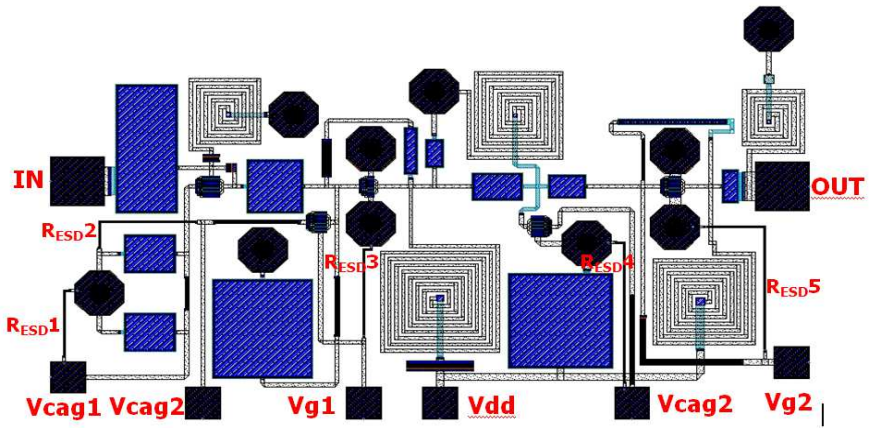

Figure 2.27: Layout of the VGA

The values of the R_{ESD} resistor are in the order of 10 to 20 kOhms, mainly limited by the available space.

As the chip had to be fabricated within a Multi Project Wafer run (MPW), only predetermined chip sizes were available. For this reason the circuit was placed in the same 2mm x 2mm die (Figure 2.28). containing also a LNA (described later in chapter 5) to be used together with the VGA in the receive chain of the S-band transponder. A

Process Control Monitor (PCM) transistor was placed within the two chips. The size of the transistor was selected as the average size of all the devices used in both the circuits. The aim of the PCM FET is for direct wafer probing at the foundry to control the value of all the significant fabrication process parameters within each individual chip allowing discarding non-compliant chips following the restrictions set by the yield analysis described hereafter.

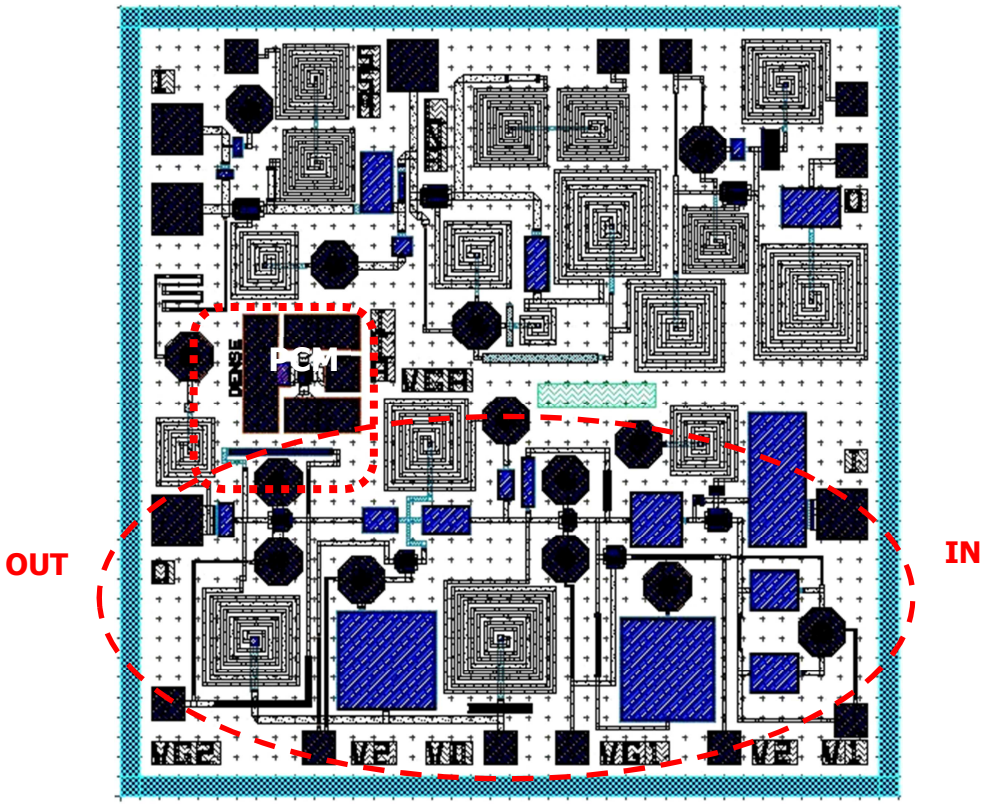

Figure 2.28: Layout of the chip including the designed VGA (mirrored) and a LNA amplifier

Yield analysis based on Montecarlo simulations were performed at the worst case temperature of 70 º C by varying all the process parameters with distributions functions provided by the foundry **t**o check circuit performance compliance with the specification.

Following the results of the yield simulations, for each sample not meeting one or more requirement the corresponding value of the fabrication process parameter were analysed and a set of non-compliance criteria (interval value) established. Once the validity intervals for the fabrication parameters were known, the direct on-wafer measurement of the PCM transistor at the foundry, would allow discarding all eventually no- compliant chips.

In the figures below, the yield results are plotted for some significant parameters.

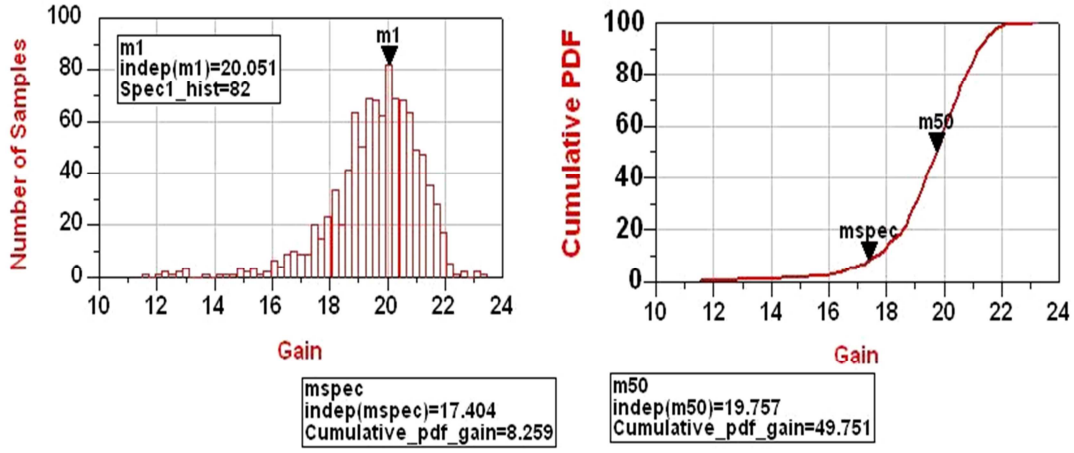

Figure 2.29: Number of Samples vs. Gain and Cumulative PDF of the Gain. Freq∈ [2.0, 2.4] GHz, Number of Samples=201.

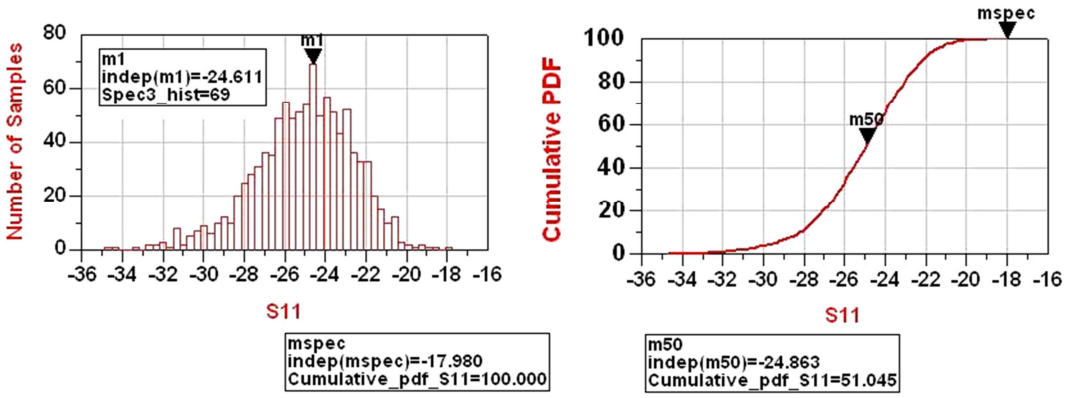

Figure 2.30: *Number of Samples vs. Input Match at max. Gain and Cumulative PDF of the Input Match. Freq∈ [2.0, 2.4] GHz, Number of Samples=201.*

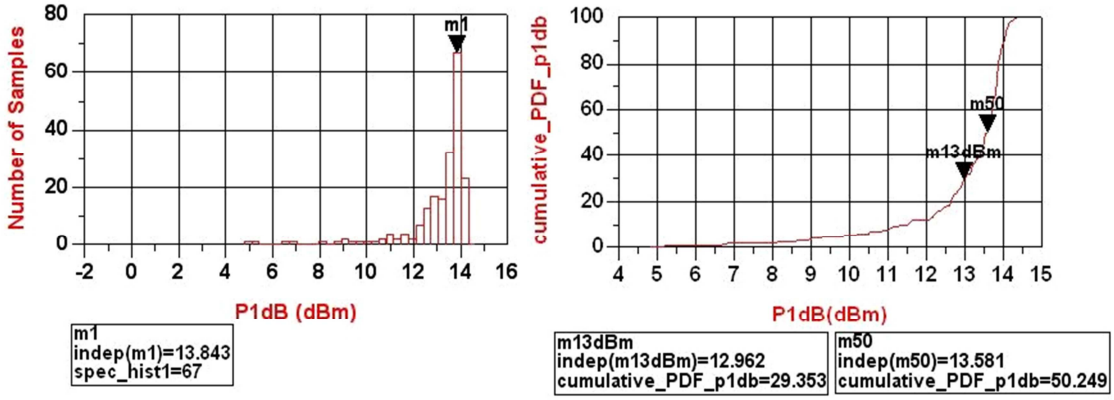

Figure 2.31: Number of Samples vs. Output Compression Power (1dB) and Cumulative PDF of the Output Compression Power. Fin=2.2 GHz, Number of Samples=201.

The graphs illustrate the histogram of samples (y-axis) versus the selected parameter value (Yield Specification, x-axis) and the cumulative PDF (Probability Distribution Function) as a function of the same parameter.

The cumulative PDF describes the probability that the selected parameter value (e.g. VGA gain) presents a value lower or equal to the specified.

It is important to underline that the results should be considered as an estimation because the correct yield can be obtained only with an infinite number of trials. Limitations to the number of trials have to be associated to CPU memory and convergence time of the simulator at the time of performing the simulations.

A measure of the precision of the approximation of the results is given by the confidence level (CL), which is defined as the area under the normal curve within a given number of standard deviations. For C_σ (number of standard deviations) =1 the CL is 68.3%, C_σ=2 the CL is 95.4% and for C_σ=3 the CL is 99.7%. For an estimation of the accuracy of the simulation the following expression can be used:

$$N = \left(\frac{C_\sigma}{\varepsilon} \right)^2 Y(1-Y) \tag{2.9}$$

where N is the number of trials, ε is the error in the estimation, and Y is the yield. So, referring for example to Figure 2.29 we have N=201, Y (Probability of Yield Specification> Nominal Specification, obtained analyzing the result of the simulations) =0.917 (91.7% as can be extracted by the cumulative PDF value). If C_σ=2 we obtain: ε=0.039. This means that with this number of trials we have the 95.4% probability (confidence) that the real yield is in the interval 91.7% ± 3.9%.

A summary of the yield results and the associated CL is reported in table 2.3. The mean value which appears is estimated considering the results obtained by 50% of the trials (samples) in the Cumulative PDF.

Table 2.3 *Summary of yield simulations*

Parameter (Yield Spec.)	Yield	Nom. Spec. (dB)	Mean value (dB)	Error +/- %	
				CL=95.4%	CL=99.7%
Max. Gain	91.7%	17	19.7	3.9	5.84
S11@ Max. Gain.	100%	-15	-24.8	0	0
P1dB@ Max. Gain.	94.5%	10	13.5	3.25	4.82

Once checked that the probability of proper behaviour of the circuit was ensured in more than 70% of the samples (for the worst case scenario), the new version of the S-band MMIC VGA was fabricated (Figure 2.32) to fit in a layout area of 1x2mm for integration into a single chip with a LNA (chapter 5)

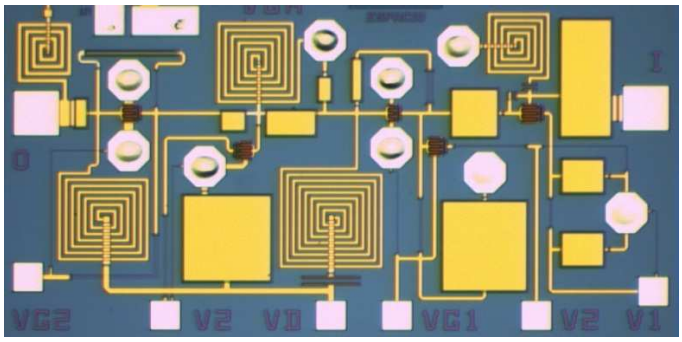

Figure 2.32: Microphotograph of the final circuit. Layout area is 0.95 mm x 1.9 mm.

All the measurements were carried with the assembly shown in Figure 2.33.

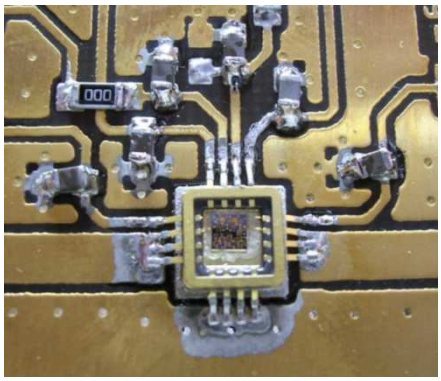

Figure 2.33: S-band MMIC VGA assembly on FR4 PCB

The chip was mounted in a 16 pin gull-wing package. An FR4 Printed Circuit Board (PCB) with 50 Ohm input/output connector is used for ease of testing.

Figures 2.34 and 2.35 illustrate s-parameter measurements of the packaged VGA between maximum and minimum gain. As can be noticed both the gain control range and the input match performance are substantially the same as in the previous case, showing how the proposed methods leads to consistent results and that the package modeling (described in chapter 5) worked properly.

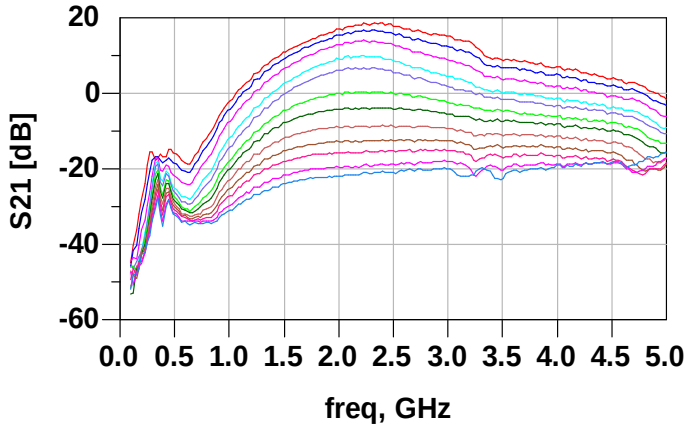

Figure 2.34: Packaged VGA Gain variation as a function of the Control voltage V_c.

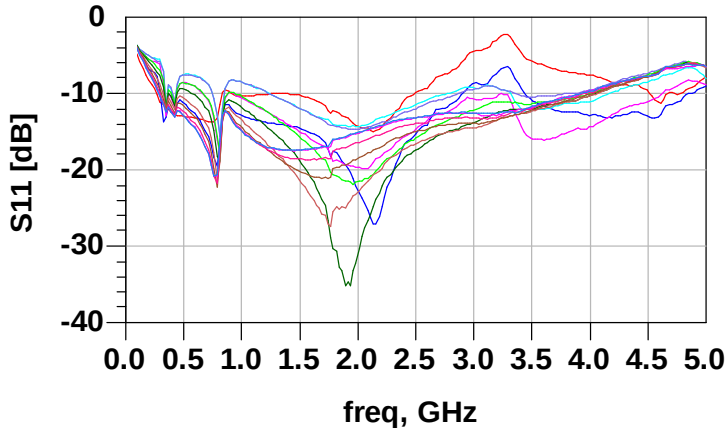

Figure 2.35: Packaged VGA input match variation as a function of the Control voltage V_c.

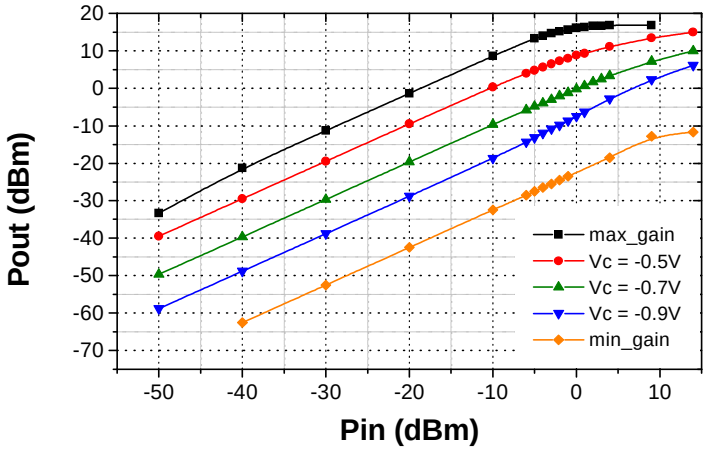

Figure 2.36: Output 1-dB compression at different control voltages (Vc=V1).

Figures 2.36 and 2.37 summarize the output power measurements. It can be noticed how the input P1dB degradation which was present in the previous prototype for values

close to the pinch-off is minimized. This is due to an optimization of transistor/resistor pair in the input switch to cmopensate the effect of non-linearities.

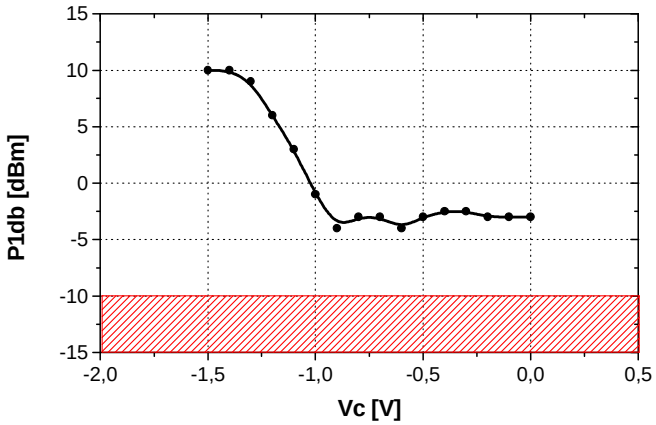

Figure 2.37: Input 1-dB compression as a function of the control voltage

Overall, the measured circuit performance were substantially the same as the first prototype, and has been omitted for simplicity. The main difference associated with the shift of the center frequency from 2GHz to 2.2GHz. The presence of the package, the non-perfect ground contact associated to the bonding of the MMIC to the package and the steep transitions associated to the PCB assembly contribute to the partial degradation of the out of band response as seen in figures 2.34 and 2.35.

2.8 CONCLUSIONS

A method to design compact linear-in-dB VGAs with good input/output matching and power handling capability has been presented. A wide dynamic range of 40dB with a deviation from linearity of only ±1.5dB is obtained. Input and output match remain always better than 14dB with an output compression power of 12dBm.

The method has been validated with the design of a GaAs fully monolithic amplifier. Several circuits have been tested and excellent agreement between the measured and predicted results has been achieved.

ACPR was also measured at the 1.95GHz WCDMA band showing values of -55dBc at 885-KHz offset and better than –80dBc at 1.98-MHz offset with an output power of +8.5dBm. With these characteristics it has been demonstrated that the method is suitable to implement the power control feature of VGA which could be used to directly drive the power stage in WCDMA systems.

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3 . E/D pHEMT multi-frequency generator MMIC

3.1 INTRODUCTION

Evolution of technology pushes toward bringing down the size and manufacturing cost of any kind of electronic equipments. In this context, the improvement of MMIC technology has drastically changed the design of such equipments. This is especially true for satellites and space modules asking for complex transmit/receive circuits with very stringent requirements. The use of MMIC circuits allowed an incredible reduction in mass and cost from the previous generation of circuits employing discrete IC, not only keeping but also increasing the reliability and performance of equipments.

Integrated transceiver subsystems using MMIC chips are being used for satellite communication applications. In some cases the multiple MMIC chip assembly solution may result in greater manufacturing and tuning time, resulting in higher cost. Current MMIC technology offers solution to this problem allowing the integration of many functions on a single chip (up to the complete integration of a System-on-Chip, SoC) without a big impact on yield and performance (especially with the increased miniaturization of the technologies), minimizing the number of chips and resulting in a lower test and module assembly cost. However the number of circuits and the area of the chip must be carefully chosen to optimise heat dissipation and minimize the effect of wafer variability, which can degrade the yield of the process and cancel the advantages of size reduction and assembly costs savings.

The scope of the work described in this chapter was the design, implementation and measurement of a multi-function MMIC to be used as one of the building blocks for a

new generation of Telemetry, Tracking and Control (TT&C) satellite transponder (details on the scope of the application and the final result of the work will be presented in chapter 5). The design which will be presented in this section was carried out with two goals in mind. First of all to test circuits' topologies and performance achievable with the selected technology as this represented the first design/implementation iteration with a technology which we never had used at these frequencies. Secondly to allow the evaluation of the suitability of the developed solution to match with the flexibility required by the overall system design while at the same time maintaining high fabrication yield despite fabrication variability across the wafer.

Commercially available MMICs for space born application (especially if we refer to multifunction or SoC solutions) are really limited (given the limited marketability) and in most cases solutions are developed on a "case by case" basis to adapt with each specific space mission requirement. Given the specific requirement associated to the new S-band transponder to replace previous generation with a higher flexibility (to enable the use in multiple missions) as well as reduced mass, cost and power consumption, a completely custom design was required.

The developed MMIC was targeting the coherent generation of multiple frequencies needed for the implementation of specific radio frequency functions (direct QPSK modulation, phase modulation, TT&C reception, and so on) in a transmit and receive (T/R) modules of satellite systems. In addition to a Voltage Controlled Oscillator (VCO), a frequency tripler and other analogue functions (mainly amplification), a digital divider has been inserted to allow the use of this mixed analogue/digital chip in PLL systems. Main focus will be given to the divide-by-four circuit as the detailed design of the VCO has been object of a separate work [3.8], and the frequency multiplier did not supposed significant design effort.

3.2 TECHNOLOGY SELECTION

There are no technologies that suit the needs of all the modules which were to be developed in the frame of the project. MMIC design demanded many trade-offs in performance and many factors were to be considered when starting the design of the family of application-specific MMICs, including technology limitations due to space

mission requirements (e.g. radiation total dose, single event upset tolerance, and heavy ions sensitivity).

All the circuits were developed for on-board transponder applications in the frame of the Galileo program, the European Global Satellite Navigation (http://www.esa.int/esaNA/galileo.html). One of the most limiting factor is probably linked to the strict spatial requirements [3.1], [3.2]. Space radiation effects have to be considered when designing a circuit for aerospace systems. The Single Event Effects (SEE) associated with the transit of heavy ions through semiconductor junctions have to be minimized to reduce failure risk. Radiation effects from these particles can cause degradation, and also failures of the electronic and electrical systems in space vehicles or satellites. The most dangerous of this kind of effects is the Latch-up (SEL, [3.3]) which can lead to the destruction of the device and has to be completely avoided. In this sense GaAs devices, which are not prone to SEL, seemed to be the best choice. Moreover, gamma-ray robustness of p-HEMT MMICs has been investigated for space-borne applications [3.4], [3.5] showing that no degradation of RF performance was observed up to 10^7 rad-dose, which suggests over 100 years of life with gamma-ray irradiation in the space environment.

Another aspect considered was the fact that the circuits were part of a broader set of functions including also Low Noise and power amplification, hence compatibility with LNA and MPA design would have to be ensured in order to avoid the use of different technologies. The family of MMICs also includes digital circuitry, so a process with complementary logic, i.e. with both normally-On and normally-Off transistors, is preferable.

Finally, the selected process should include measurement-based accurate models for active and passive circuit elements, along with layout libraries and thermal, reliability and process variation parameters, all of them in a format compatible for use with standard circuit simulators. Space evaluation/qualification of the process is a must in this case.

After a careful evaluation, the chosen process was a commercial foundry process from OMMIC in France (ED02AH), developed specifically for low noise applications up to 60GHz but capable of providing good output power level and normally on and normally off devices. The technology was already used by our research group at the

University of Cantabria in the frame of other space related developments, albeit at much higher frequencies[2], but the familiarity with the technology and the models, allowed a quick check of the attainable performance and provided reasonable confidence on the capability to meet almost all the design requirements.

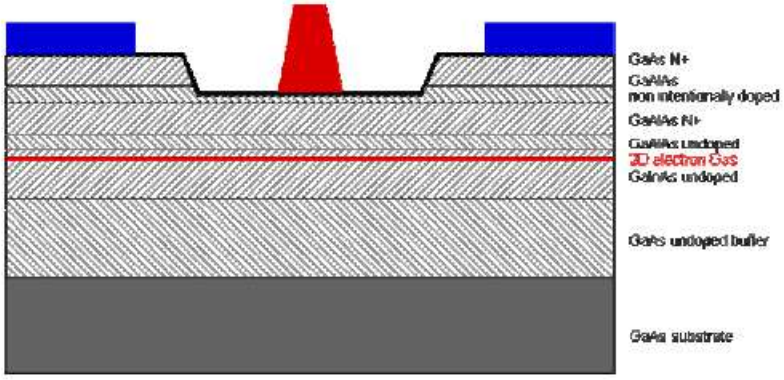

Figure 3.1: Cross section of a p-HEMT transistor from OMMIC

The ED02AH process features an active pseudomorphic GaInAs layer grown by Hetero-Epitaxy and the p-HEMT transistors (Figure 3.1) have a gate length of 0.18µm with an f_T=60GHz. A significant Indium concentration ensure better electron mobility, higher cut-off frequency and lower operating voltages. Two types of transistors are available: depletion (D) and enhancement (E), featuring nominal pinch-off voltage (V_t) of -0,9V and +0.225V respectively. D-mode transistor operate with negative gate control voltages whereas E-mode with positive one hence providing a lower dynamic range. A higher dynamic option for E-mode is also available with a V_t = +0.1V.

Combining enhancement and depletion mode devices, the process is suitable for the implementation of both digital and analogue functions. The ED02AH process is today (at the time of the design of the circuit the process was ongoing) one of the European Space Agency (ESA) European preferred part list (EPPL) technologies. Some successful results from this process have already been reported ([3.6], [3.7]).

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3.3 MMIC SPECIFICATIONS

A block diagram of the specified MMIC is showed in Figure 3.2. The selection of the three main functions (oscillation, frequency multiplication by 3 and division by 4) was motivated by the use for which the chip was developed: the generation of all the system frequencies used in a TT&C T/R module at S-band and the frequency planning of the module itself.

A *quasi-MMIC* VCO approach (i.e. the resonator placed outside the MMIC) was imposed instead of a fully integrated solution to enhance the flexibility (with respect to the limited capabilities which can be granted by a fully integrated solution) to support the use in multiple space mission. The tank resonant circuit outside the chip gives a degree of freedom (and even better performance) which is not possible if varactor and/or resonator were included on chip (and this is independent from the technology selection).

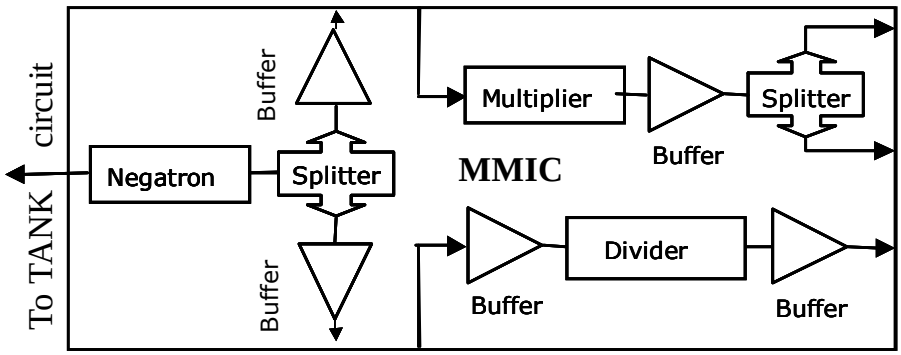

Figure 3.2: Block diagram of the frequency generator MMIC

As can be noted, each of the elementary functions presents two or more input/output terminals to access the circuit from the outside. A solution which was adopted to facilitate the first on wafer testing and allowing different system configurations through appropriate connections.

Two possible configurations of use, in transmission and reception mode, are illustrated in figures 3.3 and 3.4. Additional RF and digital functionalities, sketched as separate circuits in the figures, have not been integrated in the same chip to make possible the sharing the same MMIC in both types of modules (T/R), and to reduce the chip size to trade off fabrication yield.

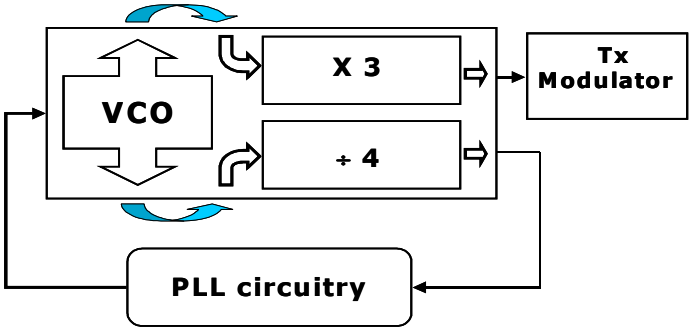

Figure 3.3 : Multi-frequency chip use in a transmit module

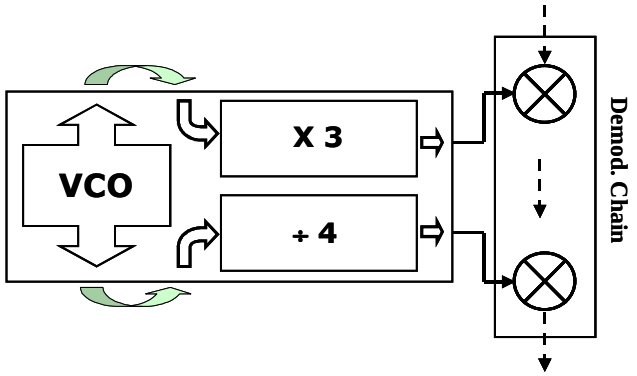

Figure 3.4 : Multi-frequency chip use in a receive module

In order to meet overall system specifications, individual sub-circuits requirements were fixed as it is detailed in Tables 3.1 to 3.3.

Table 3.1*: Frequency Multiplier design specifications*

Id	Characteristic	Value			Units	Conditions
		Min.	Typ.	Max.		
P_d	Dissipater power		15		mW	
F	Bandwidh	660		780	MHz	
M	Multiplying factor		3			
P_{in}	Input power		5		dBm	
P_{out}	Output Power		5		dBm	@50 Ω
Z	Input/output impedance		50		Ω	
Harm	Harmonic suppression	40			dBc	
Spur	Spurious tones	90			dBc	Not Harmonic
T	Temperature	-30	25	70	°C	

Table 3.2*: VCO design specifications*

Id	Characteristic	Value			Units	Conditions
		Min.	Typ.	Max.		
P_d	Dissipater power		15		mw	
F	Bandwidh	660		780	MHz	Negative Resistance
F_{pull}	Frequency pulling		0.2		%	Load VSWR = 2
F_{push}	Frequency pushing		0.01		%	@V_{cc} ±5%
P_{out}	Output power		5		dBm	Both outputs
Z_{in}	Input impedance		50		Ω	
ISOL	Isolation		90		dB	Buffer/ Splitter
N_{flkr}	Flicker Noise	17			dB	@$V_{ACG(L)}$
PhN	Phase Noise					Depending on the external resonator
T	Temperature	-30	25	70	ºC	

Table 3.3*: Frequency divider design specifications*

Id	Characteristic	Value			Units	Conditions
		Min.	Typ.	Max.		
P_d	Dissipater power		35		mW	
F	Bandwidh	500		2800	MHz	
D	Division Ration		4			
P_{in}	Input power		-5		dBm	Sensitivity
P_{out}	Output Power		-5		dBm	@50 Ω
Z	Output impedance		50		Ω	
SEL	Latch-up		immune			
SEU	Single Event Upset			10^{-9}		Errors per bit/day
T	Temperature	-30	25	70	ºC	

3.4 CIRCUITS IMPLEMENTATION AND CHARACTERIZATION

The prototype multifunction chip which has been fabricated is shown in Figure 3.5.

Layout area of 4x5mm^2 includes coplanar test points and multiple DC-bias pins to allow individual and collective characterisation of the functions and independent bias pads to adjust DC power consumption, check performance in non-nominal conditions and test multiple connection configurations.

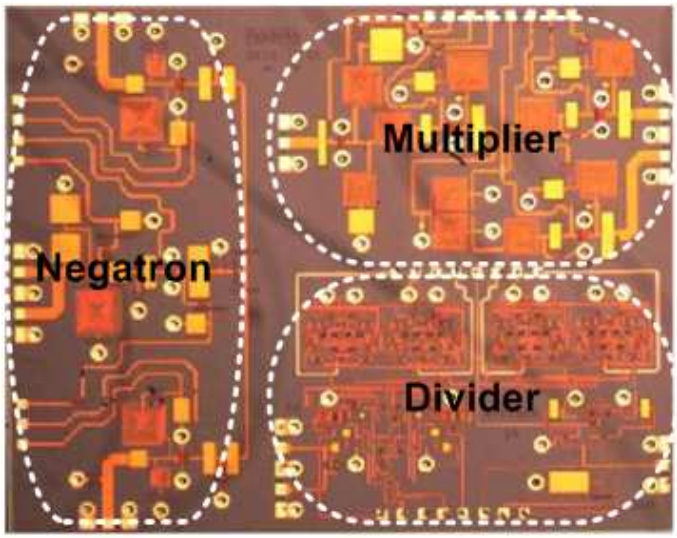

Figure 3.5: Microphotograph of the multifunction MMIC

Following sections will detail the main implementation features of the circuits together with a summary of the measured performances. However, relevance will be given mostly to the design and implementation of the divider circuit as the other circuits were object of a parallel research.

3.4.1 **Voltage Controlled Oscillator**

The VCO consists basically of an external tank circuit (resonator and varactor) an integrated negatron (Figure 3.6). This solution was selected because the use of a high quality external resonator and varactor, provides a high degree of versatility for the operating frequency range and higher quality of performance, compared with the attainable with integrated resonators.

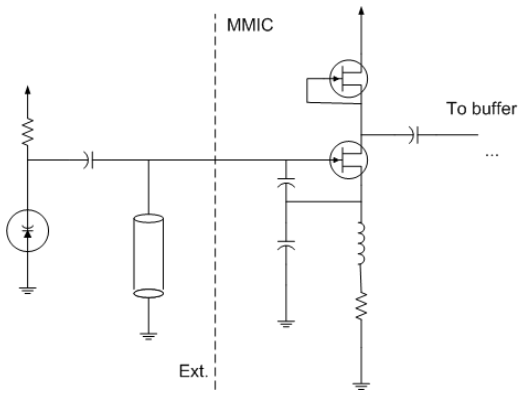

Figure 3.6: Topology of the oscillator (negatron plus resonator).

The negatron uses a transistor with the source capacitively coupled to ground. To simplify the biasing scheme the active device is self-biased. The output is taken from the drain and the varactor tank circuit is connected to the gate of the transistor. This solution achieves better isolation between the output and the resonant circuit and requires a single pin for the connection with the resonator.

As can be noticed in Figure 3.5 (left side of the ASIC), for this first implementation a double input pin has been placed to facilitate tests with different type of resonators (i.e. varactors, inductors, and coaxial resonators).

The buffer (a common-source amplifying stage with active bias) was designed to increase isolation (more than 40dB) in order to avoid dependence of the VCO frequency from the load (frequency pulling). As a double output is required to feed both, a frequency multiplier and a frequency divider (Figure 3.2) a power splitter plus two buffers were added. The former consists of a resistive splitter occupying minimum area, and the output buffers were designed to provide additional isolation and proper power interfacing with 50Ω system.

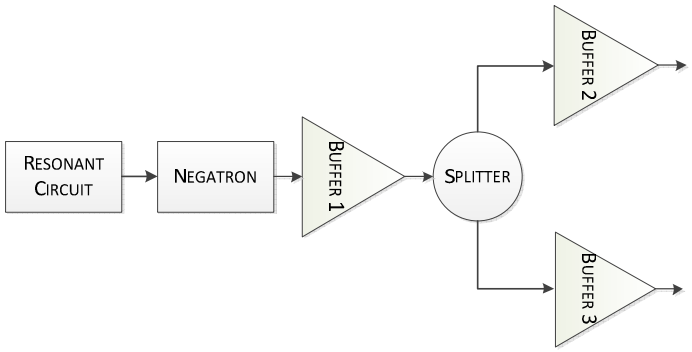

Figure 3.7: High level block diagram of the complete oscillator circuit

The MMIC negatron is capable to provide oscillation (i.e. negative resistance) in a band in excess of 1 GHz around 700 MHz, with an output power around 5dBm independent from the used resonator and with a sensibility from supply voltage (pushing) less than 0.07%. The circuit draws 47mA from a 3.5V supply voltage. Details of the design technique used for the VCO are outside the scope of the present work and can be found in [3.8]. Figure 3.8 reports the measured performance (oscillation frequency and output power) as a function of the control voltage in two different cases in which a simple surface mount inductor was used as low-Q resonator.

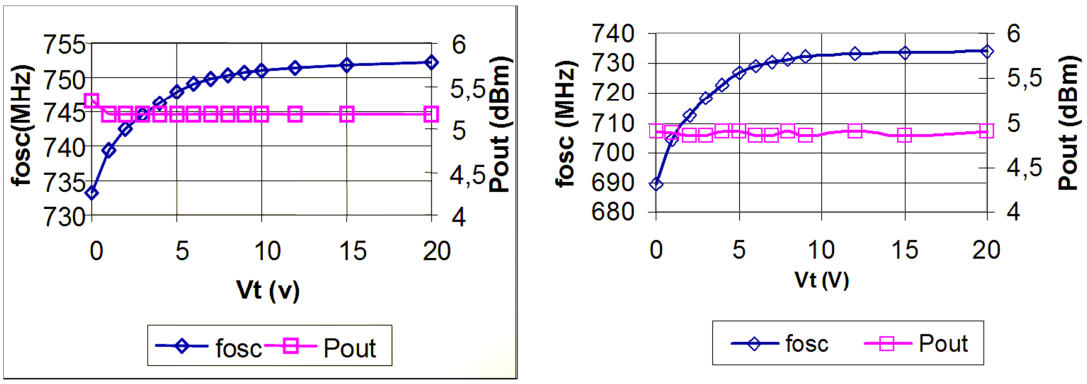

Figure 3.8: Oscillation frequency and Output power as a function of the varactor control voltage with two different low-Q resonators.

Different values and configurations for the tank circuit were tested to demonstrate the capability of oscillation of the VCO in the entire BW in which the negatron shows negative resistance.

An oscillating BW of 19MHz around 740MHz with an output power of more than 5dBm at each output was obtained with a 2.7nH inductor (left). The measured phase noise was –99dBc/Hz at 100Khz offset from the carrier with the control voltage set to 0V. In the second case we used a 2.2nH inductor with a lower Q factor and a different tank circuit to obtain a greater oscillating BW of 44MHz @710MHz and an output power slightly lower than 5dBm. The measured phase noise was in this case –95dbc/Hz @100KHz offset.

To improve phase noise performance a high-Q coaxial resonator was tested at Alcatel space laboratories. Results at three different operating temperatures are shown in Figure 3.9.

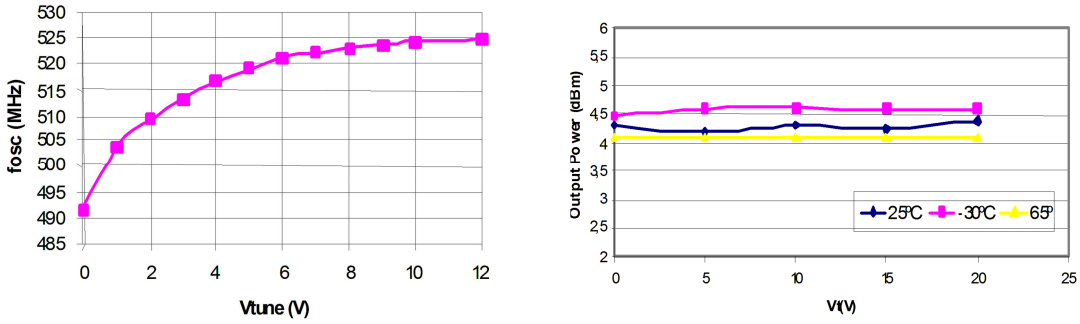

Figure 3.9: Oscillation frequency (left) and Output power (right) as a function of the varactor control voltage with a high-Q coaxial resonator.

In this case the achieved frequency bandwidth was 34MHz with a variation with the temperature (not reported in the graph) around 4Mhz. The output power is slightly lower than the previous cases, but always greater than 4 dBm with little variation with the temperature. This is a fact that can be associated to the dispersion of the process parameters across the wafer.

In Figure 3.10 and 3.11 are shown the measured phase noise performance at 491 MHz and 1GHz of –106.6dBc/Hz@100KHz and -116.8dBc/Hz@100KHz respectively. These values are similar to the values obtained with Si-MMIC using the same resonator configuration [3.9], and it is not far from the phase noise achieved with SiGE BiCMOS technology [3.10] despite the much better corner frequency performance of the latter technology with respect to GaAs.

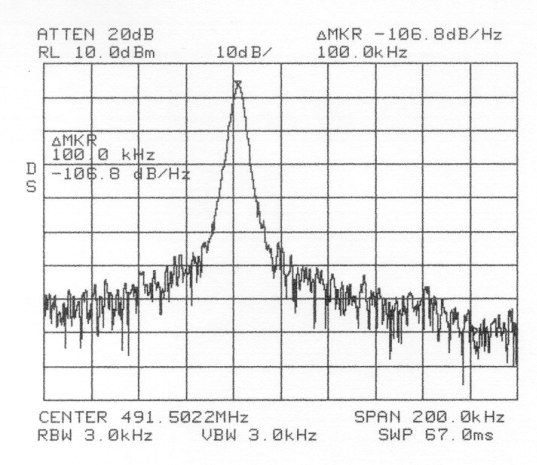

Figure 3.10: Measured spectrum of the free running VCO (F_{osc}=491MHz) at a tuning voltage of 0V. Phase noise is approximately –107 dBc/Hz @100KHz.

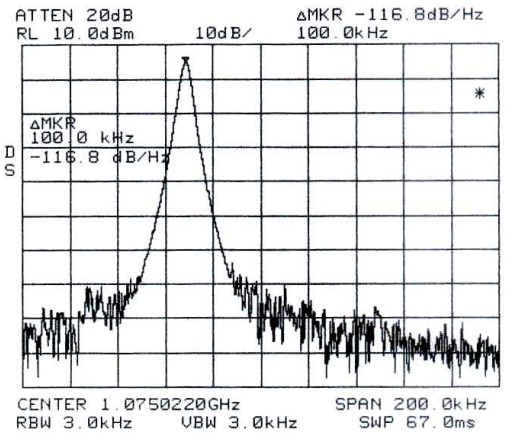

Figure 3.11: Measured spectrum of the free running VCO (F_{osc}=1GHz) at a tuning voltage of 0V. Phase noise is approximately –117 dBc/Hz @100KHz

3.4.2 **Frequency Multiplier**

The frequency multiplier consists of a frequency tripler [3.11], a buffer, a power splitter and two output buffers (Figure 3.12). The tripler is basically a pHEMT that works as a harmonic generator. Its biasing point was optimized to obtain the maximum third harmonic power. This block also includes resonant circuits to attenuate the first and second harmonics. The first buffer ensures enough output power to drive the splitter. The latter is a lumped Wilkinson power divider designed to contribute also to the attenuation of the fourth and higher harmonics. Finally, the output buffers were designed to improve isolation and output matching over a wide bandwidth.

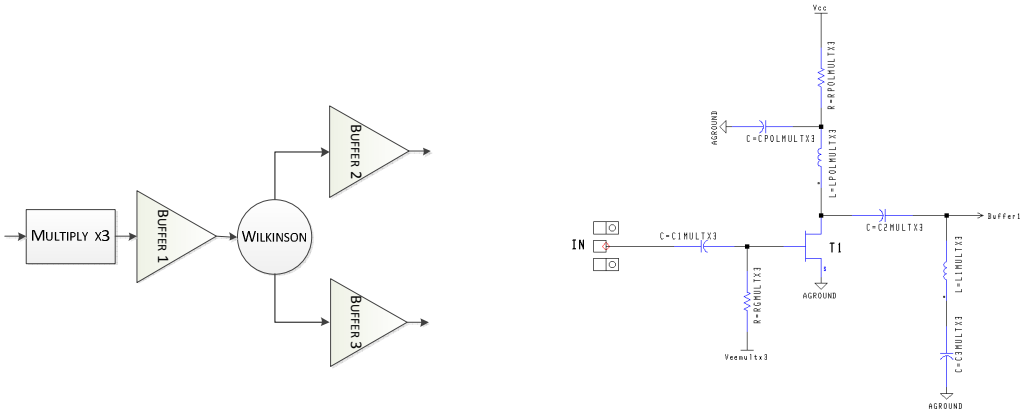

Figure 3.12: High level block diagram of the frequency multiplier (left) and schematic of the multiplier-by-3 (right)

The measured output power is greater than 5dBm with more than 18% bandwidth around 710 MHz at an input power of 5dBm (Figure 3.13). Output match is better than 12dB when the input signal is applied, and power consumption is 38.5mA@3.5V.

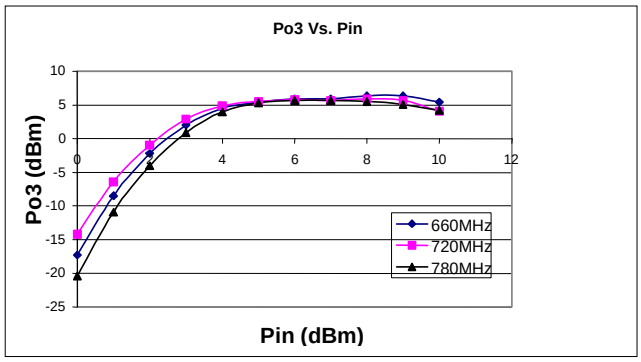

Figure 3.13: Multiplier Output vs. Input Power within the operating bandwidth

Fundamental frequency is around 28dB and 2nd harmonic 22dB below the desired signal right at the output of the MMIC (Figure 3.14). The level of other higher frequency unwanted harmonics can be further decreased with external passive filtering. DC bias requirements at the maximum output power are +3.5V and 38.5mA. Bias of the output buffers can be adjusted to trade-off harmonic contents at the output and DC power consumption.

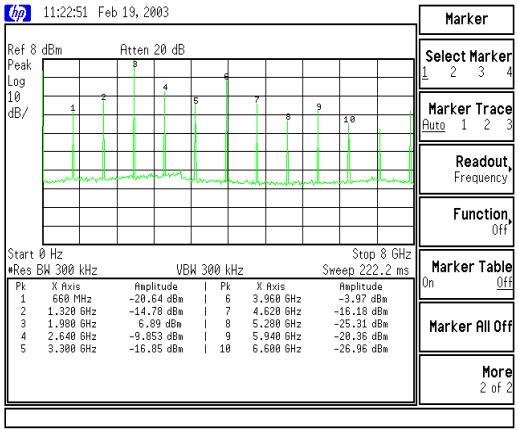

Figure 3.14: Measured output spectrum of the multiplier (Fin= 660 MHz)

3.4.3 **Frequency Divider**

3.4.3.1 **OVERVIEW**

Frequency dividers IC are essential building blocks in today's frequency synthesizers and PLLs for a wide range of applications. There has been a number of different microwave frequency divider concepts described in the literature. Each of these individual concepts may be categorized into two basic categories: analogue and digital.

Main difference between the two types of circuits is that analog dividers rely on non-linear properties of the active device while digital ones operates substantially like digital counters (even if its behavior could be analyzed also from an analogue point of view as will be further described in chapter 4).

Analogue dividers feature lower power consumption, simpler circuit designs (they generally exploit a single non-linearity) and higher operating frequencies, which makes them attractive for communications purposes. Among analog divider we can distinguish between: injection-locked (a free-running oscillator synchronized with a specific

harmonic), parametric (in which a sub-harmonic oscillation is generated from a nonlinear element, e.g. a varactor), or regenerative (mixing the input signal with the feedback signal from a mixer). In all the cases, the division mechanism is associated to non-linear properties of the active device which are strongly variable with frequency and difficult to model properly. For these reasons, this kind of dividers are inherently quite narrow-band and present a frequency behavior which is quite difficult to predict accurately.

On the other hand, digital frequency dividers rely mainly on the on/off behavior of the active device, yield instantaneous frequency division of a given signal on a cycle-by-cycle basis, but require quite complex implementations and high number of transistors.

Attempts have been made to broaden the operating bandwidth of analogue frequency dividers ([3.12], [3.13]) but all these features can be better guaranteed by digital dividers for which the operating window can cover the range from DC to the maximum working frequency of the active device offering more flexibility and modularity than analogue dividers [3.14]. In addition, high speed quadrature clock signals are required in modern zero-IF and low-IF wireless receivers [3.15] and phase-shift-keying demodulators, feature which can be easily achieved with a digital divider [3.16] while requiring additional circuitry in analogue dividers.

Despite their complexity and lower speed, if compared with their analogue counterpart, digital frequency dividers are usually preferred in the implementation of frequency synthesizers because of the common requirements of commercial applications: robustness against process and temperature variations, and an operating window (i.e. bandwidth) wide enough to cover different applications without the need of redesigning the entire circuit for each application. All features which can be better guaranteed by a digital divider. All these reason make digital divider widely used in modern electronic systems. At the same time, and differently from the analogue case, its functioning principle is relatively independent from the accurate characterization of the non-linear devices, hence simplifying the design and the reliance on very accurate device modeling.

Within the digital domain, the design strategy can be further divided into two categories: static logic and dynamic logic. The static implementation is the most popular

approach and has been selected for the targeted divide-by-four implementation given its wide acceptance and demonstrated functionality. This type of circuit could in principle work from the maximum operating frequency of the active device down to DC. In the reality on implementations the upper limit is affected both by the technology and the topology chosen (in addition to the circuit load), while the lower limit is set by the input analogue circuitry (e.g. buffers).

3.4.3.2 CIRCUIT TOPOLOGY

After an initial study on the different digital divider topologies capable of meeting the design specification, the one selected for the implementation of the circuit is based on the master-slave D-Flip Flop (DFF) with two clock phases ([3.17], [3.18]).

It can be easily shown how a DFF with feedback from the inverted output allows multiplication by two of input signal period Let´s consider a positive edge-triggered DFF which initial state is set as D=NQ=1 and Q=0. When the clock changes its state, Q follows D and goes to 1. At the same time NQ goes to zero, and D (due to the feedback) follows NQ. At the next positive clock edge Q will go back to zero (as it is the value stored in D), hence NQ and D will become 1. It can be then easily observed in the logic diagram (Figure 3.15), that the result is the multiplication by two of the (input) clock signal period, hence the division by two of the input frequency.

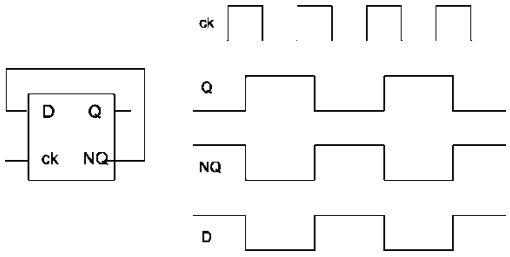

Figure 3.15: D-type Flip Flop with negative feedback to implement division by 2 and relative logic diagram

Cascading two master-slave DFF of this type will result in a division by four of the input signal frequency (Figure 3.16).

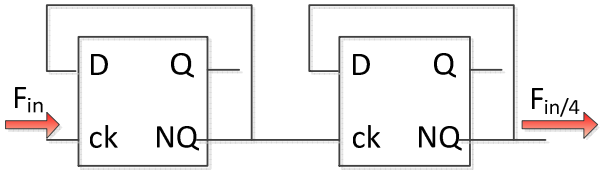

Figure 3.16: Block diagram of a static divide-by four

For the implementation of the basic DFF logic cell, SCFL topology was selected for its suitability to the application.

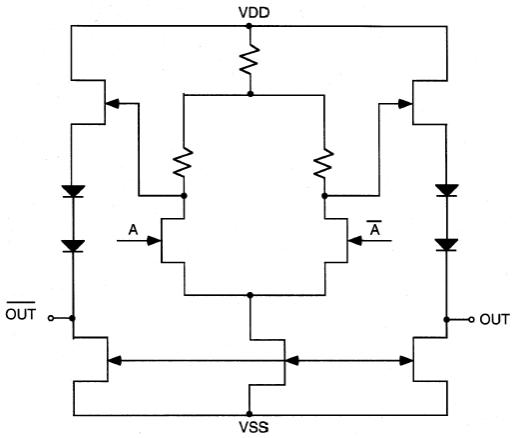

Figure 3.17 Generic diagram of SCFL inverter with source follower output buffering

Functioning principle of SCFL is based on differential amplifiers. An SCFL inverter (substantially a buffered differential amplifier) is shown in Figure 3.17. The high speed of this logic family derives from some properties which can be deduced from its circuital implementation: small input capacitance, fast discharging time of the differential stage output nodes, and good drive capability ensured by the source followers.

In addition to higher speed than Direct Coupled FET logic (DCFL) due to smaller input capacitance and fast discharging time at the output nodes, SCFL is characterized by high functional equivalence and reduced sensitivity to threshold voltage variations (and all other common mode variations as temperature and other process parameters) due to the fully differential structure (DCFL feature a quite low noise margin making it very sensitive to any kind of process variation). The current-mode approach used in SCFL ensures an almost constant current consumption from the power supplies and, therefore, the power supply noise is greatly reduced as compared to other logic families. The differential input signaling also improves the DC, AC, and transient characteristics of SCFL circuits.

A drawback of SCFL topology is the complex transistor gate topology (7 transistors are needed to implement an inverting gate), but this is counterweighted by

the fact that this family has a high functional equivalence, so that even complex functions can be implemented with a reduced number of cells.

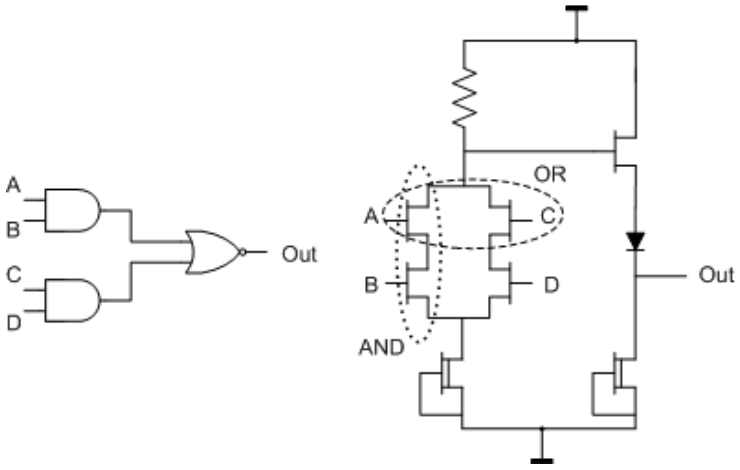

Figure 3.18: Logical equivalence of an AND-NOR gate with a two level SCFL cell.

A single two level series SCFL cell can be in fact used to easily build a DFF. The basic logic equivalences are shown in Figure 3.18. Two series transistors operates as an AND gate while two parallel transistors as an OR gate. Cascading these gates with a source follower, NAND and NOR functions are implemented.

The logic block diagram of a master-slave DFF is shown in Figure 3.19 [3.19]. It can be noticed how the clock controls both the data acquisition and the feedback from the inverted output.

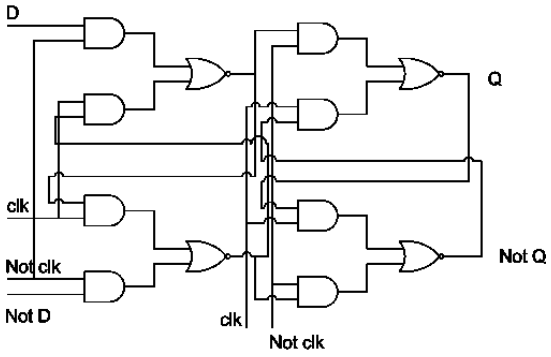

Figure 3.19: Logic diagram of the master-slave D-type FF with two clock phases

Given the differential structure of the SCFL cell, and the inverting characteristic, only two SCFL cells (two-level) are required to implement a complete DFF. Using

conventional DCFL logic, at least eight cells would have been needed to implement the same functionality.

3.4.3.3 CIRCUIT IMPLEMENTATION

Following the principles detailed in the previous section, a D-ff with feedback from the inverted output could be implemented through the circuit schematic shown in Figure 3.20 which features a two level series-gated circuit. Each of the AND-NOR blocks, is implemented with a differential cell with two series transistors. The inputs at the two levels require different DC-offsets in order for the circuit to work correctly; thus, level-shifting networks using diodes or source followers are needed. The source followers at the output of the SCFL cell are complemented with level-shifting diodes which are needed to allow a cascaded connection of multiple DFF. The current source was dimensioned to ensure the best common-mode suppression and, together with the load resistors, to set the output logic swing. In order to ensure an optimum behavior of the circuit [3.19], the transistors in the differential pairs should be kept in saturation all the time to maintain a low gate-drain capacitance.

Even if, in principle, a differential input is not strictly needed (as one of the inputs could be connected to a reference voltage), we chose to use a fully differential input to endure a better high frequency behavior.

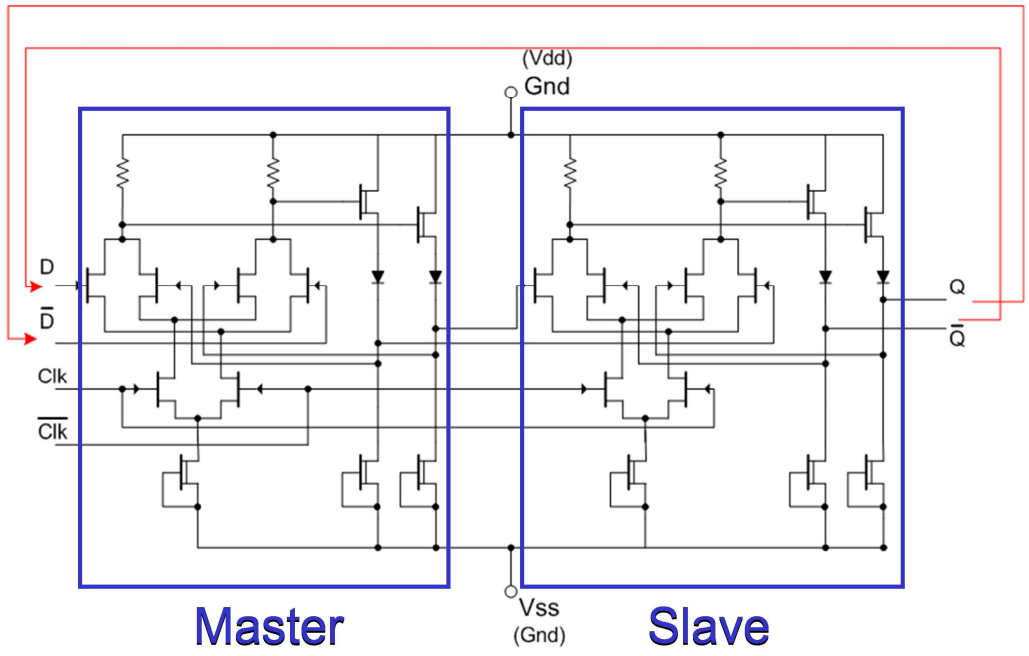

Figure 3.20: Schematic of the master-slave SCFL D-type FF

In additional to the core logic, the overall circuit is completed by an input and an output buffer to interface with the external circuitry (Figure 3.21).

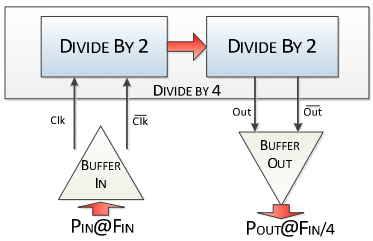

Figure 3.21: High level block diagram of the complete divider by four

3.4.3.3.1 Input Buffer

The following functions need to be performed by the buffer:

- DC decoupling of the logic core ;
- Interface with 50Ω (required by the characterization set-up and to allow multiple test configurations in the multifunction chip);
- Generation of two out-of-phase differential signals from a single-ended input;
- Level shifting of the input signal to level compatible with the logic cell.

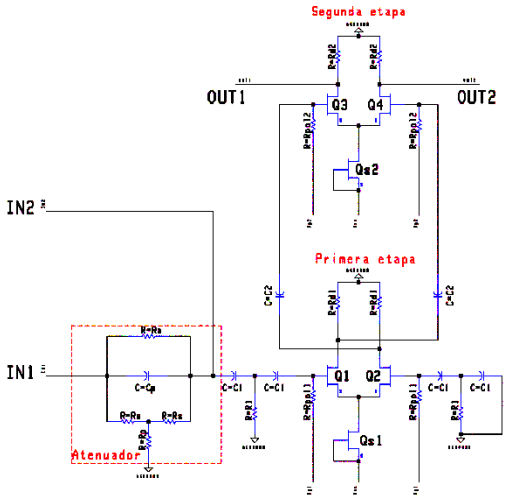

Figure 3.22: Schematic of the two-stage differential input buffer

To perform these functions two differential stages were cascaded (Figure 3.22) to ensure the generation of two complementary signals from a single phase input signal

with an accurate and constant 180º phase shift. An additional attenuated input was included on-chip to ensure proper behavior of the divider. This input will be used as the nominal one as the cascaded amplifier has an excess gain given the very good behavior of the GaAs transistors at the operating frequency. The non-attenuated input was kept as an additional option to be used in case the divider does not present the required sensitivity level (it has to be recalled that this represented the first design iteration). As an additional functionality, the input attenuator is also used to slightly equalize the gain of the differential amplifier across the full input signal bandwidth (500-4500MHz).

Level shifting to drive the cascade of the logic core is achieved inserting source follower stages directly coupled to the output of the second differential stage (Figure 3.23).

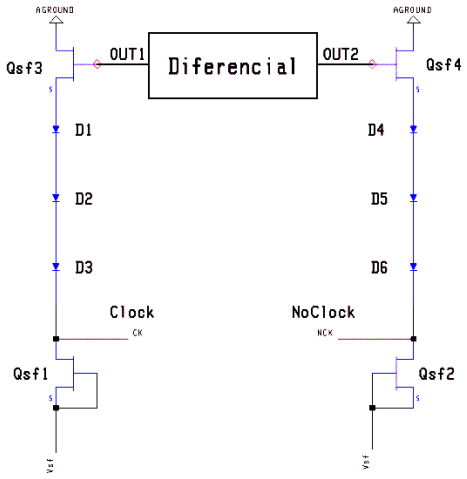

Figure 3.23: Input Source follower stages

3.4.3.3.2 Divider core

A detailed step by step procedure has been applied for the selection of transistor sizes and bias, to maximize efficiency, to keep HEMTs always in saturated region and to adjust delays during the high-low transitions at each one of the three different transistor levels present in the SCFL cell. DC inverting curve was obtained as a first approach. In a further step the dynamic inverting transfer characteristic was optimized taking into account the signals present at the other inputs. The resulting divider core (Figure 3.20) was implemented with normally off pHEMT (V_t>0) transistors with a gate width of 2x30µm. The current sources transistors providing the saturation current I_{dss}

(V_{gs}=0V) use normally on pHEMT (V_t<0) with a gate width of 2x10µm. The latter represent the minimum transistor size for which the foundry guarantees proper modeling, and it has been selected to minimize overall circuit consumption. The overall voltage swing higher than 5V ensures that transistors in all 3 logic levels operate always well above the saturation voltage (but with a heavy power consumption drawback) and the circuits provide enough output voltage swing. This choice was associated to the fact that the design was a first run, and enough safety margins had to be ensured. As the only available voltage (in the overall system specification) were +3.5V and -6.3V, this implied that the circuit was designed with V_{dd}=gnd, and V_{ss}=V_{Supply}. Simulated current consumption was in the order of 50mA@5V. Source followers used internally to the SCFL cell are depletion type with a gate width of 2x35µm.

3.4.3.3.3 Output Buffer

The following functions need to be performed by the buffer:

- DC decoupling of the logic core.
- Interface with 50Ω and isolation from the load.
- Amplification of the output voltage swing to the specified power level.

As the divider provides a DC-coupled differential output, an additional differential stage is needed to decouple the output, while a push-pull amplifier connected to the complementary outputs was used to provide broadband match and the requested output power (Figure 3.24).

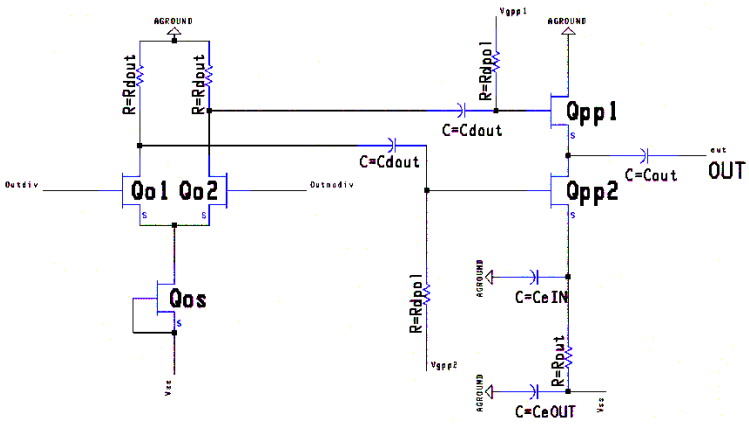

Figure 3.24: Output Buffer

3.4.3.4 LAYOUT

Figure 3.25 shows a micro-photograph of the complete divider. The two input pads are on the bottom left while the output is on the right. The two rows of pads on the top and bottom of the die are used as multiple supply voltage and bias pins. All the circuits' biasing networks have been separated in order to better control all sub-circuits and allow post fabrication tuning of the operating point. Due to the low frequency divided-by-four output, the output bypass capacitor required is quite big and it was kept off-chip to fit the layout area within the available space.

Interconnections between the two logic cells and internal feedbacks have been optimized to avoid phase shifts and maintain equilibrium among simultaneous paths.

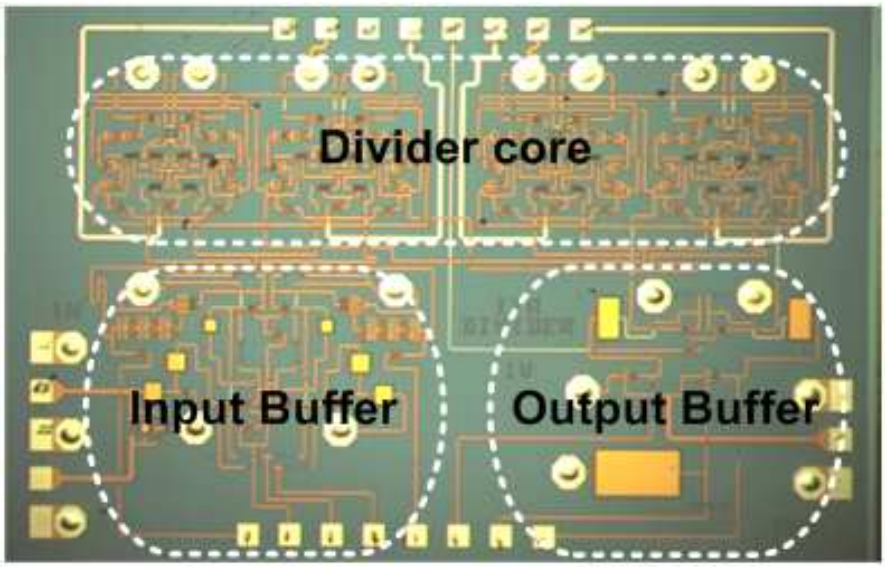

Figure 3.25: Detail of the divider by four

3.4.3.5 SIMULATIONS

The most relevant simulation related to the main divider specifications are detailed in this section for sake of completeness.

The results are relative to the overall circuit (D-FF plus buffers) with input/output loads set to 50Ω. The values have been obtained by means of transient simulations as at the time of developing the circuit and with the simulation techniques known by that time, the Harmonic Balance (HB) simulator showed convergence problems in the available workstations due to high number of non-linearities (around a hundred transistors) present in the circuit and to the fact that in case of divider circuit the

solution needs to be properly initialized. Even if transient simulations do not provide information on the steady state solution (as is the case of HB), by taking a sufficiently large transient time interval, we can assume that the solution is quite close to the steady-state.

Due to convergence problems also with DC simulation, static current consumption was evaluated by means of transient: the average RF power consumption in a sufficiently large interval (hundreds of cycles) after the initial transient behavior is stabilized was estimated. Overall current consumption was in the order of 75mA.

Input/output waveforms in a close to steady state solution and its relative output spectrums at different input frequencies are shown in Figure 3.26 and Figure 3.27.

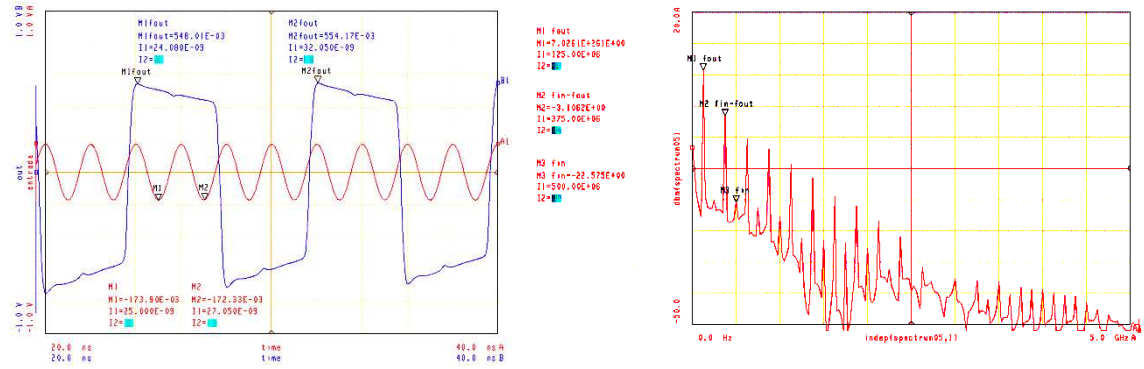

Figure 3.26: Input/Output waweforms (left) and output spectrum (right). P_{in}=-8dBm, F_{in}=0.5GHz, F_{out}=125MHz

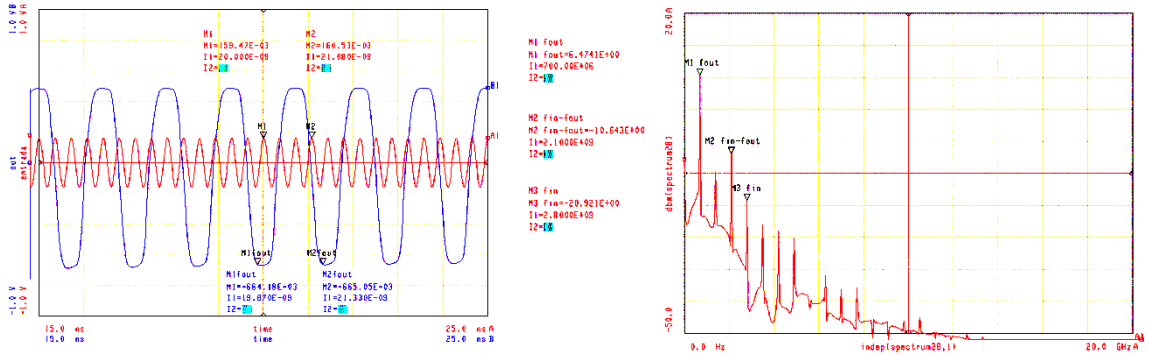

Figure 3.27: Input/Output waveforms (left) and output spectrum (right). P_{in}=-8dBm, F_{in}=2.8GHz, F_{out}=700MHz.

One of the most important parameters which describe the performance of a digital divider is its input sensitivity. The input sensitivity is defined as the minimum input power level for which the circuit works as a divider with the division ratio for which it

has been designed. In this kind of dividers maximum sensitivity (absolute value) is observed in correspondence of the "self-oscillation" frequency. The self-oscillation in absence of input signal (but in presence of white noise at the input) is typical of Emitter Couple Logic (ECL) dividers and consequently of SCFL which represent ECL counterpart using field-effect transistors.

The presence of self-oscillation for this type of circuits can be explained as follows. Being each divider-by-two implemented by a master-slave DFF with feedback from the inverted output, an output-to-input feedback path is established similar to what happens in ring oscillators (see chapter 4 for further details). Depending on the input clock state, one between the master and the slave is "transparent" while the other is latched to the value which was present at its output before the last clock state change, thus preventing self-oscillation. Without an input signal, flip-flop input differential voltage (clock and its complementary) are equal and zero. This state corresponds to an *invalid* logic level between HIGH and LOW states, which implies a transparent state for both the master and the slave. The circuit behaves as an inverter, and starts operating like a ring oscillator (the oscillation frequency is associated to the delay in the feedback path).

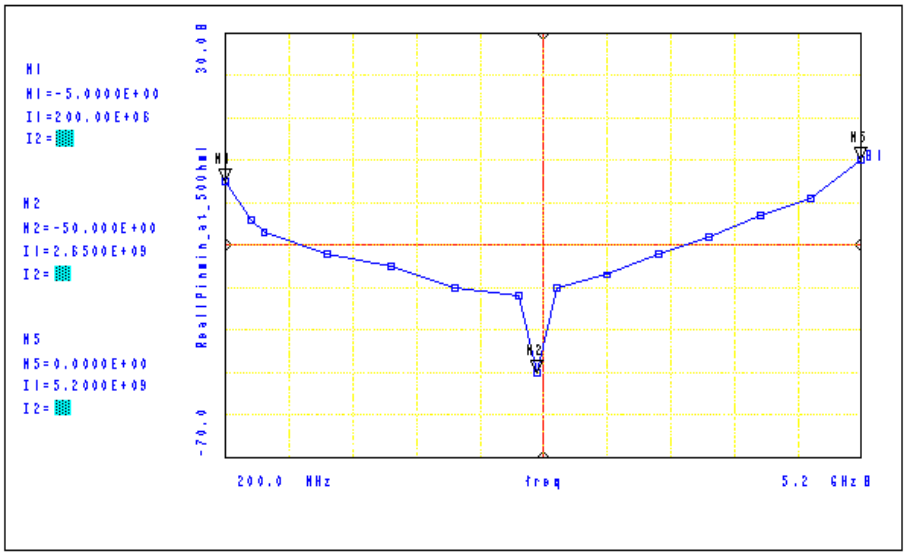

Figure 3.28: Input sensitivity at room temperature (25°)

Simulated results for frequency divider MMIC input sensitivity as a function of the input frequency is reported in Figure 3.28. The sharp peak between 2.6GHz and

2.7GHz corresponds with the self-oscillation frequency (~650MHz). It must be stressed that the self-oscillation of the circuit do not represent a problem as the input will be continuously fed by the VCO or forced to a low value.

3.4.3.6 MEASUREMENTS

Performance of the fabricated MMIC were checked both on wafer by means of the coplanar testing point and with the divider assembled on a test fixture PCB (Figure 3.29) with input/output 50Ω connectors.

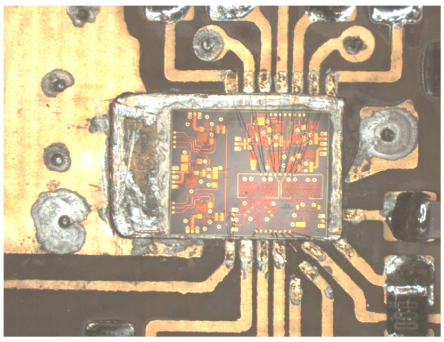

Figure 3.29: Photo of the chip assembled on the test PCB for the divide-by-four characterization

All the measurements were carried out with the help of a spectrum analyzer and a 40GHz microwave transition analyzer (HP71500A). In the following figures, a selected sub-set of results is shown.

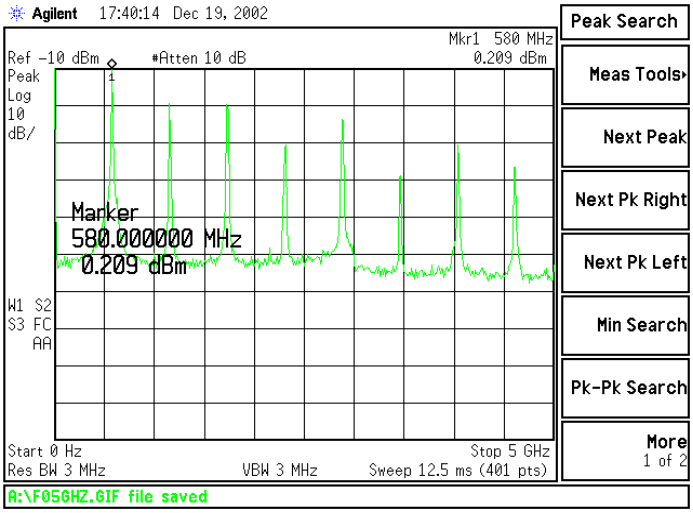

Figure 3.30:Output spectrum of the self-oscillation

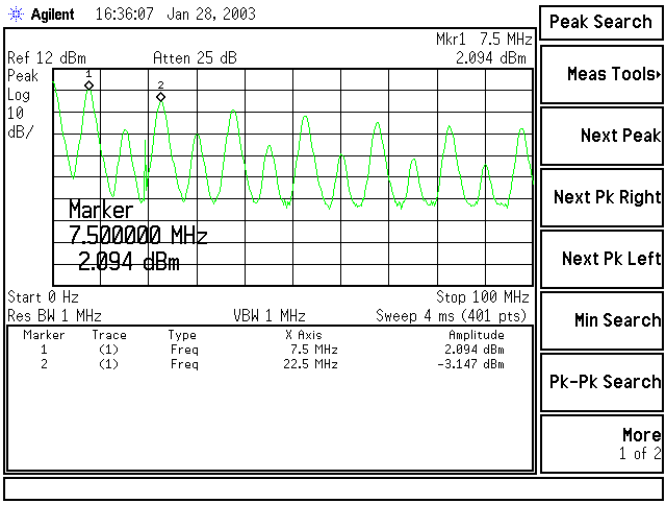

Figure 3.31: Output spectrum at minimum operating frequency (F_{in}=30MHz)

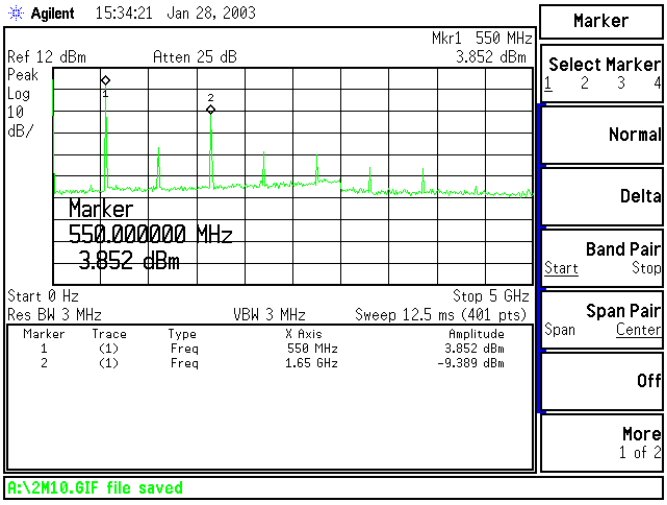

Figure 3.32: Output spectrum at self-oscillation frequency (F_{in}=2.2GHz)

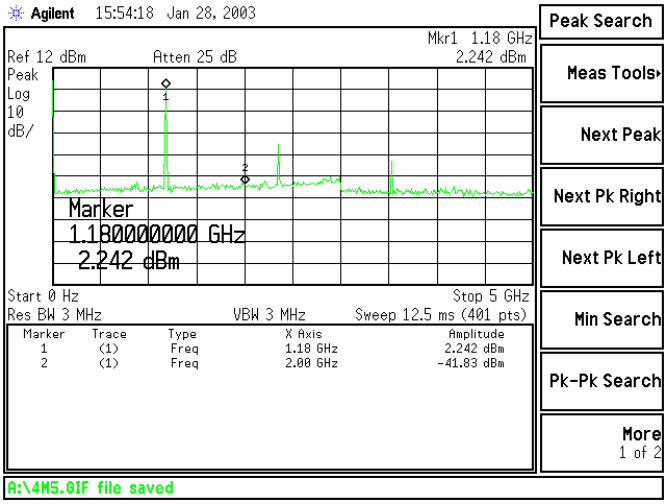

Figure 3.33: Output spectrum at maximum operating frequency (F_{in}=4.7GHz)

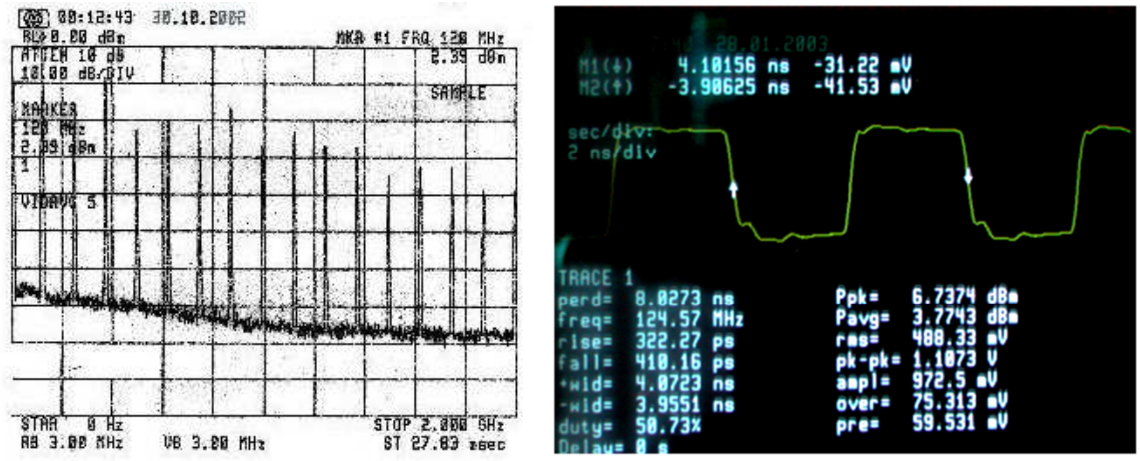

Figure 3.34: Output spectrum (left) and output waveform (F_{in}=500MHz, P_{in}=-10dBm)

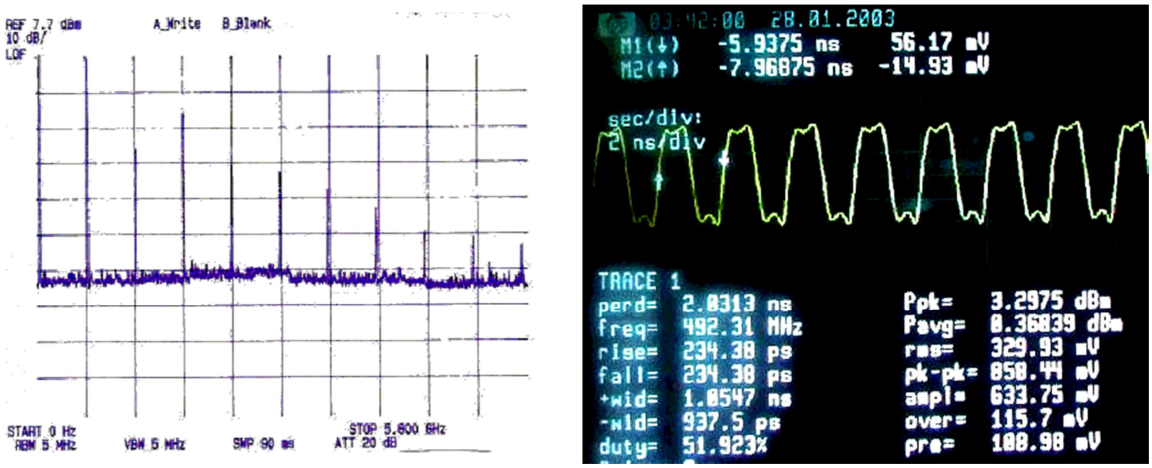

Figure 3.35: Output spectrum (left)and output waveform (F_{in}=2GHz, P_{in}=-10dBm)

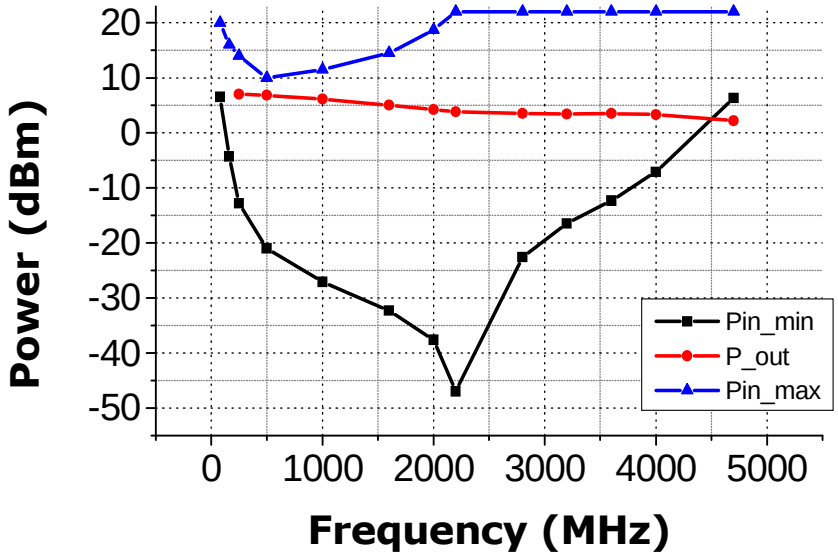

Figure 3.36: Measured input sensitivity and maximum input power (T=25°)

Figure 3.36 illustrates the measured input sensitivity together with the corresponding output power (measured with a power meter) and the maximum input power to ensure a correct behavior of the circuit.

The measurements are relative to the attenuated input and at room temperature, with a supply voltage of V_{Supply}= -5.2V. It can be noticed how the maximum sensitivity is in line with the simulated results and with the measured self-oscillation (slightly less than 600MHz). The circuit is capable to provide an output signal power of more than 4dBm (depending on the output buffer biasing) with the input ranging from 80MHz to 4.5GHz and a sensitivity window wider than 30dBm

The current consumption of the divider leading to the described performance is summarized in Table 3.4.

Table 3.4*: Detail of the measured divider power consumption*

Sub-circuit	Quantity	I(DC, mA)	V_{Supply}(DC,V)
Input Differential stages	2	4.1	-5.2V
Input Source Follower	2	4.6	-5.2V
SCFL basic cell	4	12.2	-5.2V
Output Buffer	1	11.5	-5.2V
Total		78	-5.2V

.

If we exclude power consumption figure, all the performance requirement were met by the circuit with significant margin. However, comparing the measured results with the original specifications it is clear that the power consumption figure is almost an order of magnitude bigger. This is associated to the technology used, as the value specified was derived from a CMOS implementation (which was discarded at the time of development because of the space requirements limitations and the non full compatibility with low noise and power requirements). An analysis was carried out to quantify the minimum power consumption which could be expected once the technology selection and associated circuital implementation. Disregarding the contribution of the buffers (which have been designed to interface with 50Ω system and provide a quite high security margin), focus was on the SCFL logic core.

Each of the cells contains three separate current sources (one in the differential core and two in the source followers, Figure 3.20) each of which draws approximately 4 mA. This high current consumption is associated with the behavior of the smallest pHEMT transistor, which can be used with the selected ED02AH technology (2x10µm). In order to ensure a proper behavior as a current source, the transistor should be biased in saturation (current≈constant). With a gate to source voltage (V_{gs}) set to 0, this happens when the drain to source voltage (V_{ds}) is greater than 1V. This situation corresponds roughly to a current consumption of 4mA (M1 in Figure 3.37). It would have been possible to lower this power consumption by using a lower V_{gs} , but to simplify biasing and layout this option was discarded for this first design iteration. Hence the power consumption obtained is in line with the minimum that could be expected with this topology and technology selection.

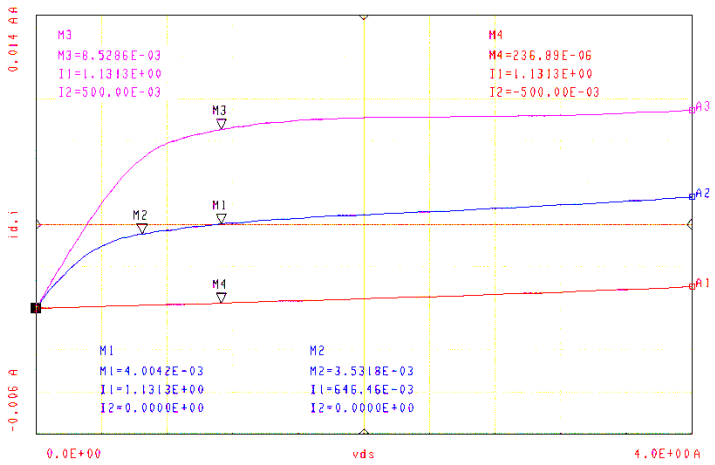

Figure 3.37: I/V characteristics of a 2x10um gate width ED02AH n-ON pHEMT transistor (I2=V_{gs} value)

Some units of the MMIC prototypes were also sent to Alcatel Space laboratories, to perform space qualification tests. In particular, the variation with the input sensitivity and the output power as a function of the temperature are illustrated in Figure 3.39 and Figure 3.40 showing the robustness of the selected circuit topology against temperature variation.

The downward shift of the self-oscillation frequency (Figure 3.39) has to be associated (and checked with simulations) to the fact that these measurements were carried out with different conditions (V_{Supply} reduced to 4.5V to minimize current

consumption) and on a different chip. Moreover, the circuit bias was optimized by the customer to ensure maximum output power and a better behavior only in the targeted frequency band (0.5 to 2.8GHz) disregarding higher frequency behavior.

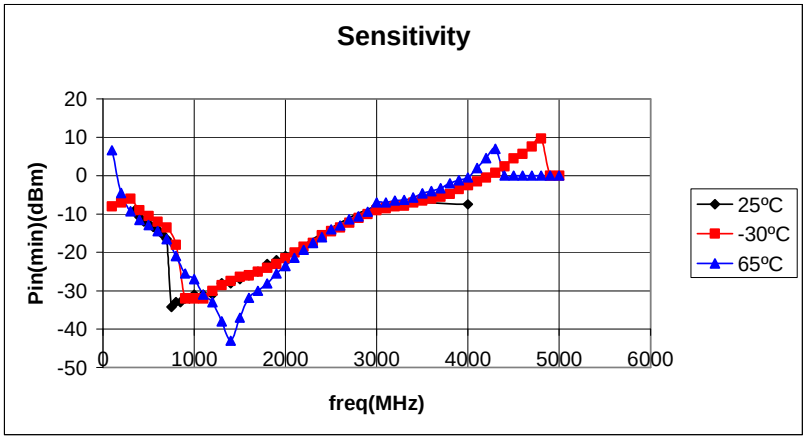

Figure 3.38: Measured Input Sensitivity as a function of the operating temperature

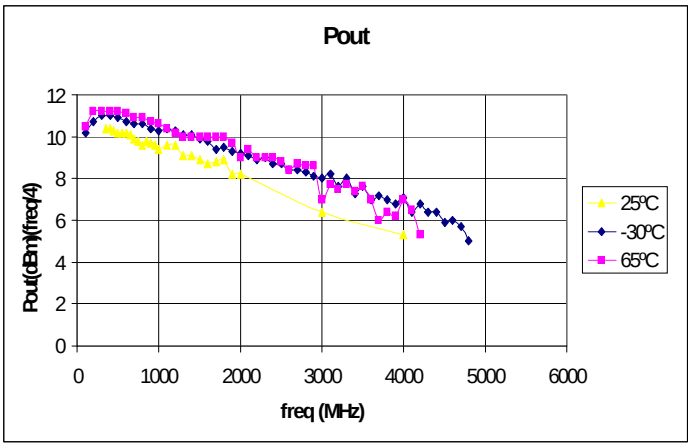

Figure 3.39: Output power @F_{in}/4 vs. F_{in} as a function of operating temperature.

3.5 COMPLETE CHIP PERFORMANCE

Once the individual characterization was completed, interconnection of the different functions in some of the operational configurations was tested. Connecting VCO and frequency multiplier as shown in Figure 3.3 and Figure 3.4, the resulting tripler output spectrum is shown in Figure 3.40. VCO is running at 750MHz and the composite output delivers more than +5dBm of output power with an output match

better than -15dB. Total power consumption is in the order of 91mA@3.5V. Measured phase noise of the third harmonic is -84dBc/Hz @100KHz.

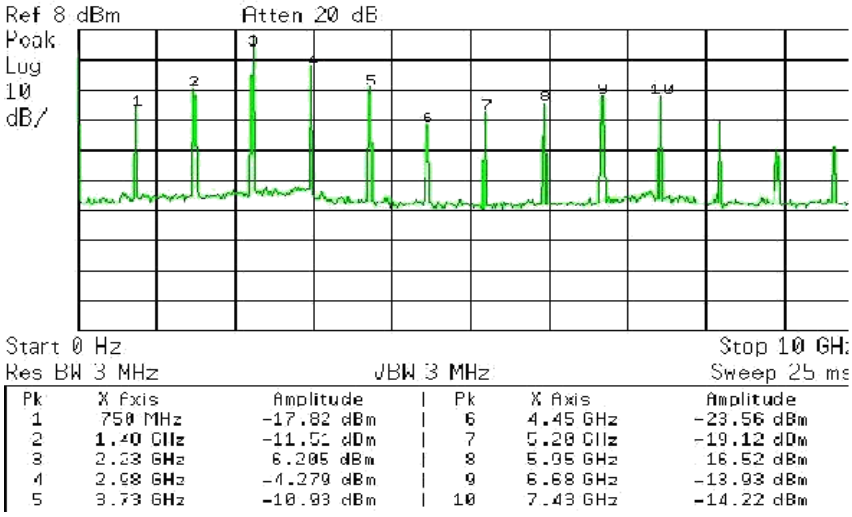

Figure 3.40: Output spectrum of the frequency multiplier with the VCO as input

The output of the VCO was also connected to the input of the divider. Input/Output waveforms and output spectrum are shown in Figure 3.41 and Figure 3.42 respectively. The 7dBm output power is obtained with a VCO output power in the order of +4dBm. Spurious level at F_{VCO}, $F_{VCO}/2$ and $F_{div/4}$-F_{VCO} is between 30 and 15 dB below desired signal ($F_{div/4}$) level.

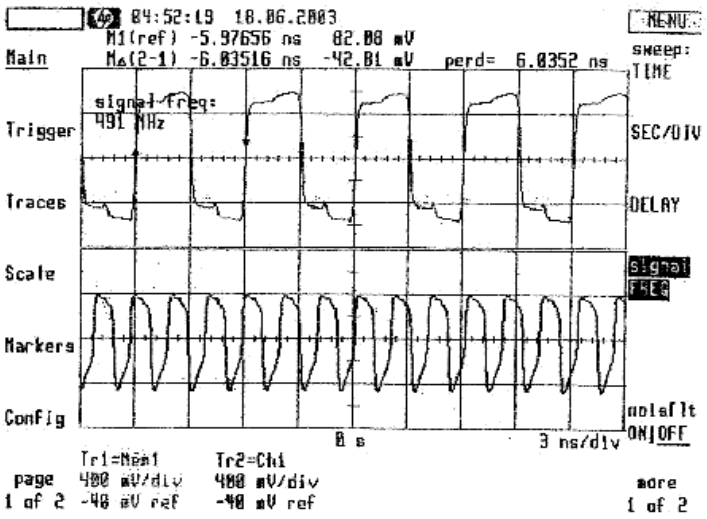

Figure 3.41: Output waveforms of the VCO and divide-by-four when interconnected (F_{VCO}=491MHz)

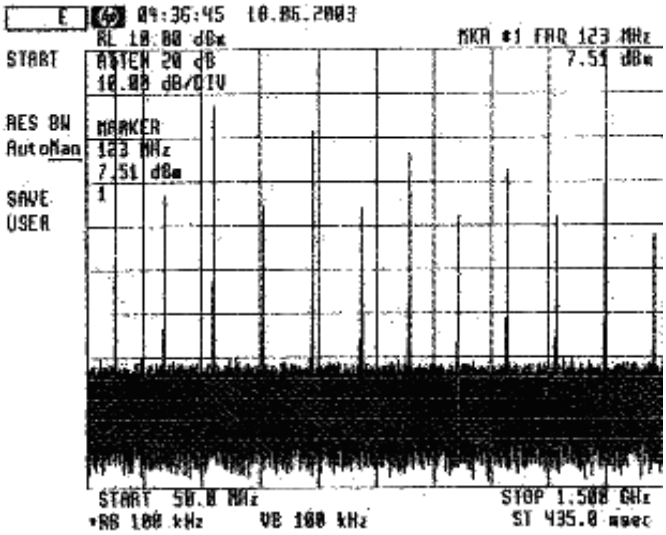

Figure 3.42: Output spectrum of the divider connected to the on chip VCO

3.6 CONCLUSIONS

The design, implementation and characterization of a multifunction MMIC targeting space applications (including a negatron, a multiplier by three and a frequency divider) have been presented. This custom multifunction MMIC circuit is in principle capable of providing a flexible and efficient solution for the generation of all the system frequencies in both transmit and receive modules for the S-band TT&C applications for which it was developed.

Measured results are in good agreement with the simulations and the overall circuit shows good performance. The negatron is able to provide oscillation in a band exceeding 1 GHz and phase noise performances (around -106dBc/Hz @100KHz offset), not far from the phase noise achieved with BiCMOS technology. The multiplier by three provides two outputs with more than 5dBm each and low spurious level. Frequency divider by four has an operating window from 80MHz to 4.5GHz with excellent sensitivity and an output power higher than 4dBm in the whole frequency band.

Despite the promising results obtained with the chip (which would have required an additional design step to fine-tune the performance and reduce the power consumption due mainly to the over-sizing of the active devices and buffers), the overall system design strategy changed during the design phase and a modular (multi-chip)

solution was selected instead by the customer. This was mainly driven by the excess variation of the on-chip fabrication parameters (the resulting chip size could not be reduced less than 4mm x 3mm) and by the additional flexibility of use of each individual circuit (i.e. each circuit could be used in a separate T/R chain). The separate circuits were then modified and optimized individually to allow their use in a plurality of applications.

Results of the final implementations will be given in chapter 5, while chapter 4 will be dedicated to the design and implementation of the dual-modulus divider which resulted from the upgrade of the divider by four presented in this chapter.

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4 . Dual modulus digital divider design and simulation

4.1 INTRODUCTION

Dual Modulus frequency dividers are widely used in modern cellular, GPS, and satellite communication systems and constitute an essential part of frequency synthesizers and PLLs used in transmit and receive modules. They are frequency dividers with two selectable division ratios which are commonly used to extend the frequency range of programmable dividers. Generally, the division ratio (being integer numbers) can be controlled through the variation of a single circuit parameter (e.g. the varactor bias voltage in an analogue divider or an external control voltage in a digital divider).

Despite the higher circuit complexity with respect to their analogue counterpart, digital dividers are used as fundamental building blocks in PLL feedback loops to implement dual-modulus prescalers. These circuits provide high order division ratios of the input signal frequency (128/129, 256/257 …) to lower its value down to frequency values comparables with the ones commonly used for PLL reference crystals.

Two division ratios N, N+1 or N-1 are usually implemented, being N a power of 2. Main problem is associated with the generation of the N+1 or N-1 division, as it requires the introduction of additional circuitry which limits the operating frequency if compared with the same divider operating as an integer power of 2 [4.1]-[4.5] from which they are generally derived. As a matter of fact, the latter are documented up to >100GHz whereas dual modulus dividers reach frequencies in the order of 50GHz.

The common implementation of dual-modulus prescaler comprises a synchronous circuit which works at the highest frequency and provides the variable ratio division

(the dual-modulus divider) and asynchronous counter plus combinatorial logic (Figure 4.1). The counter is usually realized cascading N DFF (each working as a divide-by-two hence resulting in 2N division) working at lower frequencies and providing high divide-by-value. This part of the prescaler is implemented with standard CMOS logic cells and is available as low cost commercial circuits or provided in the form of digital ASIC libraries for automatic placement inside the final circuit. The combinatorial logic is in charge of controlling and programming the whole circuit.

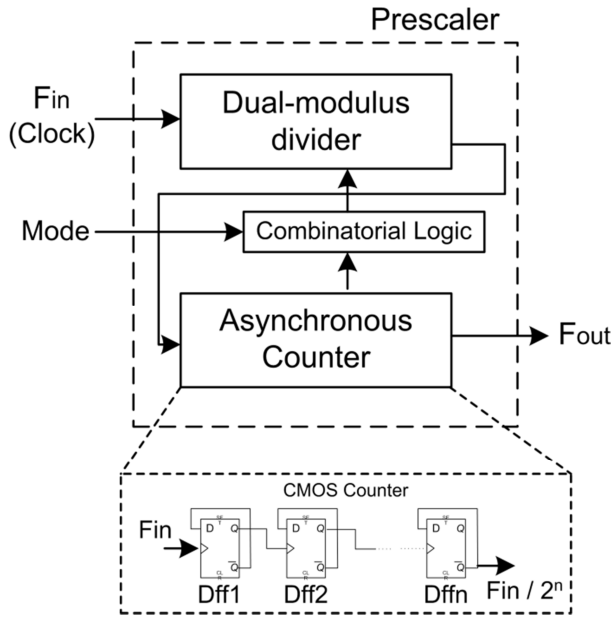


Figure 4.1: Block diagram of a generic dual-modulus prescaler and asynchronous counter.

This chapter presents a new dual-modulus frequency divider IC topology, which utilizes only two flip-flops and no external gates to overcome some of the drawbacks of conventional dual-modulus dividers.

The divider has been fabricated with a GaAs PHEMT technology (ED02AH from OMMIC) and extensively characterized in the frame of collaboration between the University of Cantabria and Alcatel Espacio.

Main goal of the work was to provide an evolution and performance improvements with respect to the fixed ratio divider presented in chapter 3 to match with updated requirements (Table 4.1).

Additionally to the conventional digital divider design tools (i.e. transient simulations), an analogue description of the operation principle of digital dividers is

proposed and validated through Harmonic Balance (HB) tools. The "*switched-ring oscillator*" which can be used as basic building block for fixed-ratio dividers is extended to describe variable-ratio dividers functioning, potentially serving as a design guide for any kind of multiple ratio frequency divider .

The analogue modelling of digital dividers is then exploited to apply to the implemented divider simulation tools whose utility is normally limited to analogue dividers (HB, phase noise analysis and envelope-transient) with the potential of speed-up and simplify the design of complex digital circuits with a high number of non-linearities.

Table 4.1: Dual Modulus divider updated design specifications

Id	Characteristic	Value			Units	Conditions
		Min.	Typ.	Max.		
P_d	Dissipater power				mW	Minimum
V_{dd}	Supply Voltage		3.5		V	
D	Division Ration	3		4		
F	Bandwidh	500		2800	MHz	Both division ratios
P_{in}	Input power		-5		dBm	Sensitivity
P_{out}	Output Power		0		dBm	@50Ω,both outputs
Z	Output impedance		50		Ω	
SEL	Latch-up		immune			
SEU	Single Event Upset			10^{-9}		Errors per bit/day
T	Temperature	-30	25	70	°C	

Even if the circuit was specifically designed to be used in transmit/receive modules of TT&C satellite transponders, it showed very interesting results even for the implementation of the first stage of generic low-power high-speed dual-modulus prescalers

4.2 DUAL MODULUS TOPOLOGY

The majority of dual-modulus dividers reported in literature are based on the structure of Figure 4.2 which represents a modification of the conventional Johnson counter. The circuit is capable of providing N and N+1 division ratios, with N generally set to 4.

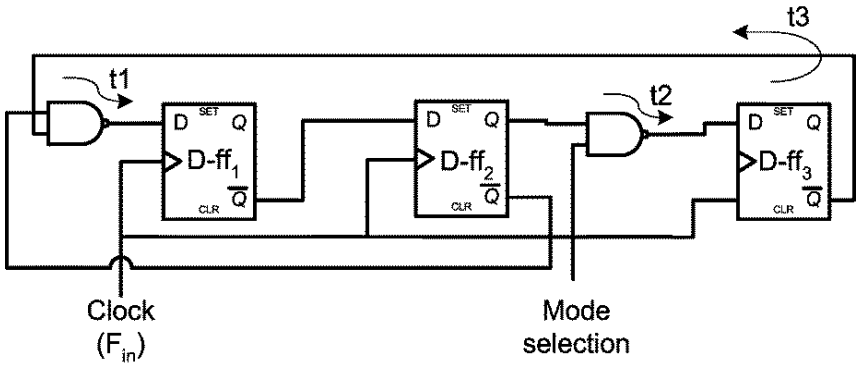


Figure 4.2: Block diagram of the dual-modulus (N, N+1, N=4) Johnson divider.

When the mode signal is low D-ff_3 is bypassed (Q3=1, notQ3=0) and the circuit behaves like a conventional divider by four as described in the previous chapter. In principle, the operating speed is limited by the technology used for its implementation (cut-off frequency), transistors´ size, and current consumption, as the maximum operating speed is associated to the maximum speed at which the transistors can switch between ON and OFF state.

When N+1=5, the third DFF stores a high value during a clock cycle, masking the feedback effect of D-ff_2 on D-ff_1, hence preventing division during that clock period generating the `+1'. In Figure 4.3 is shown the time chronogram of the divider.

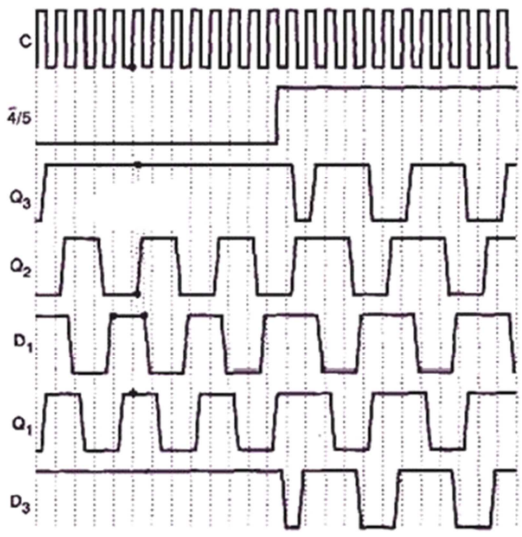


Figure 4.3 : Time chronogram of the Johnson dual-modulus divider.

This topology suffers from two main drawbacks. The operating speed is limited by the delays associated to the NAND gates (t1 and t2) and the propagation delay of the signal across the third DFF and the feedback toward the first DFF (t3). Thus, the propagation delay (T_{clk}) in the critical path from Q2 to D1 must satisfy the relationship:

$$T_{clk} > t1 + t2 + t3$$

Where, T_{clk} is the period of the clock input signal. If this condition is not met, the signal will not be able to reach the first D-FF before the next clock edge. The bigger t1, t2 and t3 delays, the lower will be the maximum operating frequency compared with that of the fixed ratio divider.

The second problem is associated with the presence of the third DFF. If we were able to implement the same functionality with a lower number of DFF, a significant reduction in layout area and power consumption would be possible.

A solution to this problem has been found by using a new solution with a lower number of associated delays. The proposed topology is sketched in Figure 4.4 for the case N-1, N, with N=4.

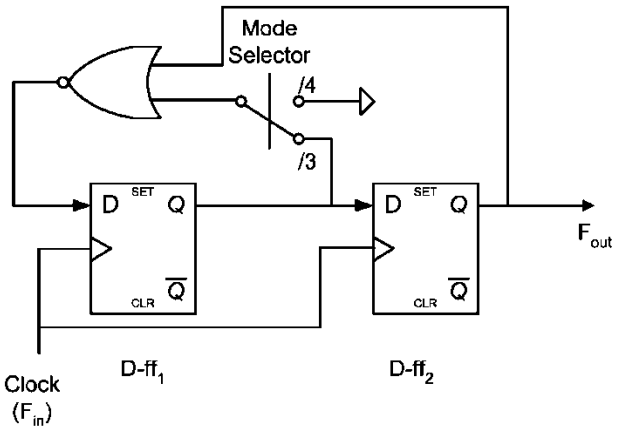


Figure 4.4: Logic diagram of the proposed dual modulus (N-1,N, N=4) divider.

As shown in Figure 4.5 (which has been derived with the help of SIMULINK©), the circuit is capable of providing a double division ratio by using only two DFF. The circuit works as follows: for the division-by-4 mode, Q1Q2 sequence of states is 00 10 11 01 00 and so on. In division-by-3 mode, whenever Q1=1 the circuit resets this output skipping the 11 state, resulting in the state sequence 00 10 01 00, hence dividing by three.

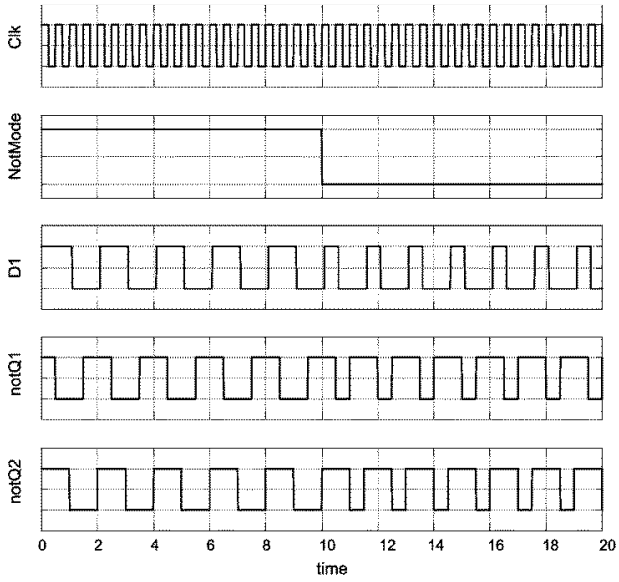


Figure 4.5: Time chronogram of the proposed dual modulus divider.

Doing so, the number of D-FF required to implement the dual modulus division has been reduced to 2 (with a consequent net saving in area and power consumption of more than 30%), and the two NAND gates (and associated delays t2 and t3) have been substituted by a simpler (and quicker) NOR gate, however there is still a logic gate in the signal path which can reduce the maximum speed of operation.

4.3 CIRCUIT DESIGN

4.3.1 Dual Modulus divider core

The solution to this problem has been found merging in the first D-FF the control signal logic (the NOR gate) and the mode control. In addition to allowing the operation at the same speed as the basic divide by four, this solution further reduces the power consumption (as an additional current source is removed) and layout area.

Utilizing for the D-ff Source Coupled FET Logic architecture (SCFL) presented in chapter 3, the merging of the additional circuitry can be accomplished with an additional level of series gating in the first D-ff. Figure 4.6 shows a simplified diagram of the proposed prescaler.

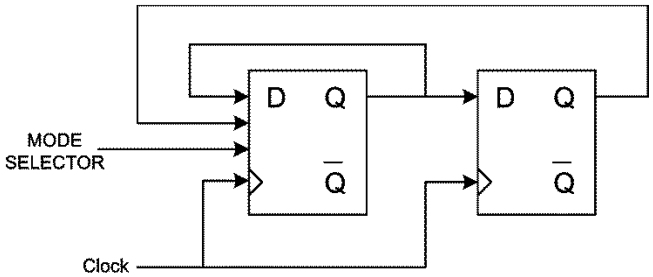


Figure 4.6: Simplified block diagram of the implemented prescaler

In order to implement the circuit in a fully differential topology such as SCFL, all the signals must be present throughout the circuit with its complementary counterpart. Using basic logic equivalences, it can be demonstrated that a NOR feedback path from the second DFF to the D input of the first one (divide-by-3 mode), requires as complementary signal a NAND feedback from the complementary output (Figure 4.7). On the other hand, these logic gates should de deactivated when the circuits operates in division by four.

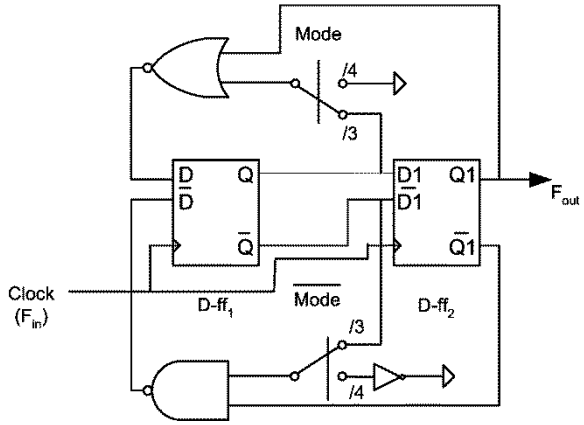


Figure 4.7 Fully differential (SCFL) logic scheme of the dual modulus divider

In order to better understand the functioning of the circuit, one should keep in mind the logic equivalences described previously in chapter 3. The standard SCFL logic cell can be modified to implement the proposed dual-modulus architecture by introducing properly sized transistors[3] in the first DFF (Figure 4.8).

[3] *For the circuit to operate properly, all transistors in the logic cell must operate in Saturation all the time.*

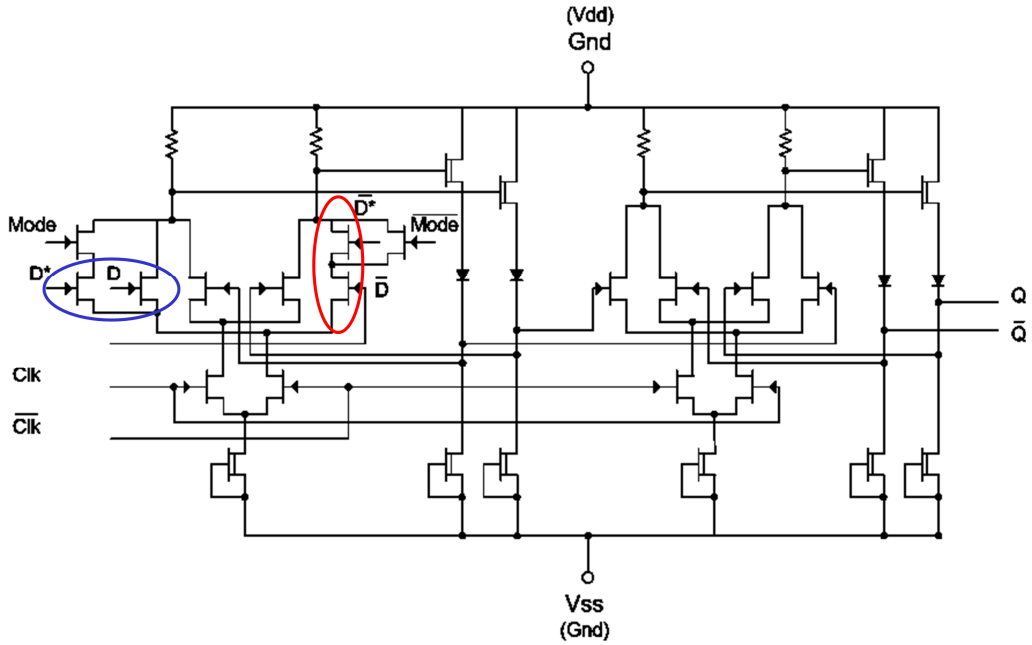


Figure 4.8: Modified SCFL cell.

The NOR (plus NAND) function necessary to implement the mode-selector has been also embedded in the modified DFF. When the mode selector input (Mode) is LOW (and its complementary signal is HIGH) the circuit acts as a divider by four. In fact, by adequately selecting the control signal levels, the correspondent gate is always in its OFF state preventing the current to flow in the associated circuit branch, effectively deactivating the "*mode*" transistor D* (≈open circuit) while its complementary transistor (not D*) is by-passed (≈ short circuit): the logic cell is then equivalent to a standard SCFL D-ff.

If the mode selector is set HIGH the mode transistor is turned ON, so allowing the implementation of the NOR and NAND functions required for the division by 3 (complementary signals will be present at the complementary branch).

The complete schematic of the dual modulus divider is obtained by cascading two D-ff (the first one being the modified cell) and connecting properly the feedback paths (Figure 4.9).

It may be noted that, in order for the circuit to work properly, both the logic gates and the control signals need to be adequately selected. In such a way, no external gate is required and the resultant dual-modulus divider will have, in principle, the same speed limitations of the basic divider from which it derives.

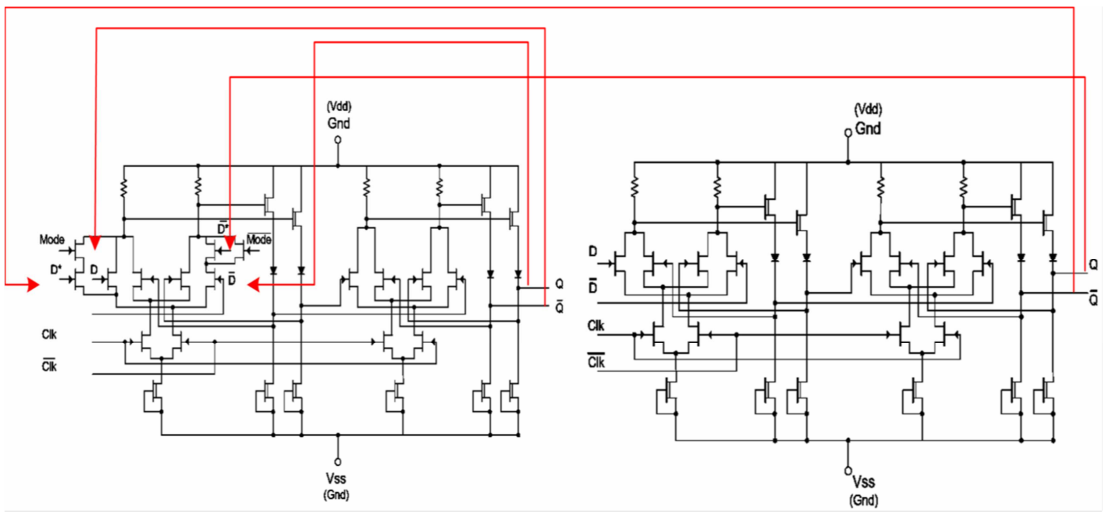


Figure 4.9: Complete schematic of new the dual-modulus divider

4.3.2 Input and Output Buffers

In addition to the logic core, two buffers have been designed to guarantee the functionality and testing of the circuit in a conventional 50Ω system and to ensure enough output power to drive the loads. DC decoupling of the logical core (which functionality is intrinsically DC-coupled) is also performed.

4.3.2.1 INPUT BUFFER

The input buffer is an optimized version of the circuit described in section 3.4.3.3.1. To reduce power consumption this circuit does not provide any amplification because the logic cells have been designed to work even with very low input power. In Figure 4.10 is showed the schematic diagram of the complete input buffer including the level shifting source follower. The circuit also provide the DC-decoupling function of the digital core.

4.3.2.2 OUTPUT BUFFER

As far as the output buffer is concerned, the previously adopted solution has been discarded because of some problems associated with the biasing of the transistors (high failure risk during the switch-on process which could cause failure in space missions

conditions) and because an update in the design requirement imposed the availability of both logic outputs (normal and complementary) for processing.

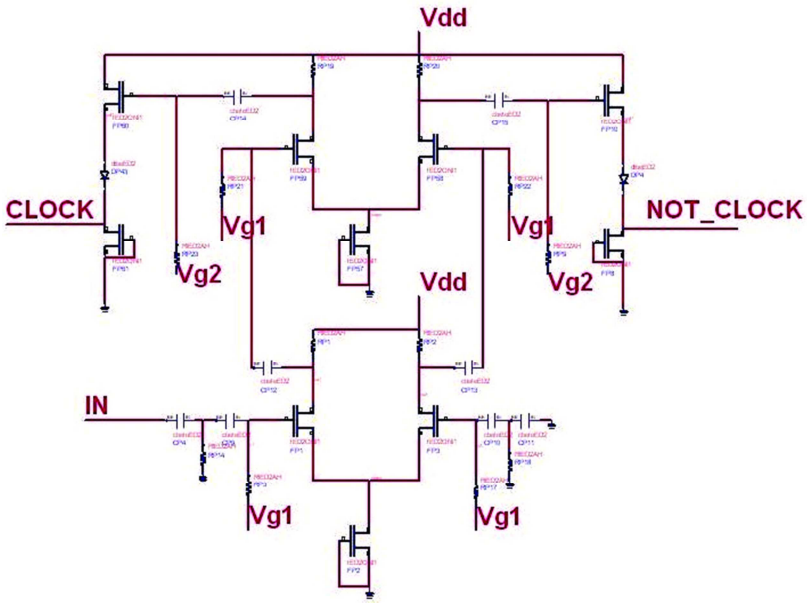


Figure 4.10: Schematic of the input buffer: double stage differential amplifier and a couple of source follower which generate the complementary clocks driving the logic circuit.

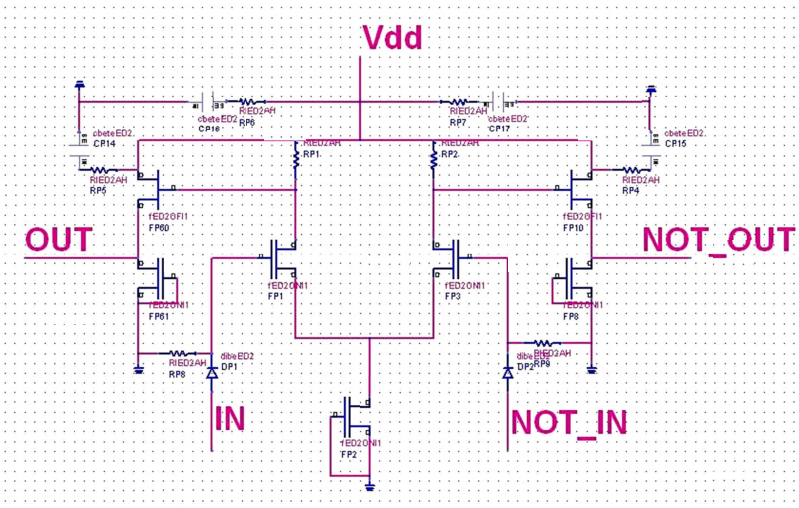


Figure 4.11: Schematic of the output buffer: differential amplifier and a couple of common-source amplifiers

Two common source amplifiers were selected to provide the required power level for both outputs. The interface between the logic core and the output stage was implemented with a single stage differential amplifier connected to the D-ff outputs. The two differential outputs of this amplifier are connected directly to the common-source amplifiers inputs-

As can be noted from the schematic the whole output buffer is still DC-coupled and the output must be connected to external DC-blocks. This solution was needed to reduce layout area and to avoid too large transient behaviour during the changing of the division mode (the DC blocking capacitors required to minimize transient behaviour due to the frequency divider output frequencies were too big for on-chip integration). The diodes at the input of the differential amplifier are used for level shifting to properly bias the differential stage which is driven directly by the digital outputs. Multiple RC networks have been also integrated to stabilize the circuit at high frequencies.

4.3.3 **Mode Generator Circuit**

This circuit has the function of generating a couple of complementary signals from a single-ended mode signal. The need was motivated by the fact that the generation of such signals outside the circuit (i.e. on the PCB) would require excessive amount of area. The signals generated by the circuit should have values which allow the switching of the mode selection transistors (Figure 4.8) between the"on" and "off" state. The input signal (MODE IN) values HIGH and LOW should vary in the interval [0, Vdd].

To implement the function a differential inverter has been used. The input signal is compared with a threshold voltage generated by a resistive divider and, depending on its value, the complementary outputs are generated. Proper output levels are ensured by selecting the current which flows in the circuit and the pull-up resistors (Figure 4.12).

When the input signal is LOW, the divider will operate as divider by 4, whereas when HIGH as divider by 3.

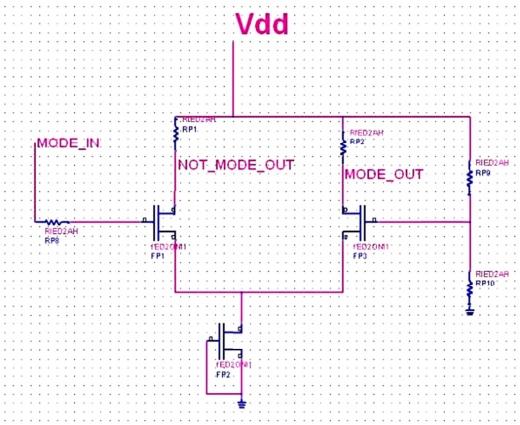


Figure 4.12: Schematic of the Mode signal generator circuit. The input resistor was added to protect the gate of the input transistor from excess of gate current.

4.4 TRANSIENT SIMULATIONS

In this section are presented the results of some relevant simulations carried out with ADS transient simulator. In all the cases the input and output impedance are set equal to 50Ohm and the simulations include the input and output buffers. If different impedance is used, it will be indicated in the figure caption. The nominal temperature is set to 25ºC, but simulations at -30ºc and 70ºC have been carried out to ensure thermal stability.

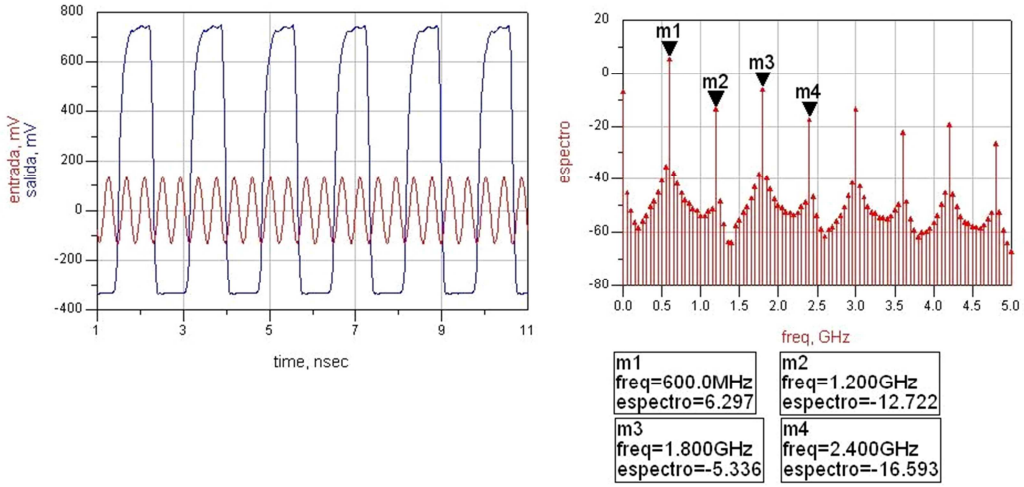


Figure 4.13: Input/Output waveforms and output spectrum: mode=LOW, Fin=2.4GHz

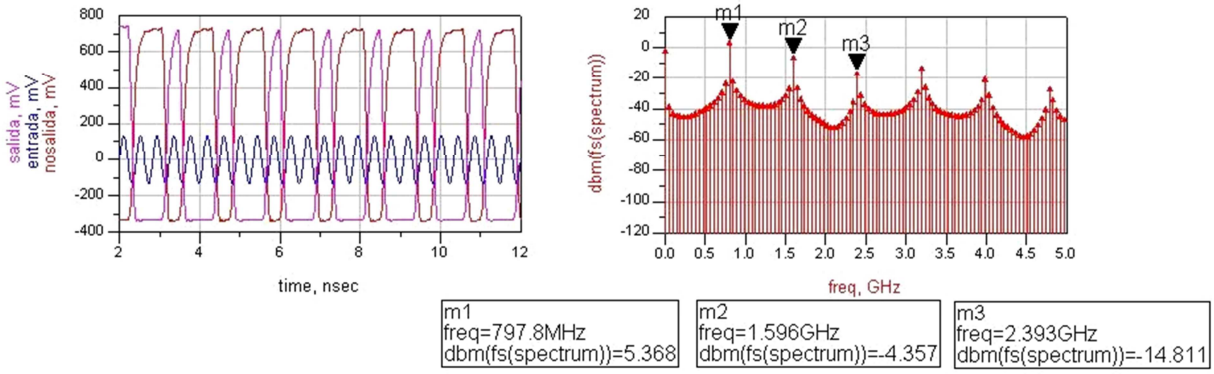


Figure 4.14: Input/Output waveforms and output spectrum: mode=HIGH, Fin=2.4GHz

As can be noted in Figure 4.14, in the case of the division by three (MODE=HIGH) the duty cycle of the output signal is not 50% as in the case of the division by four (a situation which is normal in this type of dividers), and consequently the two outputs will

have slightly different output power (≈1 dB). However, HIGH and LOW logical values (and voltage swing) at the output of the D-ff are the same in all the cases.

One aspect that is worth a clarification is the reason why the output waveforms shown in the figures (DC decoupled by means of external capacitors) are not symmetrical with respect to 0V. This can be easily explained considering how the current in the output amplifying stage has been set and why 50Ohm loads are used in the simulations.

The maximum negative excursion ($V_{\_Peak}$) when the current flows through a load resistor (R_{Load}) is given by:

$$V_{\_Peak} = R_{Load} * I_{\_load}$$

In the specific case, the output power level was specified at 50Ω to cope with different load and to resemble the loading with a conventional power probe. In order to achieve an output power level of at least 3dBm on a 50 Ω load (to take into account some implementation error margins) $I_{\_load}$≈6.5mA, resulting in a $V_{\_Peak}$ ≈325mV when the output is at logical LOW value and the current flows in the resistor, which is indeed the value observed in the simulation results. When the output goes high, no current flows in the resistor and the circuits operate in voltage mode reaching higher value in the waveform excursion.

As the requirement on the output is mainly on the power level, this does not represent a major drawback. To demonstrate proper behaviour of the circuits, Figure 4.15 shows the response with a high impedance ($R_{\_load}$=10KOHm).

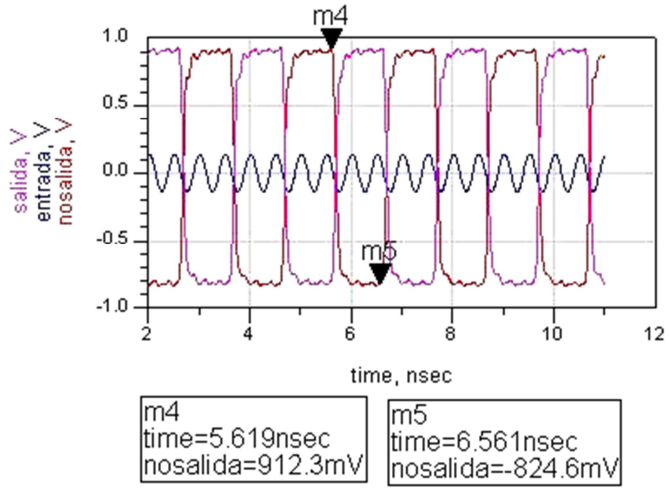


Figure 4.15: Input-Output waveforms and Output spectrum Fin=2.0 GHz, Pin=-10dBm, Mode =low), Temp =25ºC, R_load=10KOhm

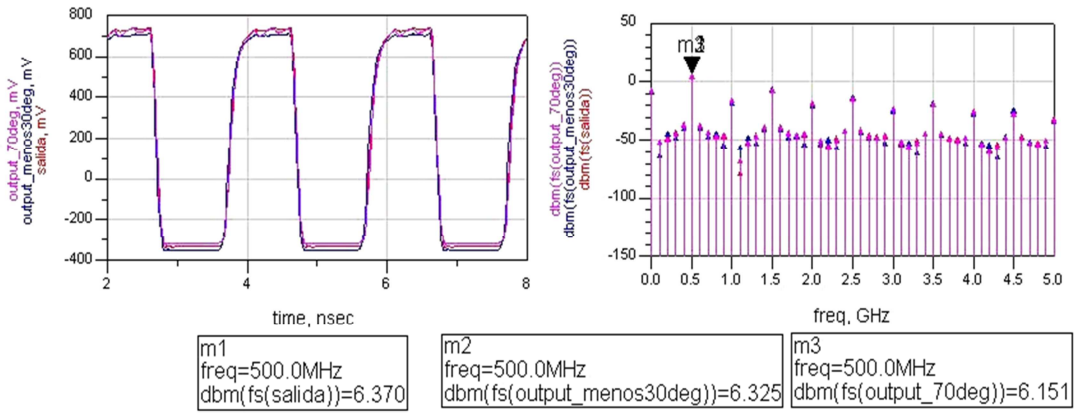


Figure 4.16: Input-Output waveforms and Output spectrum Fin=2.0 GHz, Pin=-10dBm, Mode =low), at three different operating temperatures (-30º, 25º y 70º).

The sensitivity simulations for the two divider ratios have been made separately at the worst case temperature of 70ºC and are reported hereafter. Additionally, it has been simulated (not reported here) that the circuits works correctly with input power values up to +10dBm

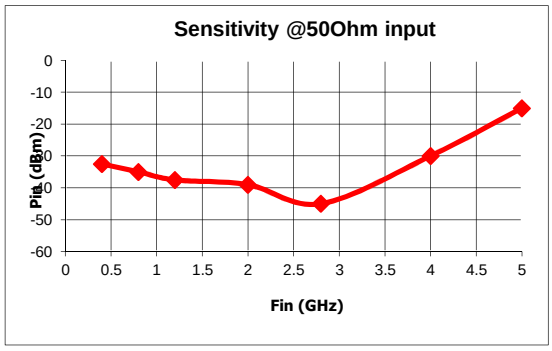


Figure 4.17: Input Sensitivity as a function of the input frequency in divide-by-4 mode.

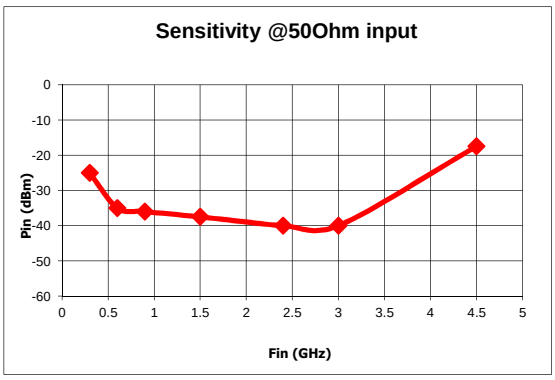


Figure 4.18: Input Sensitivity as a function of the input frequency in divide-by-3 mode.

It is important to underline that for the circuit to behave correctly, it should terminate a complete division cycle before changing the division ratio. To verify the proper behaviour of the circuit, the changing of the division mode has been simulated (Figure 4.19 and Figure 4.20). The mode signal has been modelled as a stepwise function with the high and low values corresponding to the LOW and HIGH levels of the mode generator.

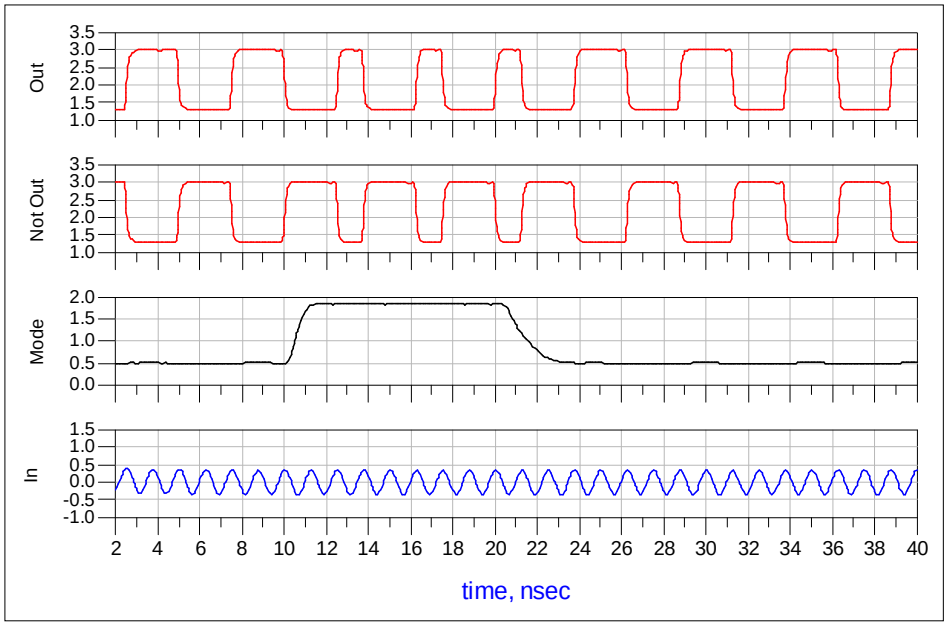


Figure 4.19: Changing of the division ratio at Fin=0.8 GHz, Pin= 0dBm, T=25ºC. No output load.

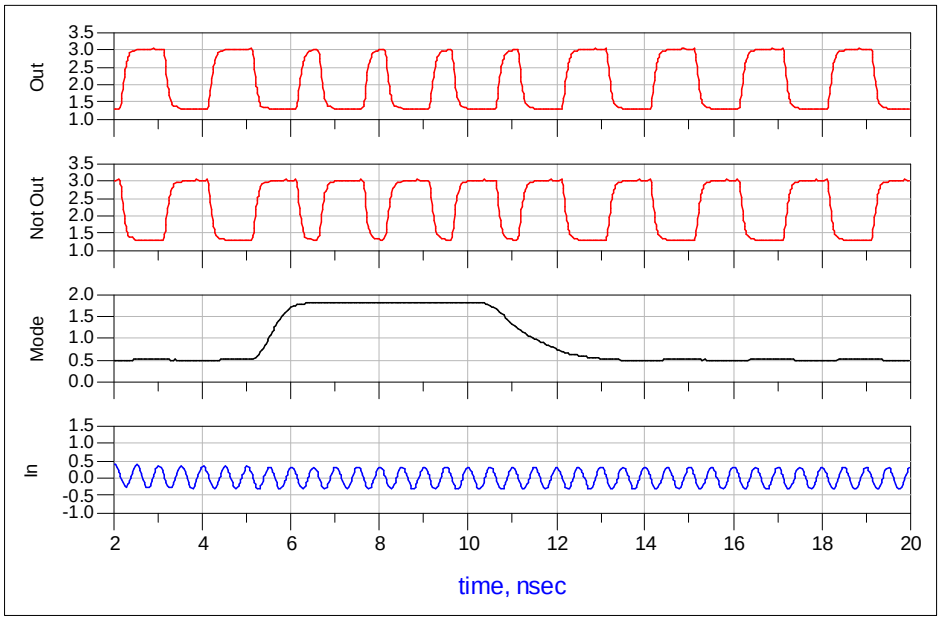


Figure 4.20: Changing of the division ratio at Fin=2.4 GHz, Pin= 0dBm, T=25ºC.. No output load.

As the circuit will operate with a single positive supply voltage (Vcc=+3.5V) and all other bias voltages (Vg1 and Vg2 in Figure 4.10) will be generated through voltage dividers, the behavior of the current during the turn-on has been monitored in all the building blocks to guarantee the absence of current spikes (Figure 4.21).

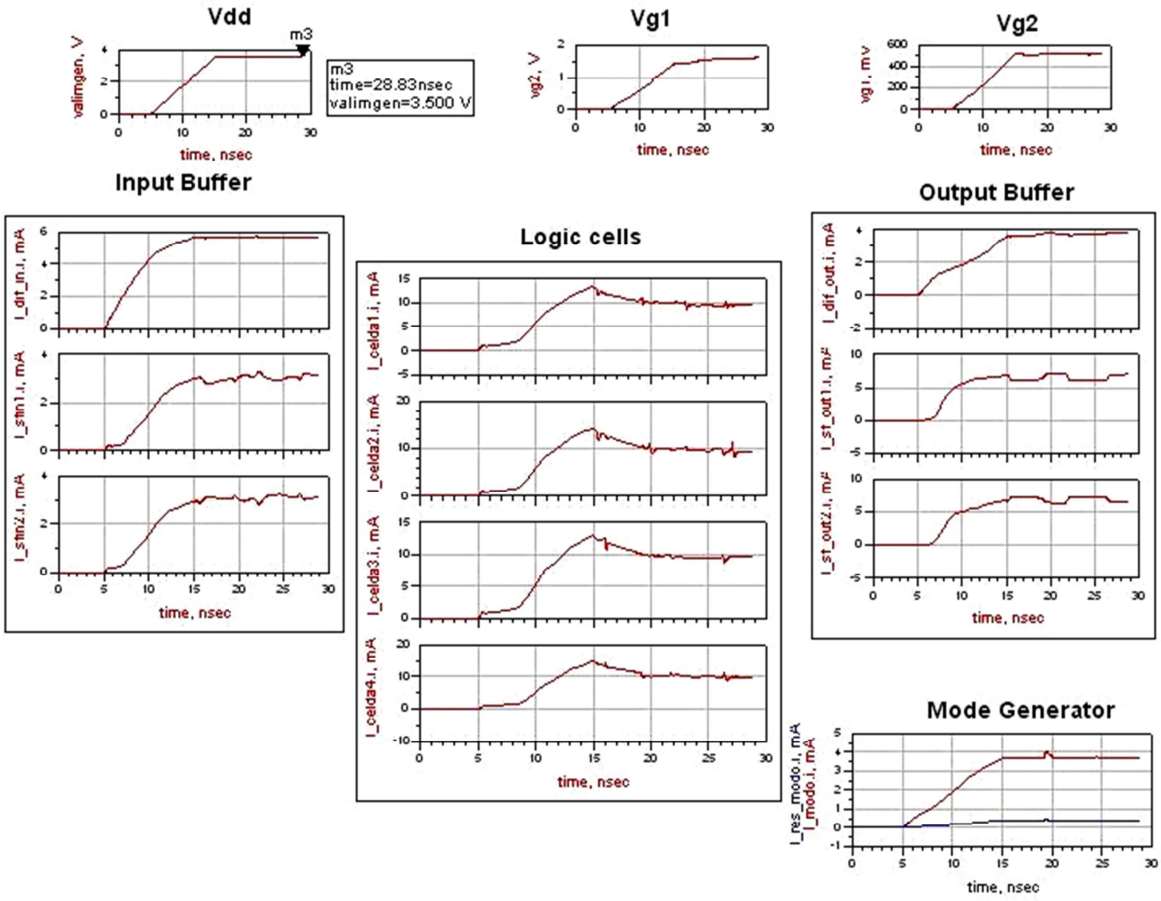


Figure 4.21: Current behavior during the switch-on. Mode=LOW, T=25ºC (Supply voltage=Vdd)

Yield analysis has been performed on the circuit in the worst case (70 º C**)**. Different input frequencies, input power levels and division ratios have been analysed. All the analyses have been carried out by way of transient simulations in a time interval and with a number of samples adequate to compute the Fourier transform of the signal and without overloading the simulator (otherwise causing the simulator to fail). Due to the inherent limitation of the transient simulations (to find the steady state response ideally an infinite duration of the simulation is needed) in some cases the interval chosen was not sufficient to estimate the correct Fourier transform (initial transient was quite long).

As a consequence, the results given in this section represented only an approximation of the real behaviour which had to be checked through real tests.

However, useful information was obtained from the simulations. Indeed through a careful analysis of the results it has been possible to establish which control voltages should have been left accessible on the chip to allow a post-production tuning for maximizing the yield of the fabrication run. The simulation parameter selected for monitoring in the yield simulations was the output power level. This selection was justified by the fact that it allows the verification of both the functional behavior of the circuit (by checking the presence or not of the divided solution) and that the output power level is compliant with the design requirements.

The statistical behavior of the fabrication process parameters' variation, is illustrated by means of t samples histograms and cumulative Probability Density Function (PDF) graphs. In such a way it is possible to monitor which is the probability that the selected parameter (in our case $P_{out}@F_{in}/4$ or $@F_{in}/3$) shows values lower than the specifications.In Figure 4.22 and 4.23 are plotted the number of samples versus output power histogram and the cumulative PDF of the output power for two different configurations (@Pin=0dBm). The results are similar for any power and division ratio inside the sensitivity window.

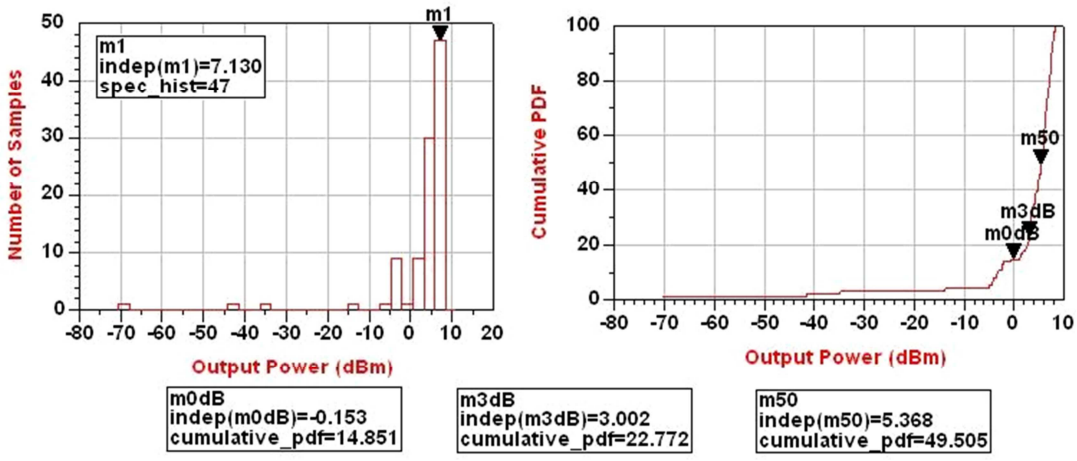


Figure 4.22: Output power histogram and cumulative PDF @Fin/4. (Fin=2.4GHz, Samples=101)

Simulation results confirm the robustness of the selected topology (SCFL) against process parameter and temperature variations. It can be noticed how more than half of

the samples (m50 in the graphs) have a output power even bigger than the nominal one, whereas almost 80-85% of the samples have a P_{out}>0dBm which was the original design requirement.

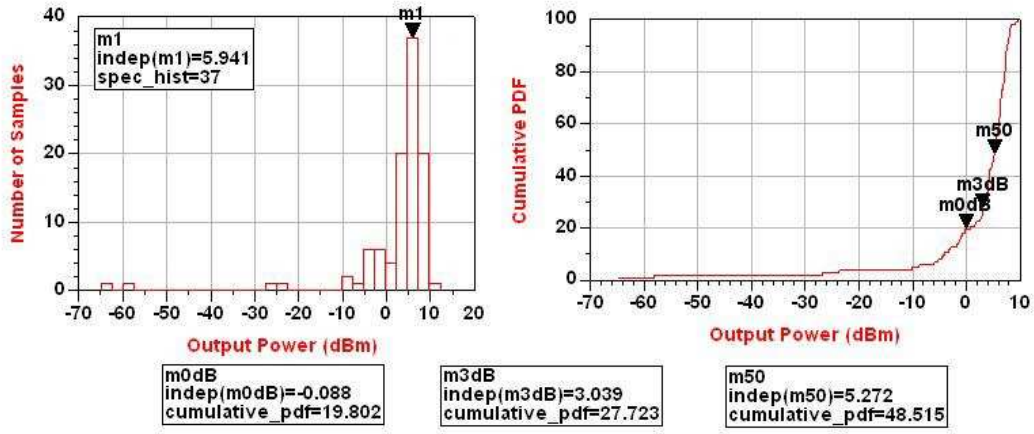


Figure 4.23: Output power histogram and cumulative PDF @Fin/4. (Fin=800 MHz, Samples=101)

Simulation results confirm the robustness of the selected topology (SCFL) against process parameter and temperature variations. It can be noticed how more than half of the samples (m50 in the graphs) have a output power even bigger than the nominal one, whereas almost 80-85% of the samples have a P_{out}>0dBm which was the original design requirement. Table 4.2 summarizes some of the results obtained at relevant operating frequency. (For a detailed explanation of the results refer to the same considerations in section 2.7).

Table 4.2: Overview of the yield results

Conditions (Input Freq)	Input Power	Prob. of Pout>0dBm.	Mean value(*)	Error +/- %	
				CL=95.4%	CL=99.7%
800 MHz,	-10dBm	86%	5.75	7.65	11.5
800 MHz	0dBm	80%	5.35	8.5	12.75
2.4 GHz	-10dBm	75%	5.2	7.56	11.34
2.4 GHz	0dBm	85%	5.4	8.24	12.37

(*)The mean output power is estimated considering the output power of at least 50% of the trials

It is relevant to underline how these results were obtained keeping fixed the value of all the circuit control voltages (including input and output buffer bias). By isolating the non compliant samples, it was possible to identify both the most critical process parameter to be monitored for the selection of the chips and how to act on the control voltages to

recover a significant amount of originally non-compliant chips. These considerations justified the choice to proceed with the fabrication of the circuit.

A summary of the simulated results is presented in Table 4.3.

Table 4.3: Summary of the simulated performance

Id	Characteristic	Value			Units	Conditions
		Min.	Typ.	Max.		
V_{cc}	Power Supply		3.5		V	
I_d	Current	69	72	75	mA	@nominal V_t
F_{in}	Input Frequency	<0.4		>4.5	GHz	All division ratios
Div.	Division Ratio	3		4	MHz	
Z_{in}	Input Impedance		50		Ω	
Z_{out}	Output Impedance		50		Ω	
P_{out}	Output Power		6		dB	Both Outputs, 50Ω
S	Input Sensitivity	-20	-10	5	dB	
T	Temperature	-30	25	70	°C	

4.5 HARMONIC BALANCE SIMULATIONS: AN ANALOGUE DESIGN APPROACH FOR DIGITAL DIVIDERS

4.5.1 Introduction

Design and analysis of analogue and digital dividers have been traditionally considered as worlds apart. The former is based on the solution of a circuit with a reduced number of non-linear devices (1 or 2) subject to harmonic excitations, and it is solved in the frequency domain. On the other hand, in digital dividers the number of non-linearities tends to be quite large (hundreds) and a high number of harmonics is required to fully characterize the circuits. These aspects increase substantially the computation time and may prevent the convergence of HB simulation (especially in the case in which distributed elements, i.e. microstrip lines, are included in the simulations). For this reason, time-domain simulations are normally used (despite time consuming especially in the case of long transients) to predict digital divider's behaviour. This approach was adopted for the design of the fixed digital divider described in the frame

of the present work (chapter 3) as well as the basic design approach for the dual-modulus divider described in this chapter.

Several examples of digital divider topologies can be found in the literature, but a general methodology to guide its design and to explain its functioning principles based on a simple analogue fashion, eventually allowing the application of more efficient Harmonic Balance simulation tools, have never been developed. The first goal of this part of the work was to provide an answer this question and the reason why an analogue equivalent model has been developed.

During the development of the digital prescaler it was in fact discovered how even this type of circuits could be explained and designed applying an analogue approach both for the circuit topology and simulation tools. The method is based on a simple ideal elements model (inverters, buffers and switches defined by simple equations) for a digital frequency divider: the *"switched-ring oscillator"*. Common aspects were identified by modelling the digital/analogue modes of operation through equivalent topologies and the use of frequency domain simulations.

A general analogue design methodology for variable ratio frequency dividers was then derived and a phase noise analysis based on Harmonic Balance (HB) originally developed for oscillators has been applied to the designed dual modulus prescaler.

The basic analogue principle is the concept of fixed frequency division generated by a chain of switch-controlled oscillation [4.20]. This model has been extended, through the use of two properly interleaved topologies, to cover the implementation of multiple ratio frequency dividers.

The design procedure based on the use of the equivalent circuits has been retroactively applied to the proposed dual-modulus prescaler developed in the frame of the current work, demonstrating the potential for use as a reference model to synthesize dual modulus digital dividers. An interesting equivalence between the proposed model and the basic logic SCFL cell has been also demonstrated. This equivalence could be easily extended to serve also for other logic families. Therefore the reference model could be used as:

- A unifying approach to study the behavior of analogue and digital frequency dividers;
- a design method for dual-modulus frequency dividers;

- Justification for the application of simulation tools conceived for analogue injected oscillators and frequency dividers to digital frequency dividers.

Once the design of the circuit was completed, HB and phase noise analysis were performed on the complete circuit proving the usability of these simulation tools to the design and analysis as an effective mean to reduce the computational time towards the steady state solution. Simulations carried out to characterize the divider phase noise performances, including the complete circuit with the inclusion of individual noise sources in the transistors, allowed to additionally identify some limitations associated to the lack (or the limited validity range) of accurate non-linear noise models which should be subject of further research.

Detailed behavioral modeling was outside of the scope of the research, but working backwards and doing behavioral modeling of the frequency divider would be an interesting continuation of the work as this could be quite useful for more accurate synthesizer phase noise simulation.

4.5.2 **Analogue Frequency Dividers Simulations**

Analysis of analogue frequency dividers is based on the solution of a circuit with a reduced number of non-linear devices with harmonic excitations, and it is solved in the frequency domain. Frequency division arises as a valid solution of the non linear circuit with proper harmonic stimulus.

Independently on the principle of operation (injection locked [4.7], regenerative [4.8] [4.9] or parametric [4.10]), when the HB simulator is used it needs to be properly initialized to converge to the desired solution. In fact, even knowing that a circuit is capable (in theory) of generating a periodic output signals whose frequency is a fraction of the corresponding input signals, and providing the HB tool a frequency base which includes the divided solution, we would always find the trivial solution (i.e. the non-oscillating mathematical solution with all the node voltages equals zero at the divided frequency, which, even if unstable in reality, is the simplest found by the simulator). Several procedures have been proposed to solve this problem and help the convergence to the desired solution.

In [4.11] and [4.12] an auxiliary voltage generator (AG) at the divided frequency is inserted at a relevant node of the circuit and the overall circuit response is optimized until the effect of the auxiliary generator is null to solve for a valid non trivial solution. For the e AG the non-perturbation condition is given by the zero value of the ratio Y_{AG} between the current flowing through the AG and the delivered voltage (i.e. when the signal provided by the AG equals the steady state oscillating solution). For the details of these techniques the above references provide an exhaustive explanation.

Another method (already applied to basic digital dividers) uses an auxiliary sub-harmonic circuit (ASC, [4.6]) to initialize the frequency components of the circuit variables to non-zero values allowing the application of the continuation method. This method can be easily understood considering by referring to the operation of a feedback inverter. A high impedance inverter with a sloped transfer characteristic can be used to simulate oscillations in the frequency domain. As the node impedance is high and the associated current flowing into the node will be low, the AG with admittance probe is not suited to simulate the oscillation as the associated optimization process would be difficult, whereas the ASC connected via a variable resistor (R_{var}) imposing the proper initial condition can better serve for the purpose (Figure 4.24).

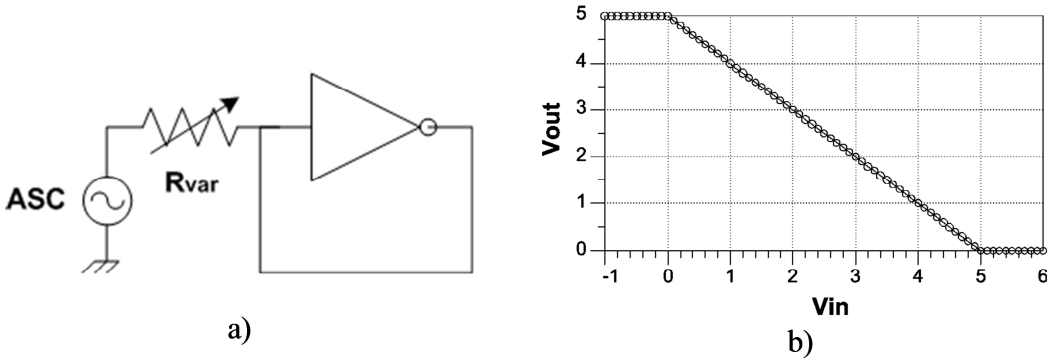


Figure 4.24: a) Ring oscillator schematic for simulation with ASC, b) Static response of the inverter used in the simulation

With the ASC connected to the circuit, a HB simulation is performed sweeping the continuation parameter from very low to very high values. For low values in the sweep, the solution provided by HB has necessarily nonzero values (as imposed by the ASC frequency and amplitude). As the resistor value increases the ASC as a smaller influence on the circuit response. Actually, for the largest values of in the sweep (10^{10} for example), the ASC is open circuited and has no effect at all on the circuit behaviour,

as in any standard continuation method, and the solution of the HB simulation represents the steady-state.

In Figure 4.25 the convergence of the method for this basic example is demonstrated by plotting the amplitude of oscillation versus the swept resistance value, proving that the non-trivial solution survive even when the ASC is open circuited and has no effect on the circuit. In such ideal case the limitations of the frequency domain analysis come only from the number of harmonics used to reproduce the square waves of such strongly non linear system.

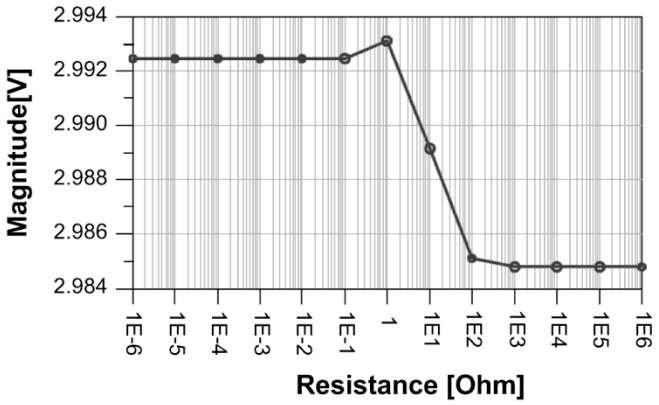


Figure 4.25: Magnitude of the fundamental tone versus swept resistance values.

A different simulation tool (transient-envelope) combines time simulation to initialize the frequency base of the harmonic balance [4.13]. The use of transient envelope in analogue frequency dividers has been proposed in [4.14]. With this technique, it is possible to use a transient seed to initialize the divided solution in support to the convergence to the proper solution, but to our knowledge, no application to digital frequency has been proposed to date.

4.5.3 **Digital Frequency Dividers Simulations**

In digital dividers the number of non-linear devices is large. Moreover, a high number of harmonics is required for accurate characterization of the digital excitations (normally square waveforms). These factors increase the computation time and in some cases prevent the convergence of HB tools in favour of transient analysis. However, transmission line effects could not always be included in time domain simulations because they tend to slow (and in some cases also prevent) convergence. This represents

a serious problem for frequencies above ~3 GHz where the presence of the interconnection lines affect substantially circuit's performance.

Considering the basic digital divider circuit used as a starting point for the design as a pure RF circuit it would be quite difficult to understand its behaviour. However, the logic analysis presented in chapter 3 showed how, with the inverted output fed back to the input and only one between master and slave active during a clock edge, multiplication by 2 of the clock period can be easily understood. Frequency division could be interpreted as the consequence of the specific logic configuration. The circuit substantially count pulses at its inputs and after a fixed number of them, triggers a pulse at the output resulting in frequency division. It is thus possible to establish an input/output relationship (non-linear and with memory) based on the logic behaviour or determine a sequence of finite states, independently on the rigorous characterization of the non linearities that build up the circuit.

An interesting method to explain analogue frequency division is presented in [4.20]. It uses a chain of inverters arranged in a ring configuration interleaved with transmission gates. In this work this concept has been extended to understand the operation of digital frequency dividers in general, to relate them with their analogue counterparts, allowing the application of the same simulation (HB) tools. It is important to stress that the equivalent circuit of the digital divider is not proposed as a way to simplify or speed-up HB and phase noise analysis, however this equivalence could be turned into a method to synthesize dual-modulus dividers based on the combination of two fixed ratio consecutive order (N, N+1) dividers. Based on this simple equivalent operation principle, it is presented how HB phase noise and also Envelope-Transient simulations, could be effectively used also for the design of digital dividers.

4.5.4 Equivalent Topology: The Dynamic Divider as a Switched Ring Oscillator

If the output of a logic inverter with a given propagation delay is fed back to its input, an instable system is formed and it will tend to oscillate. This constitutes the basic principle of the well-known ring oscillator. The same happens cascading an odd number of inverters (buffer stages are normally included to sustain oscillation, which some drawbacks on the maximum operating frequency). Propagation delay through the cell

sets the time duration of the "*contradictory logic state*", in which inverter input equals inverter output. A rigorous procedure to estimate oscillation frequency of this type of circuit can be found in [4.21] whereas specific methods for the simulation of such circuits have been proposed in [4.22] and [4.23].

The ring oscillator topology can be extended to implement a dynamic divider through the inclusion of switches in the inverter chain, what we have called a *Switched-Ring Oscillator*. A feedback structure of inverters and switches (or transmission gates) in a closed loop configuration is often referred to as a dynamic frequency divider ([4.20], [4.25]), even if analogue regenerative frequency dividers are also sometimes called "dynamic" [4.24].

One inverter in the loop is enough to explain circuit behaviour even if the same apply for an odd number of inverters. The introduction of switches in the inverter feedback loop prevents the oscillation as it breaks the feedback loop. To work as a divider, each consecutive switch in the chain should be driven by out-of-phase replicas of the input frequency (F_{in}).

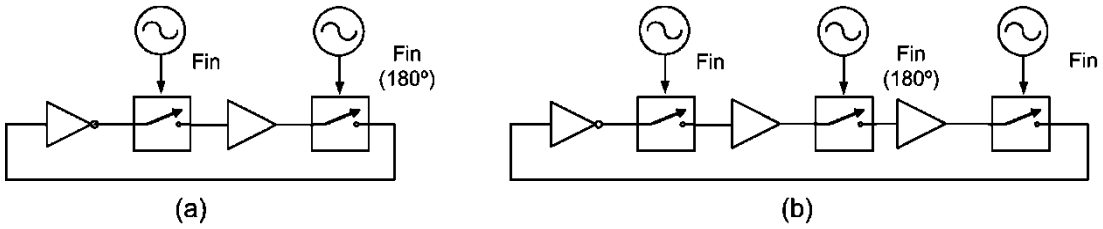
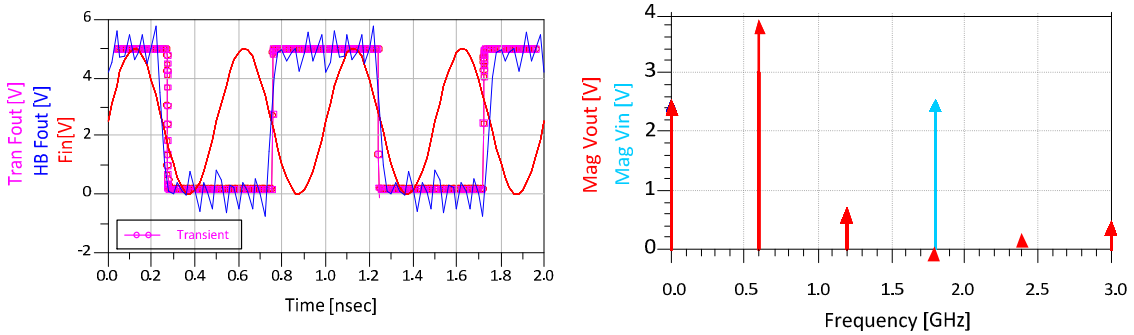


Figure 4.26: Block diagram of a divide by 2 (a) and divide by 3 (b) dynamic frequency dividers.

In the circuits of Figure 4.26 the time required for the signal to propagate across the loop is determined by the period of the clock which drives the switches, in addition to the inverter delay. In the case of two out-of-phase switches (a), it will take two clock periods for the change in state to propagate through the chain, and frequency division by two is achieved. This principle of operation could be applied to any number of consecutively out-of-phase driven switches. In Figure 4.26 (b) for example, three cascaded switches require three half periods of the input clock for the complete propagation of the signal edge through the chain. Therefore, the complete period of the loop signal is three times the period of the driving signal, hence dividing by three.

In Figure 4.27 time waveforms (a) and HB spectrum (b) corresponding to circuits in Figure 4.26 are shown.



(a) (b)

Figure 4.27: Simulations of ideal circuits in Figure 4.26:(a) Simulated input and output (HB solution with ASC and 17 harmonics superimposed to transient solution) waveforms for a divide-by-two frequency divider. (b) Simulated (HB) input and output spectrum for a divide-by-three frequency divider

In a loop with one inverter and N switches, the maximum input frequency which can be divided by N is roughly N times the self oscillating frequency (i.e. when all the switches in the loop are "on" and the circuit behaves like a ring oscillator). On the other hand, there is a minimum frequency of operation, which is set by the discharge time of the buffer stages [4.25]. Self-oscillation of the ideal divider with all switches "on" does not implies that the corresponding divider circuit will self-oscillate at that frequency. It would depend on the topology chosen to implement the switches. If transistors were used as transmission gate switches, self oscillation would be prevented as the switches are "*off*" in absence of input signal thus breaking the feedback loop [4.20]. Presence or absence of self-oscillation in a digital divider makes the difference in the procedure to be applied with the HB simulation techniques. In the first case the circuit has to be analyzed as injected oscillator with a certain synchronization range, while in the second the circuit has to be treated as a regenerative divider.

In our case, as the multilevel differential SCFL D-FF implementation of the divider is prone to self-oscillate, the principle of switched-ring-oscillator frequency division can be applied to explain its behavior.

In the simplified schematic of Figure 4.28 (a), the two levels of transistor can be associated to the clock and data levels in a multilevel SCFL topology (output buffering not included).

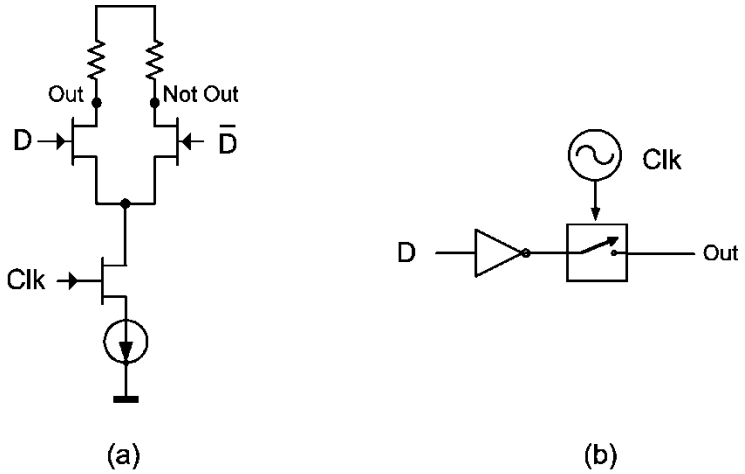


Figure 4.28: (a) Simplified SCFL cell; (b) Ring-oscillator divider cell.

Applying complementary signals to the upper level transistors, and clock to the lower level, a switched mode of operation driven by the clock signal is implemented. As a high logic voltage state at both D and Clk is required to drop the voltage in the load resistor (similarly would be the case for a second cell if driven by complementary signals), it is straightforward to establish the equivalence with the basic ring-oscillator divider cell in Figure 4.28 (b). Two of these cells could be cascaded to constitute a D-flip-flop driven by two out-of-phase Clk and Not_Clk signals (Figure 4.29).

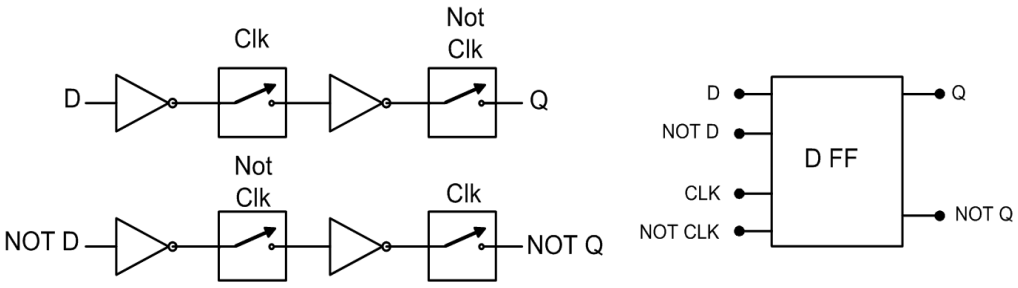


Figure 4.29: Flip-flop with basic cells and its equivalent symbol in differential structure.

As the number of inverters must be odd and two cascaded cells have only two inverters, an additional inverter would be required to close the loop. Working with differential structures (as SCFL) it is possible to avoid this additional delay in the critical path by taking the feedback from the inverted output.

To allow division by 4 and by 3 (our target) in the same circuit, the two respective equivalent topologies should be interwoven. The basic way to implement this kind of dual-modulus division is shown in Figure 4.30.

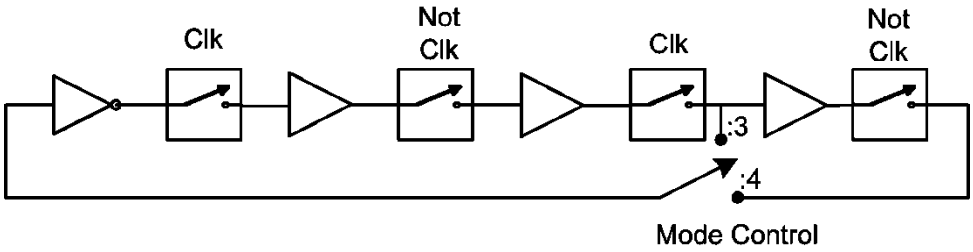


Figure 4.30: Block diagram of the simplest 3-4 dual-modulus divider

This solution has the disadvantage that the feedback loop must be broken to allow the change in the division ratio and the output should be taken from different terminals. Another possibility consists in implementing simple additional logic functions to mask the effect of the last two switching cells, enabling the use of a single output of the complete chain as in Figure 4.31.

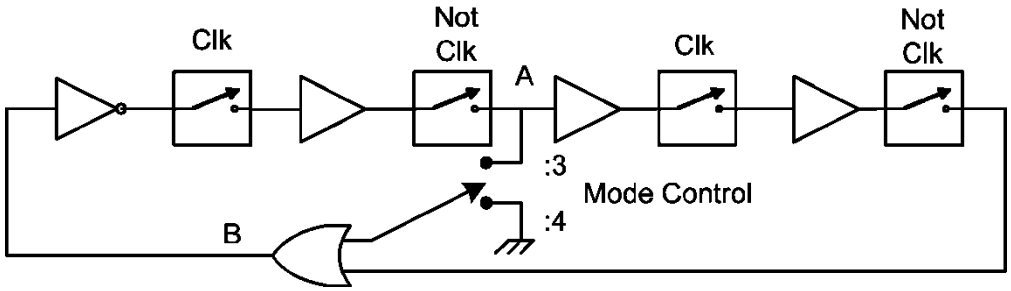


Figure 4.31: Proposed 3-4 dual-modulus divider architecture.

When in divide-by-4 mode, the OR gate is transparent, and feedback takes place as in the fixed ratio divider. In the divide-by-3 configuration, the effect of the last two switches is “bridged” by the OR gate, being equivalent to a single switch, thus forcing the circuit to act as a divider by 3. Given a sequence of logic values or waveforms for the signals at node A, Clk and Not_Clk, it is easy to build the truth table and simulate in the time domain the values of the output signal at node B and compare with the results which would be obtained with the corresponding single ratio divider.

According to the equivalences illustrated in figures 4.28 and 4.29, it could be demonstrated by obtaining the simple truth table, that this solution is equivalent to the architecture proposed in Figure 4.6 and implemented as in Figure 4.7.

4.5.5 **HB and Phase Noise Simulations**

The phase noise HB simulation techniques proposed for digital dividers generally rely on the behaviour of the circuit as injected oscillator. Therefore, prior to phase noise analysis, the circuit has to be simulated in harmonic balance to establish the quiescent point of operation. In general, these simulations have the advantage of being able to provide the steady-state solution and, combined with carrier modulation and matrix conversion techniques, information about the phase noise response, however a major drawback is associated to simulation convergence problems in complex circuits with high numbers of non-linearities.

4.5.5.1 SYNCHRONIZATION ELLIPSES

From an analogue point of view, frequency division-by-3 or by-4 can be considered as the synchronization by injection of a tone at the third or fourth harmonic of the output frequency. This behavior can be verified even in a digital divider, by applying injection conditions after the verification of the presence of the self-oscillation. Waveforms corresponding to the simulation of self-oscillation (in an internal divider node) for the two division modes are plotted in Figure 4.32 for transient and HB simulations, showing a good agreement.

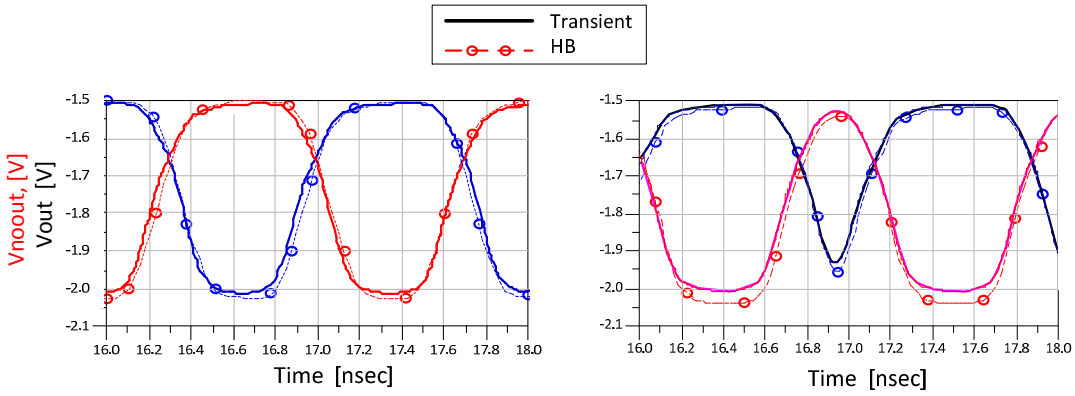


Figure 4.32: Self-oscillation transient (solid line) and HB (circles) simulated waveforms in divide-by-4 mode on the left and divide-by-3 mode on the right.

Once the self-oscillation of the circuit is verified, the describing function approach can be applied to the analysis of its behavior. As the circuit is not formed by ideal (high impedance) inverter blocks, but by finite admittances transistors, the admittance probe

with AG is used [4.12]. For the free-running oscillation, with given amplitude (V_o) and frequency (ω_o), the non-perturbation condition for the AG at an arbitrary circuit node n is given by :

$$Y_{Tn}(V_0, \omega_0) = 0 \tag{4.1}$$

Being Y_{Tn} the total admittance of the circuit evaluated at that node, which allow solving the non-linearity in absence of input signals. To study the behavior as a divider, a single tone with a current source with small amplitude I_g and frequency ω_{in}, and phase ϕ, ($i_g(t) = I_g \,\mathrm{Re}(e^{j(\omega_{in}t+\phi)})$) is injected at the input of the divider, perturbing the free-oscillating condition causing the oscillation to evolve towards an amplitude V_s, and a frequency $\omega_s=\omega_{in}$ /N at an output node. In the presence of the AG, absolute dependence can be considered of the circuit variables on the amplitude and frequency of this generator, thus at ω_s by applying current Kirchhoff law at node n, the following relationship holds:

$$Y_{Tn}(V_S, \omega_S, I_g e^{j\phi}) V_s e^{j0} = 0 \tag{4.2}$$

$_{Tn}$ is the current-to-voltage HB relationship at the fundamental frequency ω_s at the output node n, which accounts for the relationship with the input generator. Direct dependency at the node n is not possible in (4.2) as the generator is applied at the input. Note that the phase at the output node has been set to 0 as the phase of the input generator can be set arbitrarily and the relevant parameter is the phase difference between the two. If I_g is sufficiently small (e.g. very low input power level) V_s tends to V_o and ω_s tends to ω_o, and a Taylor expansion about the self-oscillation point (V_o, ω_o, I_g=0) can be applied:

$$\frac{\partial Y_{Tn}}{\partial V_0}\Delta V_S + \frac{\partial Y_{Tn}}{\partial \omega_0}\Delta \omega_S = -\left.\frac{\partial Y_{Tn}}{\partial I_{gr}}\right|_0 I_g \cos(\phi) - \left.\frac{\partial Y_{Tn}}{\partial I_{gi}}\right|_0 I_g \sin(\phi) \tag{4.3}$$

Where $\Delta\omega_S = \omega_S - \omega_0$ and $\Delta V_S = V_S - V_0$.

Equation (4.3) defines a synchronization ellipse in the plane V_s and ω_s, centered on the self-oscillation point (V_o, ω_o) which identifies the values of amplitude and frequency for which the circuit is able to work as a divider. Only one half of the ellipse (the upper or lower part) can be stable [4.11]. To trace this curve, the HB analysis can be carried

out with an AG placed at a node n, at the frequency $\omega_{AG}=\omega_{in}/N$, with amplitude V_{AG} and phase ϕ_{AG}. Fixing I_g and ω_{in} , ϕ_{AG} can be swept from 0 to $2\pi/N$ to obtain the different points of the ellipse. It would be possible to obtain the same result by sweeping the input generator phase ϕ from 0 to 2π with fixed ϕ_{AG}. In order to fulfill $Y_{Tn}=Y_{AG}=0$, V_{AG} and ω_{in} should be optimized. In the case of a circuit with differential structure, as is the case of the dual-modulus divider under analysis, it was discovered that the way to enable convergence of complex circuits is the use two out-of-phase differential AGs connected to complementary nodes. These dual out-of-phase auxiliary generators may also be suitable for the large-signal stability analysis of any differential and balanced structure. Another useful approach to obtain a valid divided solution based on the same concept is to sweep the input frequency with a fixed ϕ while letting V_{AG} and ϕ_{AG} to be optimized, until a null admittance is reached. In this case open trajectories will be obtained. Points of these trajectories match with stable solutions of the synchronization ellipses (usually its upper half).

When the circuit divides by 3, non 50% duty cycle of the output waveforms requires a small offset in amplitude and phase between the dual auxiliary generators. This effect has been verified with transient simulations and confirmed with measurements.

Synchronization ellipses at the divided frequency in divide-by-4 and divide-by-3 mode, are plotted in Figure 4.33 and Figure 4.34. The result obtained with a frequency sweep at -20dBm optimizing V_{AG} and ϕ_{AG} has been also plotted to verify the coincidence of this method in the stable half of the synchronization ellipse.

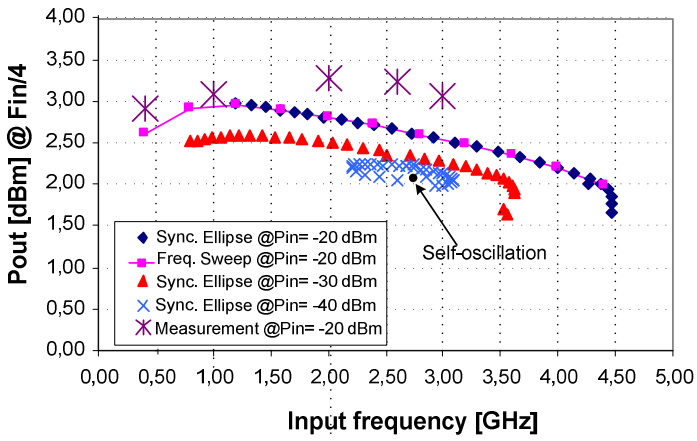


Figure 4.33: Synchronization ellipses in divide-by-4 mode. HB simulations with dual out-of-phase AG at different input power levels and measurements for -20dBm input power.

With higher input power levels the accuracy of the first-order Taylor-series expansion (3) is reduced, this is why those ellipses become open curves containing mainly unstable solution points. A parameter exchange algorithm may be required to close the ellipses or trace the curves (given the infinite slope points at the edges of the simulation curves). At the edges of the synchronization bandwidth and with higher input power levels, high optimization errors and convergence problems also cause the simulator to fail. Measured results for an input power of -20dBm are also reported in the same figure, showing good agreement with the simulations.

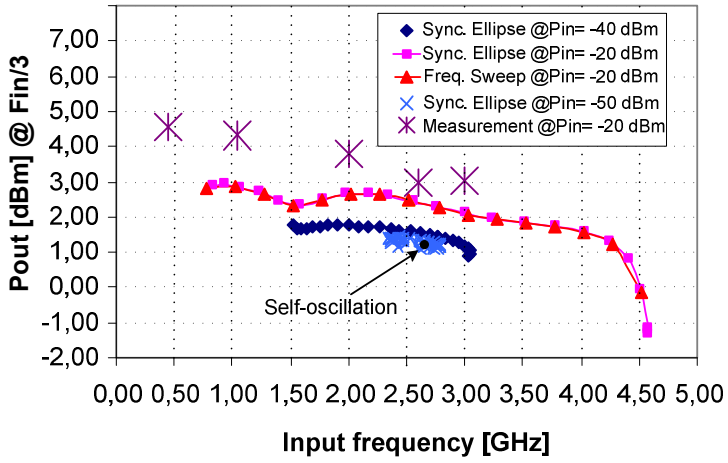


Figure 4.34: Synchronization ellipses in divide-by-3 mode. HB simulations with dual out-of-phase AG at different input power levels and measurements for -20dBm input power.

4.5.5.2 PHASE NOISE SIMULATIONS

Phase noise analysis of digital frequency dividers is commonly studied and simulated at a system level considering the circuits as a single block, from a time-domain jitter perspective [4.19]. On the other hand, different approaches exist for phase noise analysis of analogue frequency dividers ([4.12], [4.27], [4.28]). Phase noise simulation of synchronized frequency dividers can be seen as the extension of the procedure used for oscillators.

In the case of self-oscillation, the carrier modulation approach [4.29] can be applied at low offsets from the carrier, obtaining the sensitivity of the solution frequency to the noise sources.

The matrix conversion approach to non-linear phase noise [4.30] is useful to model the converted noise from the input source in the case of frequency division and to fit phase noise measurements far from the carrier, with or without external injection. It may be computed using HB analysis with noise controllers [4.31]. Matrix conversion phase noise calculation can be described with equation (4) [4.12]. It represents the sideband phasor of the voltage at the output $\Delta V_p(\Omega)$ as a function of the conversion matrices M_{pk} and the noise sources vector $N_K(\Omega)$, Ω being the offset frequency, k the index of noise sources and p the index of noise generated sidebands.

$$\Delta V_p(\Omega) = \sum_k M_{pk}(\Omega) N_k(\Omega) \tag{4.4}$$

In the case of free running oscillators carrier modulation and matrix conversion approaches reproduce measured phase noise values with reasonable agreement.

In the case of frequency division, an improvement in the input signal phase noise proportional to the square of the division ratio is ideally expected at the output at least in a range of offset frequencies around the divided carrier. In practice lower values are observed due to the noise contribution of the divider itself. Noise sources can be modelled in the self-oscillation case, and then used when frequency division occurs with appropriate input signals and their corresponding phase noise data. In the following simulations, as the built-in thermal noise models from the foundry library were not capable of reproducing the phase noise performance, basic 1/f sources (4.5) in parallel with white noise sources were added between drain and source in each transistor model. Noise current density is proportional (by a factor K) to the DC current (I_{dc}) of the transistor and inversely proportional to the frequency (f). Two exponents for the current (I_e) and the frequency (f_e) allow some flexibility in fitting the model.

$$\left\langle i^2 \right\rangle = \frac{KI_{dc}^{Ie}}{f^{fe}} \tag{4.5}$$

This model has been used to test the simulation tool, but it is very simple and may not be sufficiently accurate to emulate the phase noise contribution of the divider without injection (self-oscillation) and with low, medium or high levels of injected input signal at different offset frequencies across the entire band of operation. Nevertheless, accurate modelling of noise sources was beyond the scope of the work.

The phase noise simulation of the digital frequency dividers based on HB assumes that the main contribution to the output phase noise is associated to the phase of the fundamental output frequency. This is in agreement with the conventional procedure to measure phase noise with spectrum analyzers. As the harmonic content of the output signal increases, jitter contributions of higher harmonics should be included.

Phase noise measurements and simulations splitting PM and AM contributions are plotted in Figure 4.35, together with input generator noise divided by 4, with a 2.4 GHz input signal of -20dBm power.

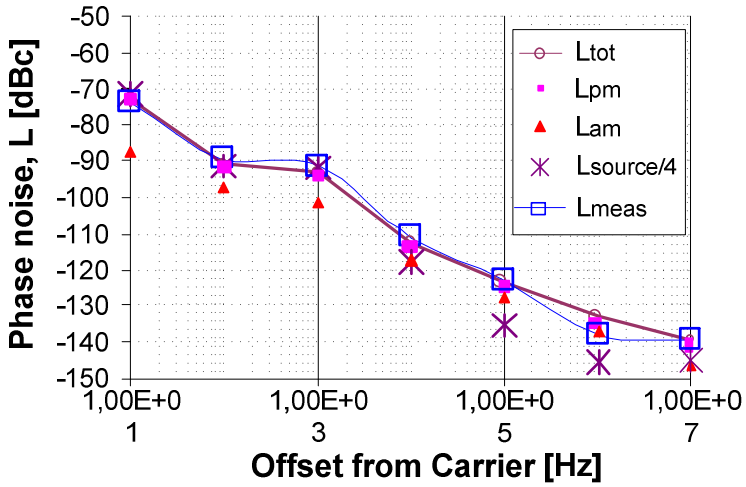


Figure 4.35: Phase noise measurements (L_{meas}) and simulations for a 2.4GHz, -20 dBm input signal. Total phase noise (L_{tot}) and individual contributions are indicated as AM, PM, and phase noise of the ideal divider (input generator noise divided by 4).

Measurements of the frequency divider contribution to the total phase noise at the output may be difficult to make, depending on the quality of the input generator. Set-ups to remove the input generator contribution are proposed in [4.19] and [4.32]. In our case, direct measurements were used: with the phase noise of the input generator accurately characterized, an ideal (noiseless) divide-by-N circuit would simply provide the divided input phase noise (i.e. a reduction of 20log(N)). To represent the frequency divider contribution (residual noise, [4.32]), the ideal divide-by-N phase noise response to a known input phase noise (measured from the input generator) was subtracted in (dB) both from measurements and simulations of the total phase noise at the output (4.6), and the resulting deviation from ideal behaviour evaluated versus offset frequencies.

$$Dev_{meas/simulated}(f) = L_{meas/simulated}(f) - \left(L_{input\_generator}(f) - 20\log(N)\right) \qquad (4.6)$$

In Figure 4.36 are plotted the results for 3 GHz input frequency, division by N=4 and a -20dBm input tone at different frequencies.

Phase noise deviation from the ideal divider is usually positive, indicating the addition of phase noise by the divider. A negative value would mean an improvement in the phase noise behaviour. The shape of measurements follows simulations mainly at low offsets. This can be easily explained taking into account that the additional noise sources modelling focussed mainly on small and medium offset frequencies. However, noise converted from the input is mainly responsible for output phase noise shape at smaller offset frequencies, while at higher frequency offsets the phase noise is substantially dominated by the phase noise of the input signal.

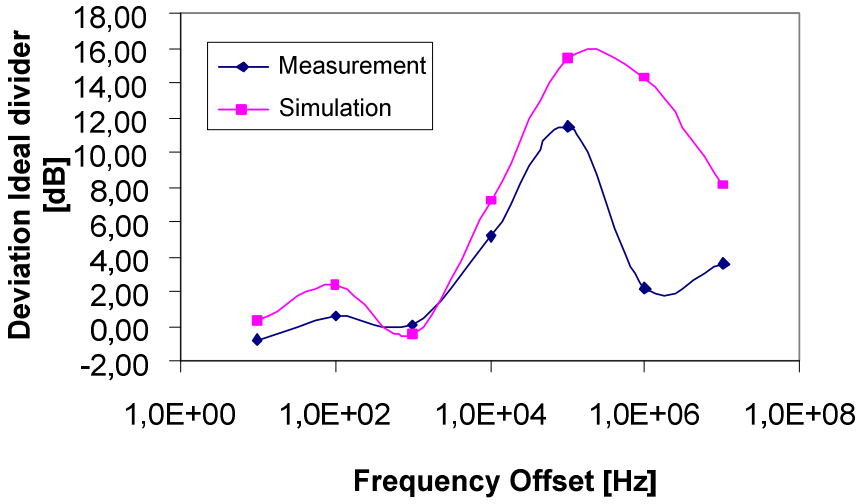


Figure 4.36: Simulations and measurements deviations of the noise contribution from ideal divider by 4 (measured input source through an ideal divider) for a -20 dBm input signal @ 3 GHz.

No significant difference was found between division by 3 and by 4 in terms of phase noise order of magnitude. Apart from limitations in the built-in noise model, some improvement was achieved with the use of added noise sources, but there is still room for improving accuracy throughout the range of offset frequencies and this could be subject of further research.

4.5.6 **Transient Envelope Simulations**

Envelope-Transient is based on the expression of circuit signals in terms of a Fourier series with time-varying phasors of limited bandwidth (eq. 4.7):

$$x(t) = \sum_{K} X_K(t) e^{j\omega_K t} \tag{4.7}$$

In all cases where this method is applied, one or more high frequency carriers (ω_K) and time-varying low-frequency envelopes ($X_K(t)$) are present. The high frequency components are analysed with HB, providing results in the frequency domain, while the envelope phasors are analyzed in the time domain. A detailed description of Envelope-Transient capabilities for the analysis of autonomous circuits is out of scope of the present work and can be found in [4.33]. Considering digital frequency dividers as injected oscillators, some of the concepts described have been also applied to the analysis of a digital divider for the first time.

The divided solution can be initialized with a source, connected to the circuit only during a transient time, acting as a seed, and then disconnected. This was implemented with an AG connected to the circuit through an increasing time variant resistance. In such a manner, once the highest value is reached, the AG is virtually disconnected from the circuit and the system is free to evolve towards its natural solution according to its own dynamics (if the solution is stable, the system will evolve to it after removing the AG). By applying this procedure without an input signal, self-oscillation can be checked.

As the self-oscillation frequency value cannot be known with accuracy a priori, some offset error in the choice of the frequency base of the envelope analysis can be compensated by leaving enough bandwidth for the self-oscillation to take place showing a frequency shift and some transient behaviour, as can be seen in Figure 4.37 for the case of division by 4 with an offset error of 40.93MHz. Minimum frequency and envelope bandwidth must be carefully chosen to allow some flexibility in the evolution of the simulations towards valid solutions without loss of accuracy.

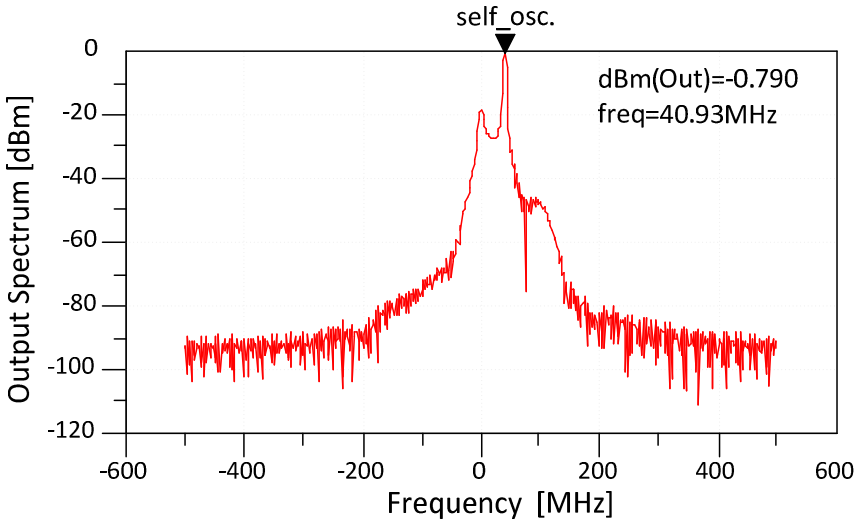


Figure 4.37: Transient envelope simulation of self-oscillation shows a frequency offset between proposed fundamental frequency and effective solution

Convergence of the divided solution and the change in the division ratio can be seen in Figure 4.38 as explained below

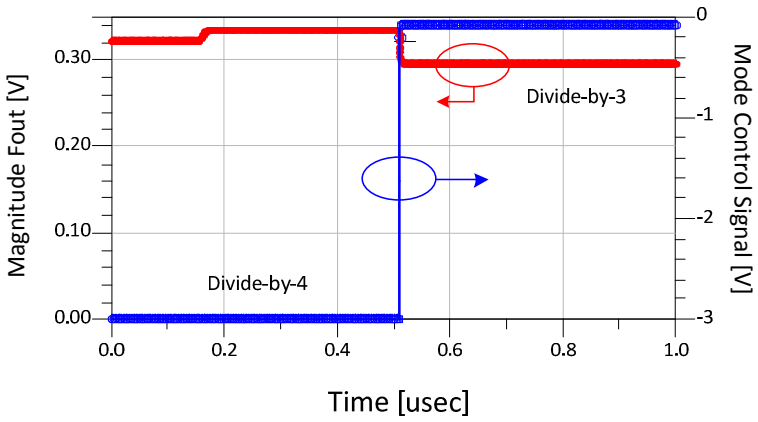


Figure 4.38: Evolution of the magnitude of the output fundamental frequency. (The mode control signal has been superimposed).

As the frequency base in transient-envelope simulation is fixed, in order to check the change in the division ratio the output frequency should be kept constant while changing the input frequency (e.g. by simultaneously switching between two generators while changing the division ratio). The evolution of the magnitude corresponding to the output fundamental frequency is plotted versus time together with the corresponding mode control signal. Simulation starts in divide-by-4 mode with the help of the AG and then changes to divide-by-3. The two discontinuities in the magnitude of the output signal corresponds firstly to the non perturbation condition reached by the AG (the

division is sustained as the magnitude of the output signal at the divided frequency is still non-zero), and then to the change in the division ratio. The latter can be associated to the change in the duty cycle of the output waveform, which implies a change in harmonic content, hence in the output power of the divided output (Figure 4.39).

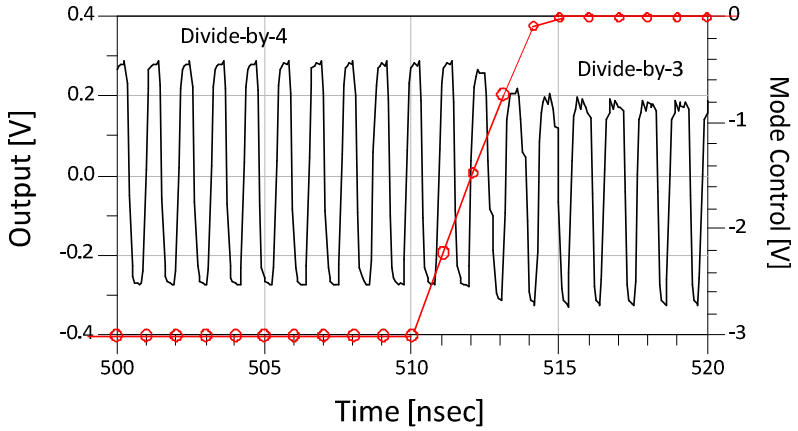


Figure 4.39: Evolution of the output waveform during the change in the division ratio.

4.6 CIRCUIT IMPLEMENTATION

The complete block diagram of the circuit is shown in Figure 4.40.

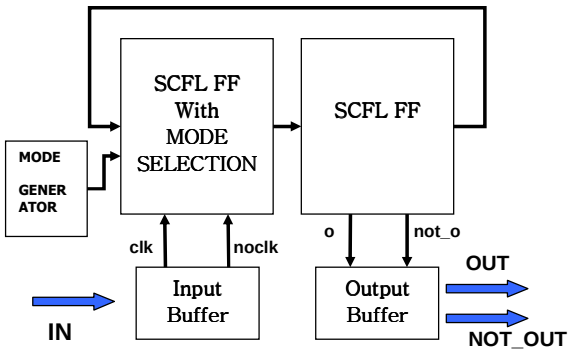


Figure 4.40: Block diagram of the whole circuit

The ircuit, fabricated with the OMMIC ED02AH technology is shown in Figure 4.41. Capacitors have been added at the nodes in which bias lines are shared between different sub-circuits c to improve stability. The microstrip lines lengths have been adjusted by way of meander lines to guarantee that each couple of complementary signals travels exactly out of phase, thus ensuring the correct behaviour of the circuit.

Grounded resistors are present in each line which connects a transistor gate to a bonding pad, to avoid electrostatic discharge problems due to the manipulation of the chip during the assembly. A Process Control Monitor (PCM) transistor has been also placed within the chip (bottom right) to control the value of all the process parameters and allow discarding of eventually non-compliant chips.

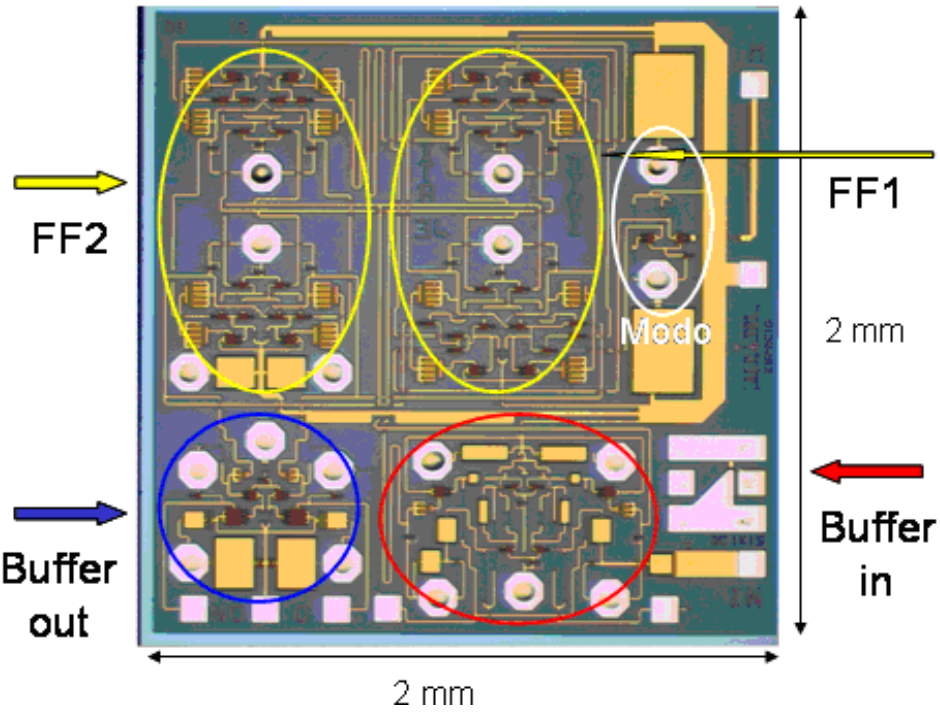


Figure 4.41: Microphotograph of the dual modulus divider with details of the main building blocks

In order to facilitate the characterization the circuit has been packaged in a 16 pin gull-wing ceramic package (Figure 4.42) and assembled on a Polymide PCB with input/output microstrip lines and coaxial connectors (Figure 4.43).

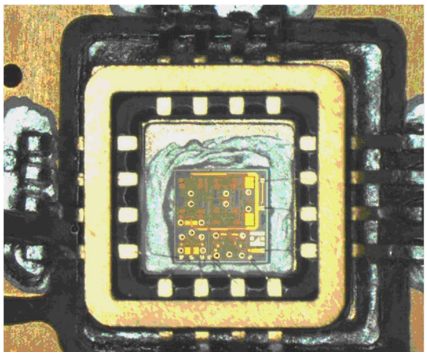


Figure 4.42: Detail of the prescaler packaged in the 16pin ceramic package

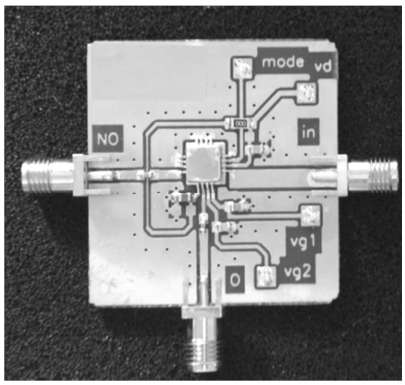


Figure 4.43: Photograph of the packaged circuit assembled on the Test PCB

4.7 MEASUREMENTS

A summary of the main measurements carried out on the fabricated divider are illustrated in the following figures. The prescalers has been adjusted to draw the nominal 75mA from the +3.5V nominal supply voltage (~ 260mW), that is about 40% less power consumption with respect to the previously implemented fixed ratio divider.

By comparing the power consumption figures with CMOS implementations, the value is one order of magnitude higher. However it is worth mentioning that more than 40% of the consumption is associated with the input/output buffers and the modulus control signal generator and that the technology limitation affect the heavily the power consumption. The measured output power varies between 3±1 dBm for each output and division ratio, for input frequencies up to 4.5 GHz. The voltage swing at an external 50Ω load was more than 2x350mV$_{PP}$. The overall wafer yield was more than 70%.

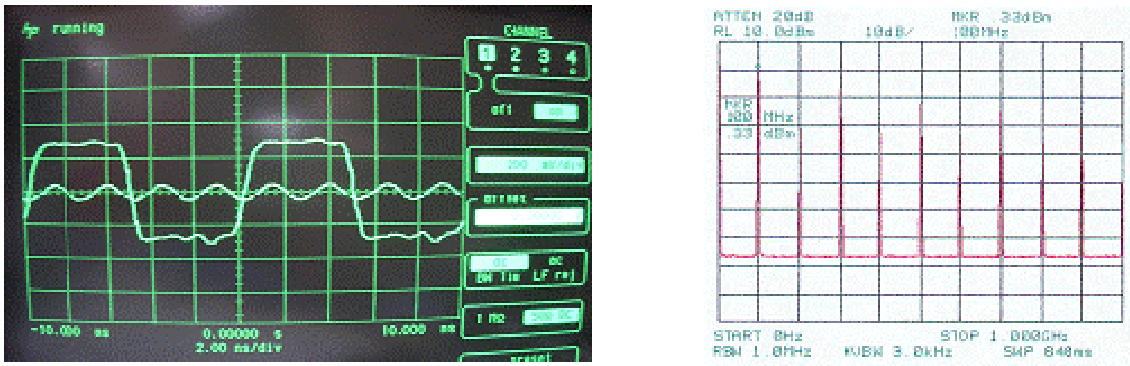


Figure 4.44:Input/Output waveforms (left) and output spectrum (right) for Fin=400MHz and division-by-4.

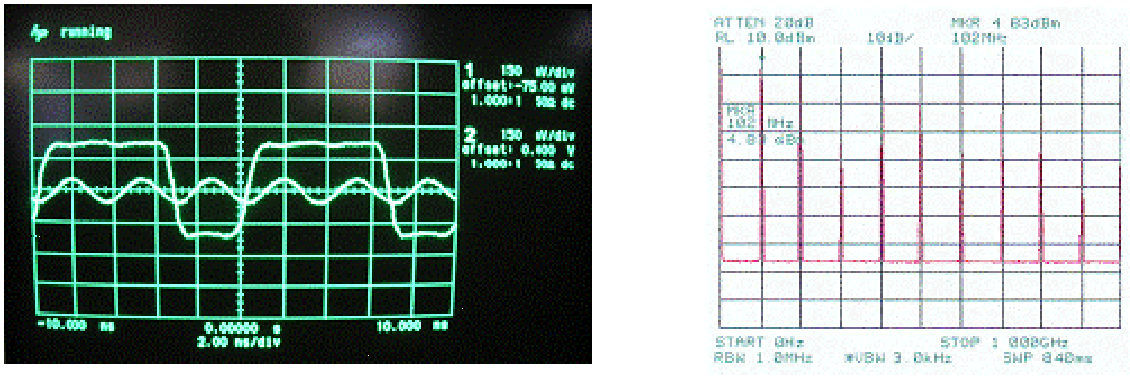


Figure 4.45:Input/Output waveforms (left) and output spectrum (right) for Fin=400MHz and division-by-3.

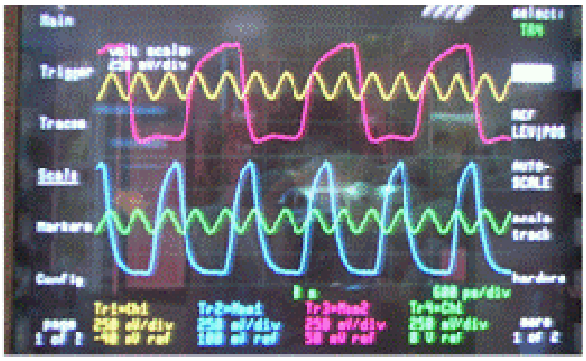


Figure 4.46: Superimposed Input/Output waveforms for the two division ratios at an input frequency of 2.5GHz

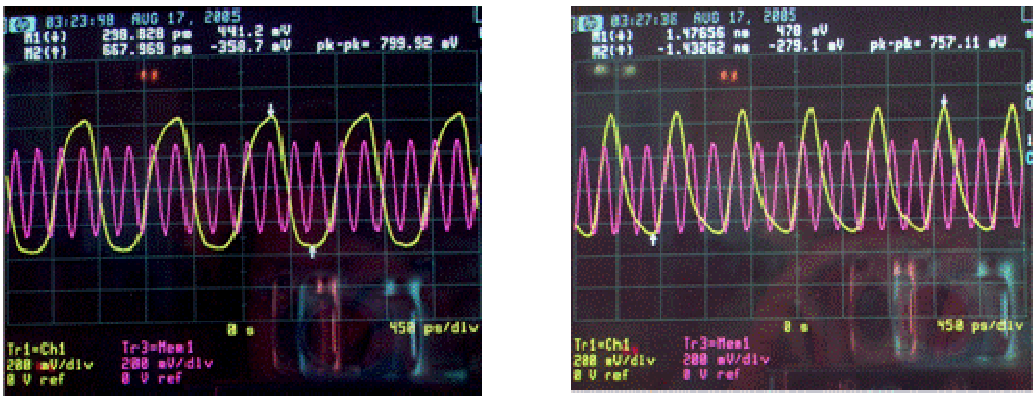


Figure 4.47:Input/Output waveforms for Fin=4.5 GHz and division-by-4(left) and by 3 (right).

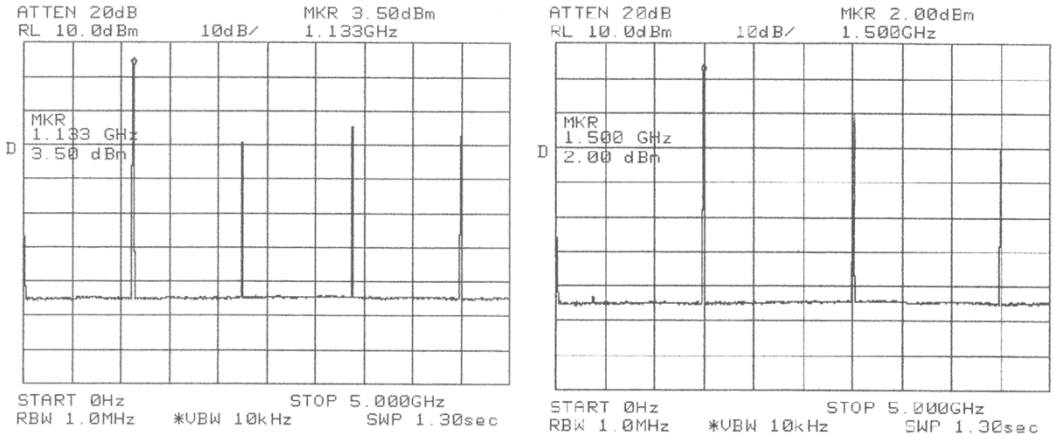


Figure 4.48 Output spectrum at divide-by-4 (left) and divide-by-3 (right) operation Fin=4.5 GHz

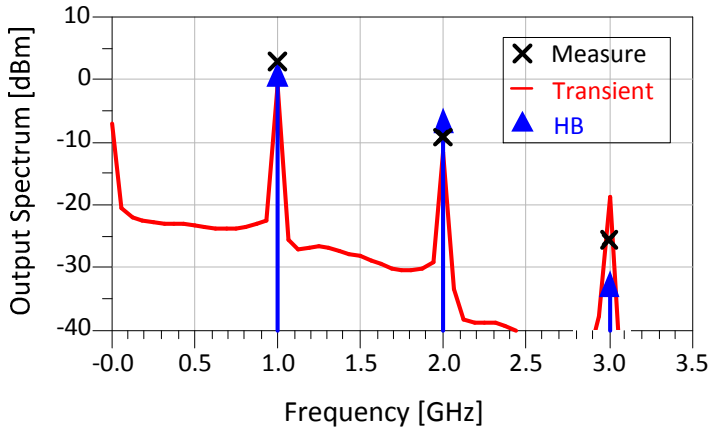


Figure 4.49: Output Spectral content predicted by transient and HB simulation compared with measurement for an input signal at 3 GHz with Pin=-20dBm.

Spectral content at the output as predicted by HB and transient simulations has been compared with measurements for a -20dBm input signal at 3GHz in division-by-3 mode showing good agreement (Figure 4.49). No relevant differences have been found between division by 4 and by 3.

Phase noise measurements were also carried out on the divider, and the results have been reported (and compared with simulations) in section 4.5.5.

Engineers working in frequency synthesis would immediately note the excessive noise levels of the selected divider as the noise is typically 25 dB lower in HBT devices (at 100 KHz) mainly because the higher flicker corner frequency in GaAs PHEMT. However it is important to stress how the phase noise requirement of the prescaler were sufficient for the application (hence the technology selection toward a low noise

PHEMT to achieve an optimum trade-off for all the circuits to be developed), and the results obtained fully meet the overall specifications using large (bigger than 50kHz) PLL cut-off frequencies to achieve the sub-1degrees targeted PLL performances. With requirements for minimum added phase noise or limited DC consumption, other technologies such as SiGe HBTs in ECL topology would be advisable.

In Figure 4.50 the measured input sensitivity for the two division ratios is plotted. The circuit has a frequency operating range from below 100MHz to more than 4.5GHz with a very wide sensitivity window.

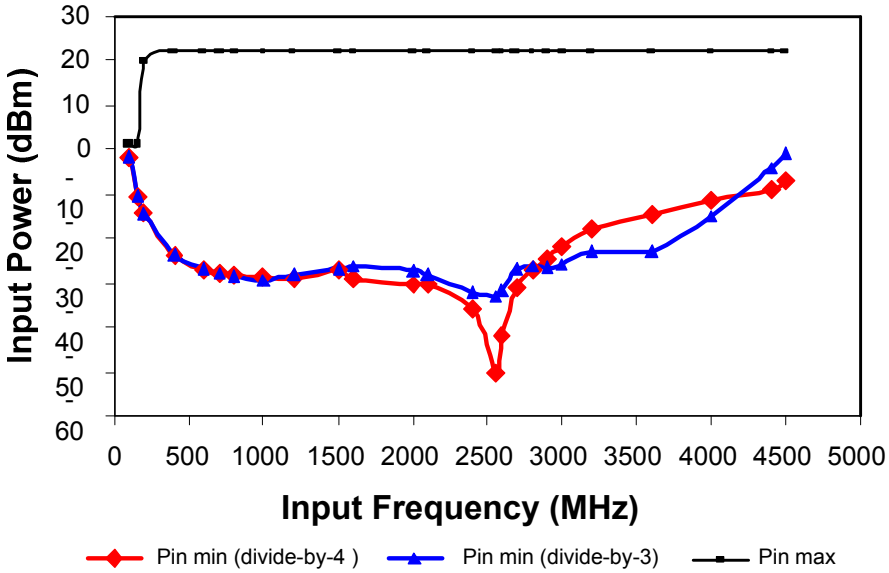


Figure 4.50: Dual modulus divider input sensitivity and maximum input power

It has to be noted that the goal of the design was not to achieve the highest input frequency of operation, but was optimized for this particular application (self-oscillation around 650MHz, good behavior for input frequencies below 500MHz, current density of the transistors in the D-ff lower than 0.4mA/μm^2 due to space de-rating requirements, and good reliability).

Higher values of maximum input frequency could have be obtained with the selected technology, if no constraints were imposed by the specifications on device size and current density at which can operate the transistors.

Good agreement with the simulation can be observed by comparing the value of the peak in sensitivity close to the simulated values (Figure 4.51). Minimum required input power is higher than the value predicted by simulations. Deviations in the technology

process, in the bias point, underestimation of parasitic effects and nonlinear models inaccuracy could be accounted for it.

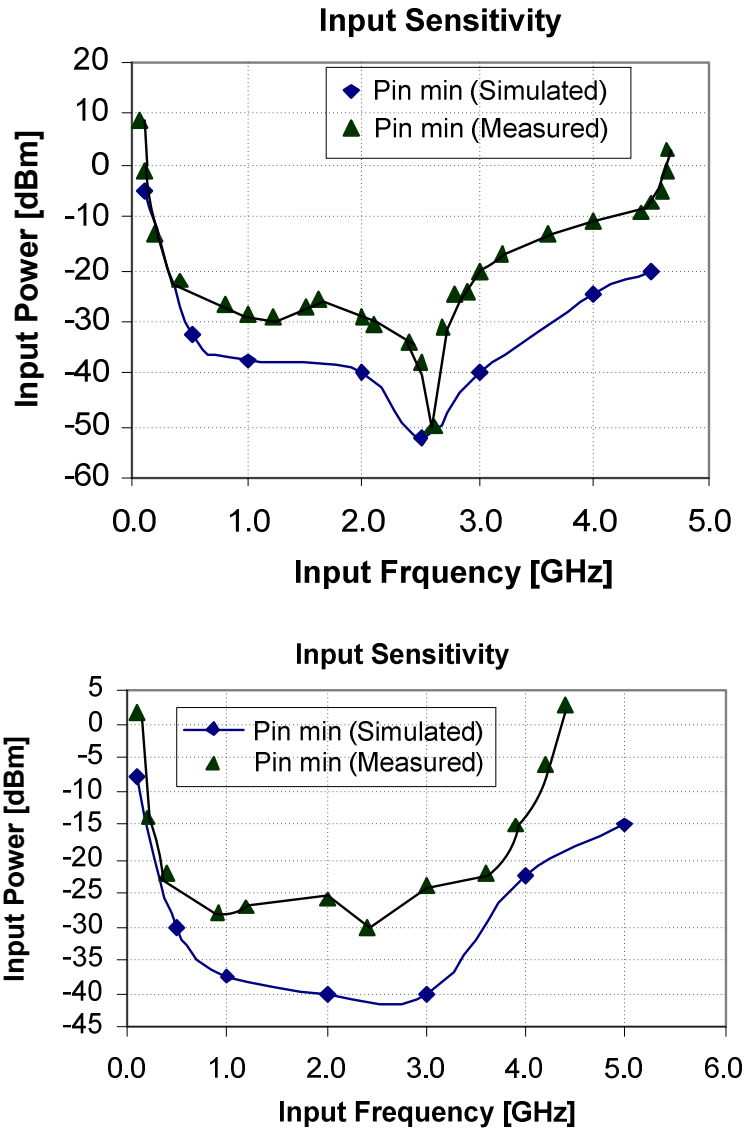


Figure 4.51: Comparison between simulated and measured sensitivity in the two configurations of the prescaler (Note that the scale on the y-axis is different in the two graphs)

In order to validate our design strategy for the implementation of the dual modulus prescaler, the measured sensitivity has been compared with the one achieved with the basic divider-by-four circuit from which the prescaler has been derived. In Figure 4.52 is clear how the maximum operating frequency is almost the same in both the cases, hence confirming our initial considerations and confirming that this topology

could be conveniently used as a building block in the design of high speed dual modulus prescalers.

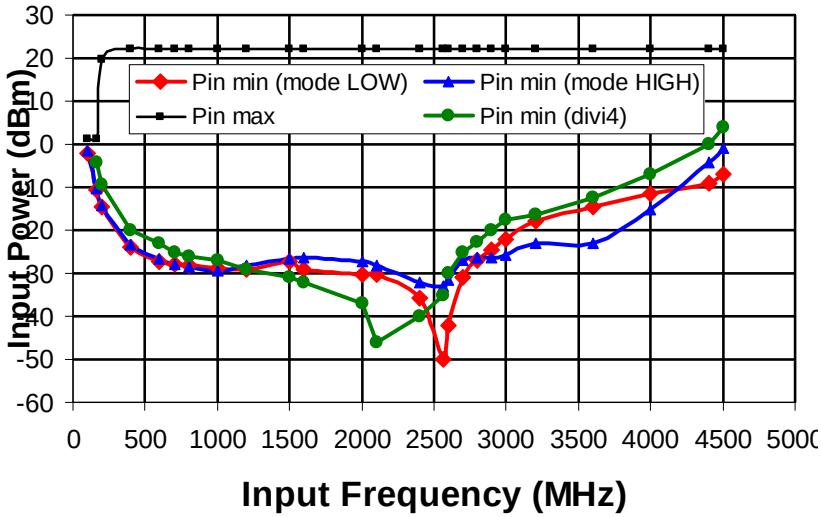


Figure 4.52: Comparison between dual modulus prescaler sensitivity (mode LOW and HIGH))and divider by 4 sensitivity (divi4).

4.8 FLIGHT VERSION

Based on the successful implementation of the prescaler, the circuit was further optimized to match with the system requirements and make it fully compliant with requirements of the targeted space mission. Details of the improvements will be given in chapter 5 even if a full characterization was carried out only at Alcatel premises.

4.9 CONCLUSIONS

In this chapter we the design of a novel dual-modulus divide-by-3/divide-by-4 prescaler topology has been reported. The topology is in principle capable to overcome the speed limitations of conventional dual-modulus dividers. Unnecessary flip-flops and logical gates are completely removed from critical paths, being the maximum allowable speed determined only by the basic fixed ratio divider circuit from which it has been derived.

The newly proposed topology has been described in detail and the modifications with respect to conventional topologies have been explained allowing its application to any kind of dual-modulus divider.

Additionally, a digital frequency divider model based on the "switched ring-oscillator" concept, suitable for dividers with even, odd, fixed and variable division ratios has been described. A simple procedure to design a dual modulus prescaler combining the topologies of two consecutive order dividers has been outlined and applied to the proposed circuit. Both HB and Envelope-Transient tools have been applied to the final circuit to validate the proposed approach, showing good agreement with the measured performance.

Phase noise simulation of digital frequency dividers based on their previous HB simulation has also been presented. The method, using a full non-linear and noise model of the individual transistors, has been justified by the previous approach to explain how digital frequency dividers can operate as injected oscillators. The proposed method provides a test bench to develop accurate modeling of noise sources. In addition, a dual out-of-phase auxiliary generator has been proposed as an HB tool for the analysis of balanced and differential circuits. Finally, Envelope-Transient has been used, for the first time to the authors' knowledge, to analyze digital frequency division mechanisms and the change in the division ratio of a dual-modulus dividers.

The circuit has been implemented in a custom GaAs MMIC for space applications. The behavior of the circuit has been checked through an extensive test campaign, validating simulated performances, demonstrating the robustness of the design and the validity of the design assumptions. Measured performance showed an operating window from below 100MHz to 4.5GHz with a total power consumption of 75mA@3.5V and an output voltage swing >2 x 350mV_{pp} with an overall wafer yield was more than 70%

This topology could be conveniently used as a building block in the design of high speed dual modulus prescalers

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5 . A Chip-set for multimode Satellite TT&C transponders

5.1 INTRODUCTION

In this chapter are summarized the design, implementation and testing of a production-oriented RF chip-set to be used in a new generation of multi-mode and in-orbit reconfigurable S-band Satellite Transponders for TT&C applications. Most of the work has been carried out in the frame of the MORFEO project[4] and relies on the several circuits implementations, some of them described in the previous chapters, some new ones, which will be described in this chapter, and some other which have been object of separate research works at the University.

The transponder functionality is to establish a two-way transfer of information between the satellite and the ground. The main transponder functions can be summarized in: tele-command (to allow modification from the ground station of certain spacecraft parameters or on-board configuration), telemetry (the transmission to the ground station of all parameters necessary to know the health status of the satellite) and ranging to accurately measure the distance between the satellite and ground.

The RF hardware section of the transponder is based on a chip-set of GaAs circuits including Multi-Chip Multifunction MMIC modules (MCMM) and custom MMIC circuits, which have been developed and qualified specifically for this implementation.

[4] *Project ref. number TIC2000-0459-P4-03 "Módulos de Radiofrecuencia Monolíticos para equipos embarcados"*

Some of these circuits have been extensively described in the previous chapters (the VGA in chapter 2 and the dual modulus divider in chapter 4) while others have been derived by optimizing the preliminary designs mentioned in chapter 3 (and are not part of the present work). In some cases, custom MMICs have been completely re-designed and will be described specifically in this chapter. Additionally, a subset of circuits have been developed in parallel works carried out in the frame of the same project, and will be briefly summarized for sake of completeness as they have been used to demonstrate the functionality of the complete system.

The active circuits contained in the MMICs include the functions needed for the front-end: a LNA, the RF and IF down-converters, all the Variable Gain Amplifiers (one RF VGA, two IF VGAs), and a variable gain driver stage), the VCO for both, transmit and receive sections, the dual modulus frequency divider and multiplier needed to synthesize the frequency plan. All the chips have been implemented with the OMMIC E/D pHEMT technology described in chapter 3.

Issues such as suitable circuit topology, efficient DC biasing, circuit area minimization, cost-oriented system design and advanced packaging techniques have been addressed during the design. Measurements and yield results from the manufactured circuits will be presented showing that these components, even though especially designed in the frame of the GALILEOSAT contract for the TT&C transponder predevelopment, are suitable for a variety of missions, from Deep space to near Earth, including spread-spectrum transponders with precision ranging function. This is witnessed by their use nowadays in a plurality of space missions.

5.2 EVOLUTION OF TT&C PLATFORMS

During the last twenty years, S-band Telemetry Tracking & Control (TT&C) systems have been demanding transponders with a standard set of requirements corresponding mainly to telecom and military Geosynchronous Earth Orbit (GEO) and 'remote science' programs, but now Low Earth Orbit (LEO) and Medium Earth Orbit (MEO) missions (Earth observation, radio navigation, remote sensing and meteorology) have gained relative importance in the space business due to the increased number of missions (and that GEO and remote science are moving to other frequency bands). Earth

Exploration has now commercial applications and this fact has developed the demand of LEO/MEO satellites.

TT&C in S-Band is an evolving market due to the high concurrency of telecom applications in the S-Band. GEO applications using this frequency range in TT&C have diminished over the last years, being the military telecom satellites the major exception, whereas LEO/MEO satellites represent the largest part of the S-Band TT&C transponders market. However, nowadays some telecom applications in the S-Band are emerging as well, such as the mobile telephony, representing a potential customer for TT&C in S-Band, following ITU's recommendation of common frequency band for both payload and TT&C.

Several factors have imposed new constraints over the TT&C systems. We can highlight some of the most important:

- Higher Telemetry (TM) and Tele-command (TC) data rates demanded by the operators (as current S-Band TT&C transponders from most manufacturers worldwide have rather limited bit rate availability for the uplink);
- The need of a better spectrum use with more efficient modulation schemes;
- The reduced mass, volume and power budget that can be allocated to TT&C in a satellite.

These new missions have a reduced number of instruments and their demand in terms of mass and power is typically moderated. The reduced cost of small platforms makes them more affordable for the limited budgets of a commercial program that need to look over the investment contention to ensure the profitability.

Such applications require new standard characteristics that define a new transponder profile. A large number of satellites is required to provide global earth coverage so the concepts of mini (<500Kg) and micro (<100Kg) satellites are being pushed up to reduce mission costs typically below 50M€. In this sense, mass/volume requirements will have higher relative importance compared to electrical/functional parameters than in previous generations of satellite equipment. Price will also suffer additional pressure beyond its evolution along product life cycle. In addition, the need for optimized use of available bandwidth and for multimode operation capabilities

requires a high degree of flexibility in terms of available functionality and possible configurations.

In order to optimize the usage of allocated bandwidth during the different phases of the mission, LEO/MEO satellites are increasingly asking for multi-mode on-flight configurability. For example, a navigation system like GALILEO defines two operation modes, a *secure mode* handling TT&C Spread Spectrum (SS) signals, and a *standard mode* (STD) with classical TT&C PM-BPSK signals with ESA code ranging system. The PM mode is residual carrier PM with BPSK subcarrier plus a PM pilot for ranging, used to ensure coverage by most ground segment stations as it is more standard. This mode is hence especially convenient for initial orbit injection phases coverage. Additionally, the requirements are different, for example, when the transponder is set to operate in low TM rate (PSK/PM) plus ranging or high TM rate (OQPSK). A third example is constituted by some meteorology systems that are already demanding complex dual-mode operation that should allow both direct to ground TTC links and relayed links via the Tracking and Data Relay Satellite System (TDRSS) Space Network. This multi-mode capability adds a new complexity dimension to the S-band transponder.

LEO satellites do often make use of GNSS receivers for precise position tracking to simplify the transponder design, by eliminating the requirements for coherency and ranging. But this is not a the case of small satellites because the GNSS receiver is an expensive piece of hardware which increased the required mass, volume and power consumption: as many positioning systems still rely on coherent Doppler tracking, ranging capability associated to the satellites is an additional feature which should be maintained.

The new solution which has been developed by Thales Alenia Space España (TAS-E) based on the circuits which are described as a part of this work, is the Integrated S-Band Transponder (ISBT) [5.1], strongly driven by LEO Earth Observation (EO) applications, although easily re-configured for other missions (e.g. : GEO, MEO navigation). The main features of this transponder can be summarized as:

- Compliance to several link standards including satellite relay CDMA links. All applicable known standards are taken into account. 450-SNUG is the reference for spread spectrum modes and ECSS-E-50-05 for the standard modes. Future

standards under preparation like ECSS-E-50-02 (ranging and Doppler tracking) have been considered as well.

- Flexibility in terms of the available modulation formats, bit rates and ranging schemes. Moreover, it will provide on-flight mode switching capability to fit most demanding operational requirements.
- Multi-standard capability (broadband, variable IF and configurable synthesizer) to cut development time down and to reduce reaction time to market evolution.
- Adaptability (a configurable set of power levels, oscillator stabilities and interface compatibility with different platforms).
- Compactness, modularity and a design oriented to simplify tuning, reducing price and delivery time.
- Use of radiation tolerant technologies.

The following missions were initially envisaged for the ISBT transponder:

- Galileo IOV (MEO, Navigation)
- Cryosat 2 (LEO , Earth Observation)
- Swarm (LEO , Earth Observation)
- SAC-D / SAOCOM (LEO , Earth Observation)

Most of them are LEO-EO missions operating in two modes in the downlink. High rate uplink configurations are being considered for new missions (through SW uploading). A summary of the modulation schemes and bit rates used in on-going ISBT programs missions is reported in the following table.

Table 5.1: Functioning modes of the ISBT transponder for ongoing missions

Program	GALILEO	CRYOSAT2	SWARM	SAC/D	SAOCOM
Uplink Modulation	SS	PCM/PSK/PM	PCM/PSK/PM	PCM/PSK/PM	PCM/PSK/PM
TC rate	2 kbps	2 kbps	4 kbps	4 kbps	4 kbps
Downlink Modulation	SS	PCM/PSK/PM	PCM/PSK/PM	PCM/PSK/PM	PCM/PSK/PM
TM Rate	25.48 kbps	16 kbps	8 kbps	4 kbps	4 kbps
Uplink Modulation #2	PCM/PSK/PM	--	--	--	--
TC rate #2	2 kbps	--	--	--	--
Downlink Modulation #2	PCM/PSK/PM	--	OQPSK	QPSK	QPSK
TM Rate #2	25.48 kbps	--	6 Mbps	2 Mbps	2 Mbps

From the table, it emerges clearly how latest LEO missions (except for Cryosat 2 that is a rebuild of an older mission) demand for two transmission modes, a low rate that is compatible with ranging and a high rate for telemetry download. In the case of Galileo, the dual mode for both up- and downlink is imposed by link security reasons more than for an optimization of the transmission rates.

5.3 RF SYSTEM ARCHITECTURE

The new TT&C transponder is based on a well-proven architecture and frequency plan, validated in the two previous transponder generations developed by TAS-E with more than 100 units on flight. The two main objectives of the developments have been:

a) Higher degree of integration, achieved by means of the new high-performance building blocks (MMICs for the RF front end and digital ASIC for the baseband processing), that leads the lowest values of mass and volume for such a unit in the market.

b) Higher level of performance in two levels: a broad list of available modulation schemes and bit rates to fit very different mission scenarios and the flexibility to operate in dual mode (high/low TM rate) to make the ISBT the more versatile TT&C and a used as a reference platform for several years.

In order to provide the required compactness and flexibility a greater level of integration is achieved with the use of a custom low-power ASIC technology for the digital part, whereas RF functions are implemented by the optimally designed GaAs MMICs and the advanced packaging techniques described in this work, aiming to reduce size and weight in comparison with the previous generations of TT&C transponders. This also offers a partial solution to the cost problem, as long as high yield and higher level of integration at the MMIC chip level are achieved [5.2], [5.3]. Figure 5.1 shows a general block diagram of a transponder configuration example, making use of the MMICs developed in the frame of the project MORFEO.

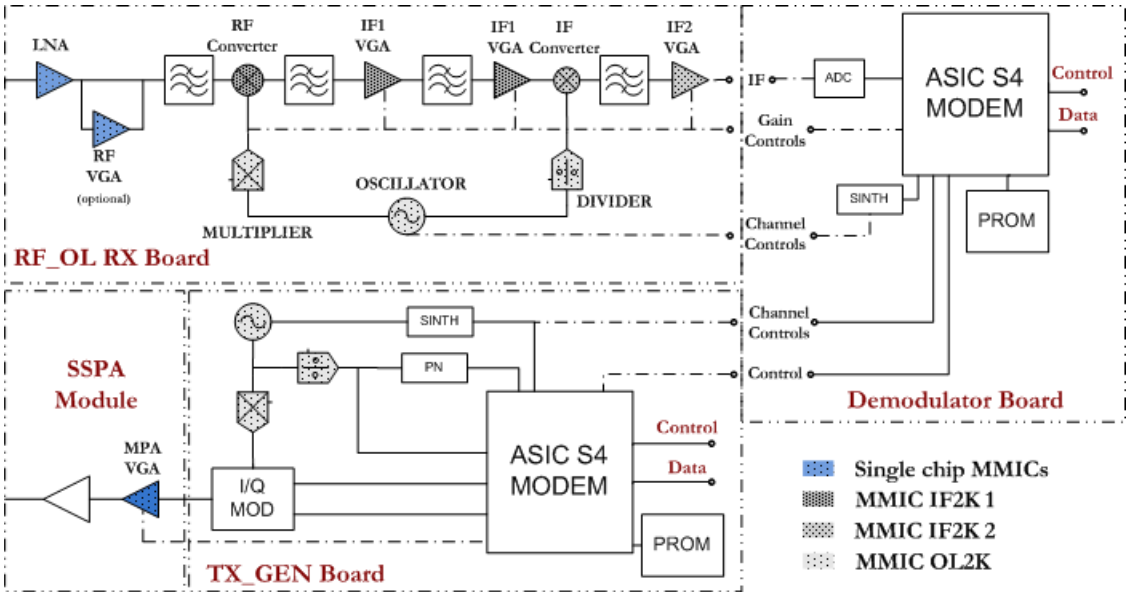


Figure 5.1: Simplified architecture of the new Integrated S-Band TT&C transponder with the developed chips and Multi-Chip Multifunction MMIC modules (MCMM)

For the new transponder architecture, building blocks have been designed and optimized in their corresponding band, but allowing a versatile use in different parts of the chain.

The custom IF VGA, for example, is used at both IF1 and IF2 due to a broadband design. Moreover, in each building block it has been necessary to go deeper into integration with the implementation of multifunction circuits, in which several functionalities are jointly optimized on the same chip. In this way, the GaAs area and the routing interfaces are minimized. Examples of this concept are the two Converters implemented at RF and IF which include RF, LO and IF amplification, and single ended to balanced conversion along with frequency conversion in the same chip. Another way of improving integration was the reduction of I/O interfaces and the simplification of routing commands. This was achieved by using MMIC circuits which combine analogue and digital functions, as in the case of the frequency divider used in two parts of the transponder.

In addition to these characteristics, the designed MMICs allow the selection of different configurations (i.e. power levels, gain…) so as to provide high level of adaptability depending on the mission. Moreover, the number of control voltages has been minimized to simplify tuning during the integration, with the aim of reducing time and assembly costs.

5.4 PACKAGE MODELING

The integration of the MMIC-based modules into the next level of interconnection in the microwave equipment relies on microwave packaging systems so as to facilitate it. Such package systems provide in addition a contamination free environment preserving the high reliability of GaAs dies which is required for space applications. Metallic micro-packages with ceramic feed-through have proven to be the best solution for this issue, also including better shielding, smaller size and easier interconnections in comparison with the Aluminium or Kovar ones [5.4]. However, parasitic effects of the micro-packages worsen the electrical performance of the circuits. Such effects must be foreseen during the MMIC design step and included in the simulations to assure the optimum performance of the designed MMICs after packaging.

Complex EM simulations are very time-consuming and the results may be questionable without measurement verification. For this reason, model extraction is often a pseudo-physical deduction, in which a preliminary modeling step is followed by further optimization so that the final model will fit an original set of measured S-parameters. In this sense, the reproduction of the exact environment in which the packaged MMICs will be allocated is extremely important to generate multiple sets of accurate "real world" S-parameters to be used as the basis of the model extraction.

The selected package was a Ceramic Quad Flat Package (CQFP) from MiniSystemInc. Different pin distributions (16, 24, and 28 leads) were measured and characterized. Figure 5.2 shows an example of a 16-pin CQFP in which the external leads have been preformed (gull-wing configuration) before soldering in order to be compliant with the stress requirements for leaded packages in airborne systems.

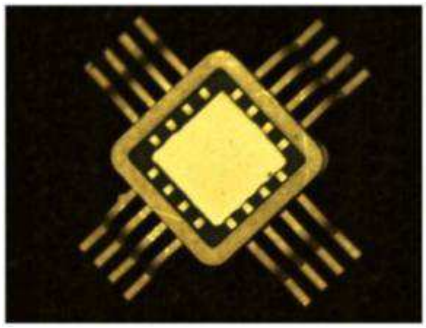


Figure 5.2: 16-pin Preformed Gull Wing lead CQFP used to integrate some of the MMICs.

Different assemblies were tested, placing a set of dummy circuits in the package cavity to evaluate the self and mutual parasitic elements associated to the leads. As an example two configurations are illustrated in Figure 5.3.

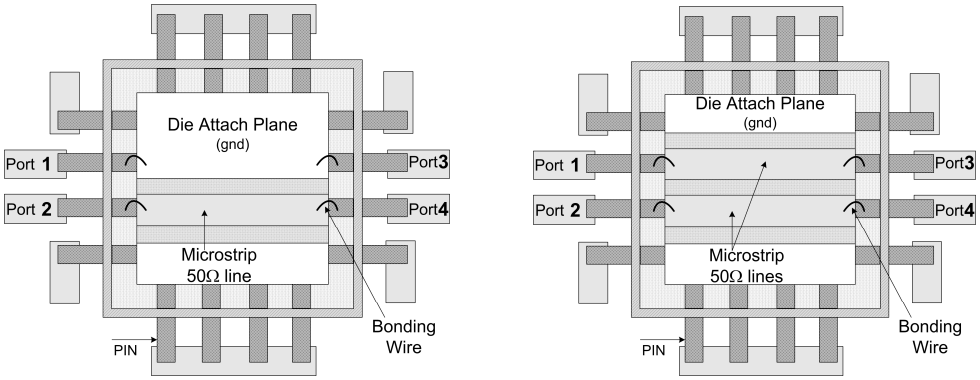


Figure 5.3: Example of dummy circuits used to determine the equivalent model of the selected package. Single (left) and coupled (right) leads. All unused pins are grounded through via holes.

The objective was not to develop a general purpose model of a CQFP but a custom model to support a successful MMIC development. For simplicity and bandwidth requirements, the coupled-π model was empirically found to be a good choice as a starting point for the characterization. Then, it was found by accurate data-fitting that to exactly model amplitude and phase response of the package, additional elements were to be added, based on existing models [5.5], [5.6] for structures with similar geometry. The equivalent model obtained for a couple of adjacent leads is shown in Figure 5.4.

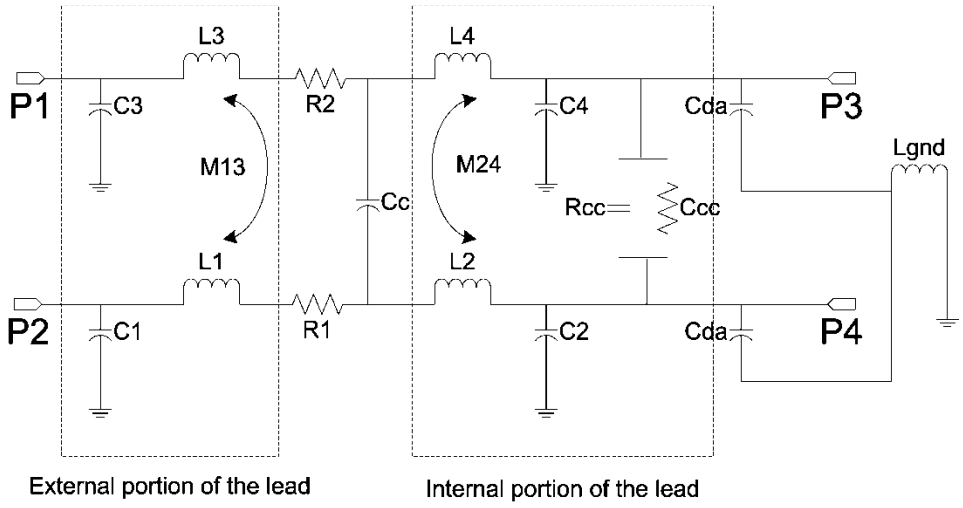


Figure 5.4: Equivalent circuit model of the package for a couple of adjacent leads

The equivalent circuit model consists of a self inductance (L1 for the external connection with the PCB and L2 for the internal connection with the bonding wires) and a parasitic capacitance associated to the dielectric between the lead and the ground plane, which is also divided into two parts. The small series resistance has been lumped into a single element (even if in the simulations part of this resistance has been integrated in the inductance) which corresponds roughly to the AC resistance calculated at 2GHz. The mutual inductive coupling factor (M_{ij}) and the mutual capacitance (C_k) are extracted from the measurement of the coupled lines configuration (Figure 5.3), once the coupled line model was validated in a separate assembly. The RC parallel between two internal portions of the leads has been introduced to provide a better fit to measured data and to allow the lead to be left unconnected with a DC path to ground. Finally, L_{gnd} represents the common ground inductance which depends on the epoxy used to solder the package and on the ground plane thickness.

It has been verified that the difference in coupling between corner and central leads is almost negligible. Hence, as the package is symmetrical, it has been divided into four parts (Figure 5.5), representing each of its four sides. Each of the four parts is connected to the other identical parts by means of the Die attach node. The ground inductance is connected, as well, to this node, which represents the point where the package is soldered to the ground plane of the PCB.

The values of the different elements were tuned until a reasonable match with the measurements was achieved. The obtained values (indicating also the correspondence with the model in Figure 5.4) were:

K1 (M_{ij}) = 0.5 ; K2 (M_{xy}) = 0.01
L1b(L2, L4) = 0.8nH ; L1a (L1, L3) = 0.4nH
R_m_1 (R_{cc})= 1e5Ohms ; C_m_3 (C_{cc}) = 0.003pF
C_m_1 (C_c) = 0.003pF;
R1 (R1, R2) = 0.4Ohms; R1b = 0.3Ohms
C1_ga (C1, C3) = 0.21pF
C1_gb (C2, C4) = 0.21pF
C_m_2 = 0.0008pF
C_da (C_{da}) = 0.003pF

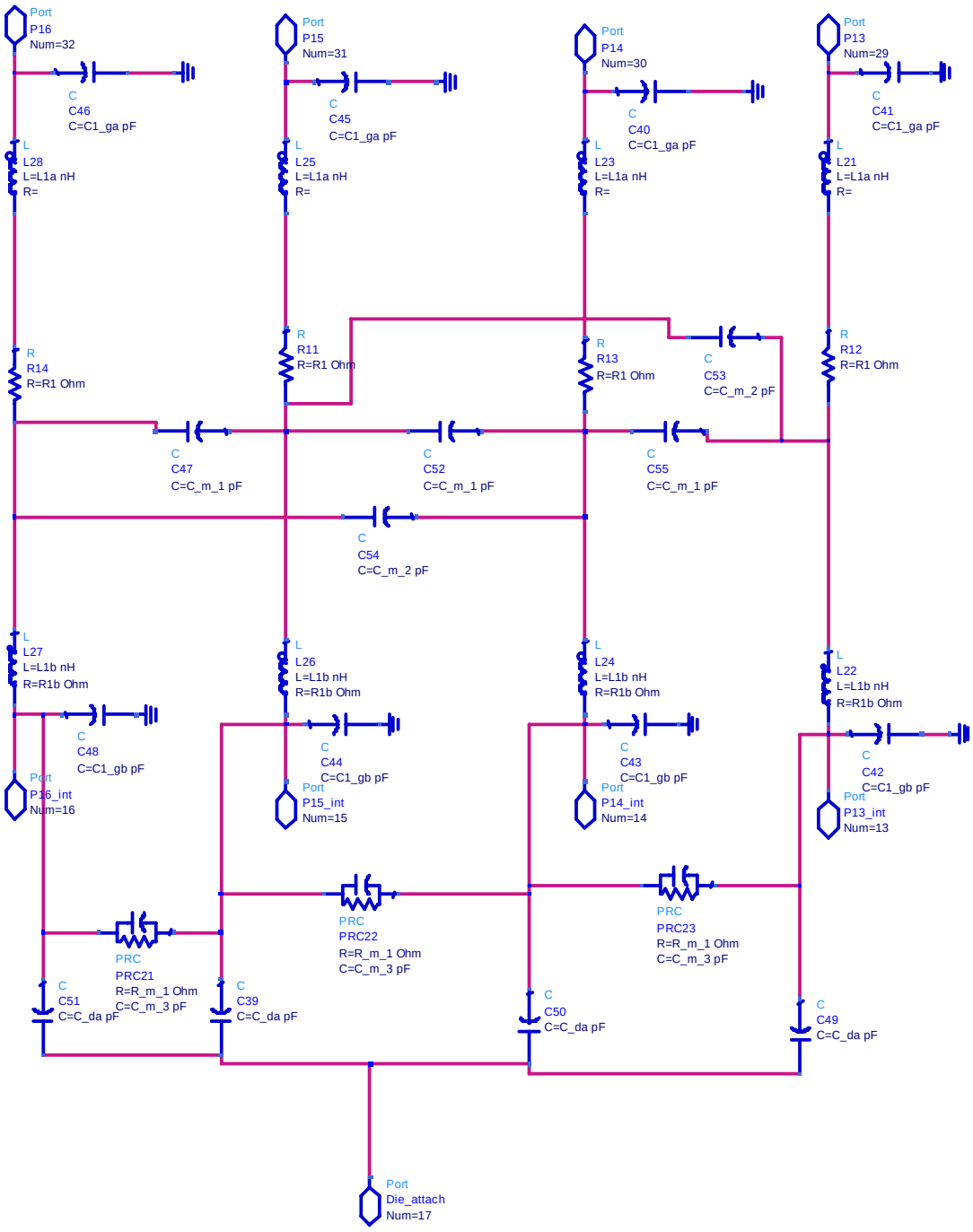


Figure 5.5: Model for one side of the package

The difference between the coupling factors M_{ij} and M_{xy} is due to the fact that the latter is relative to non adjacent leads. Similarly, C_m_2 is the capacitive coupling between non adjacent leads. The ground inductance that must be placed in the Die

attach node depends on the type of epoxy used: L_{gnd}=0.020nH for standard epoxy and L_{gnd}=0.008nH for power epoxy.

A proof of the validity of the developed model for frequencies below 3GHz is shown in Figure 5.6 and 5.7, where excellent agreement can be observed between the lumped model simulated response and the measurements up to 3GHz. Similar level of agreement has been obtained for any combination of the leads.

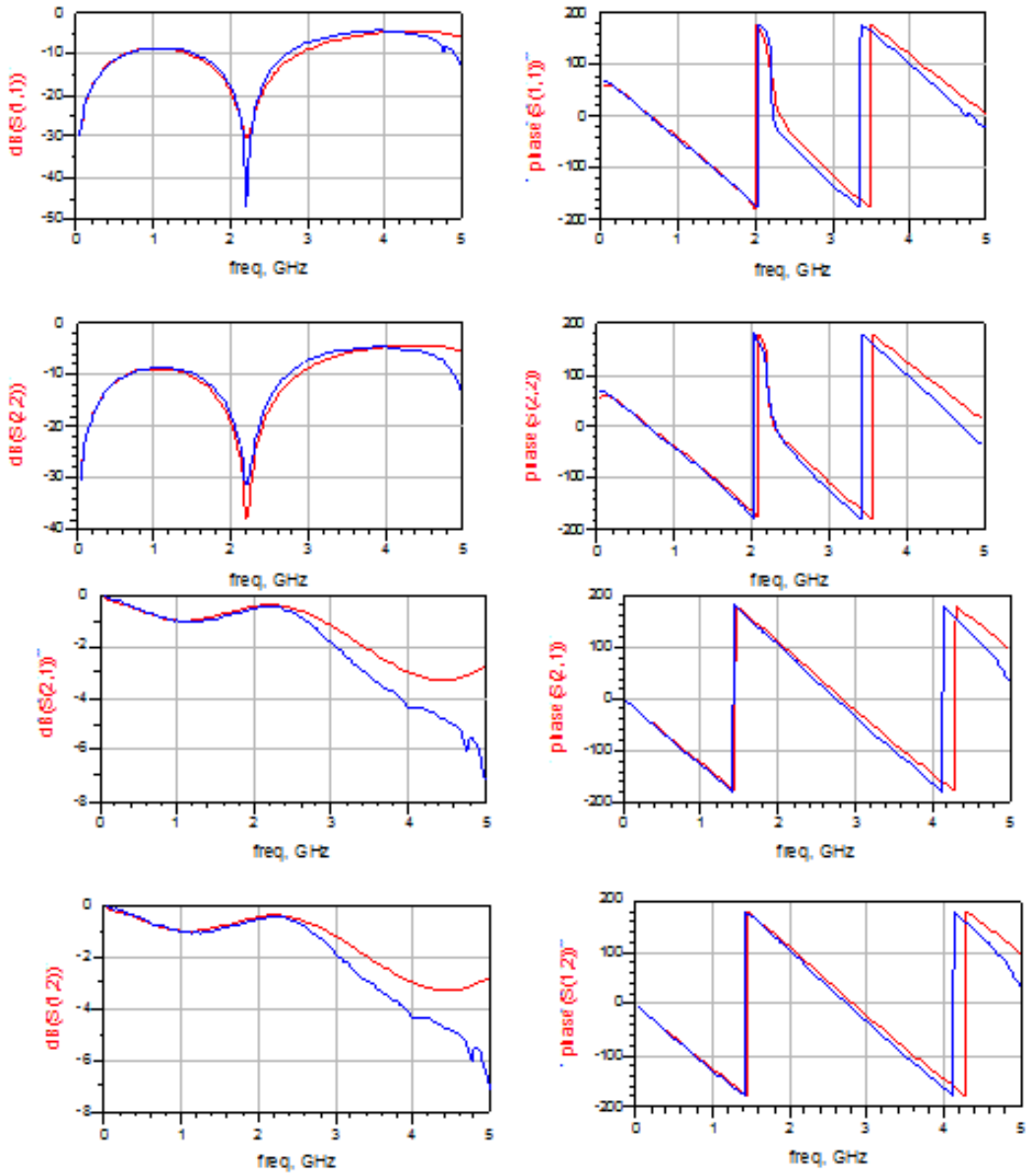


Figure 5.6: Comparison between the simulation results of the modeled (red) and measured response (blue) of the package when using adjacent leads (P1-P2 or P3-P4).

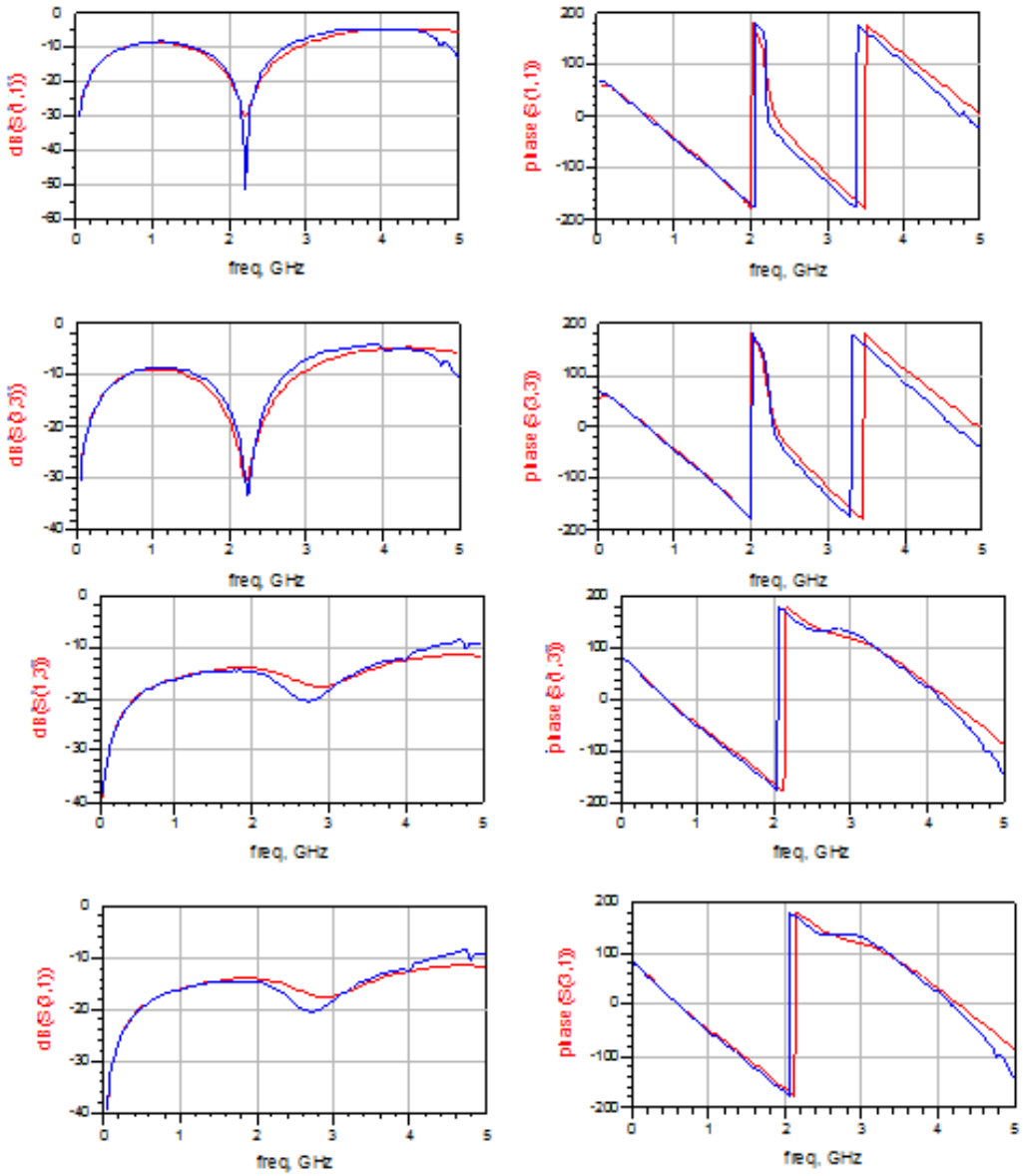


Figure 5.7: Comparison between the simulation results(red) of the determined model and the measured response (blue) of the package when using front leads (P1-P3 or P2-P4).

Following these results, the parasitic effects of the equivalent extracted model have been used throughout the MMIC design stage, to ensure optimum performance of the circuit, once assembled into the package.

One of the most important objectives of circuit design, for large or medium scale production, is to achieve the maximum system integration level. This usually means carrying out a complete system on the same chip, known as System on Chip (SoC). However, these designs are normally useful only for the particular application they were designed for, and provide lower yield in manufacture due to the large size of the chip.

Moreover, SoC test bench complexity is higher and more expensive than for individual circuits.

Nowadays, a new alternative which is widely used is the so called System on Package (SoP), in which the design of smaller parts of the system is carried out separately in order to increase manufacture yield, reduce test complexity, optimize the use of different technologies for different chips, and allow the reuse of the same circuits in other applications or configurations. For these reasons, the SoP approach has been the selected solution even in the cases in which the first design iteration aimed at a complete SoC integration (as described in chapter 3 .).

Once the packages were modeled, another step forward in the new transponder architecture was the use of SoP approach to allow the integration of several MMIC devices into one unique module resulting in MCMM with high fabrication reliability. Using this solution, the full advantage of size and weight reductions brought by MMIC utilization could be exploited, achieving high packaging efficiency by selecting the proper chips following preliminary on-wafer screening trough PCM transistors measurements. In the same way, the total assembly costs are reduced.

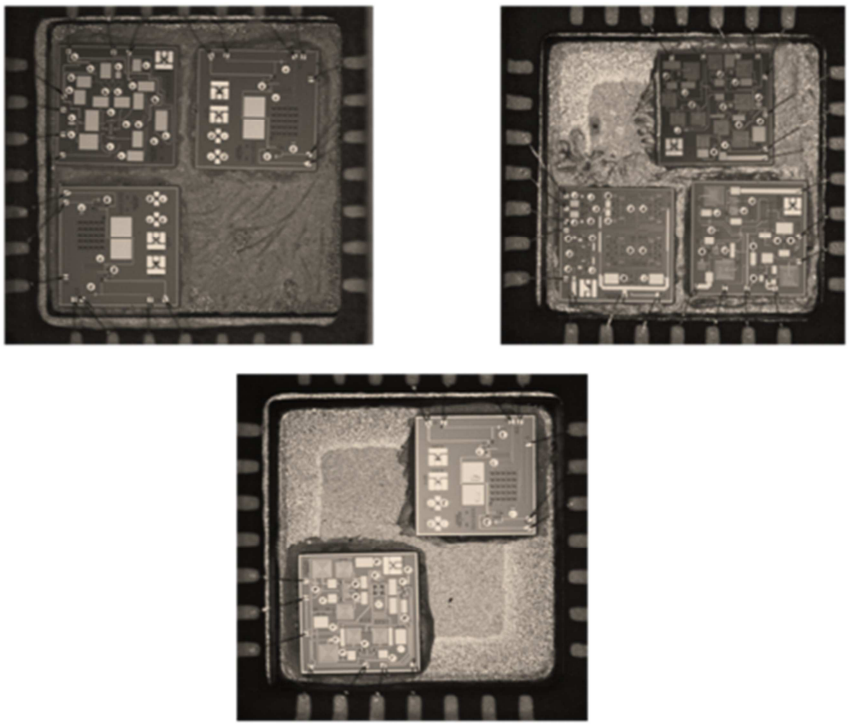


Figure 5.8: Photographs of the developed Multi-Chip Multifunction MMIC modules (MMCM) assemblies IF2K 1 (top left), OL2K (top right) and IF2K 2 (bottom)

A set of three Multi-Chip modules can perform most of the RF functions of the new S-band transponder. Additional circuits have been maintained in individual packages as they proved to be very sensitive to internal interference (i.e LNA and MPA).

Photos of some of the assembled MCMM modules for the configuration of the ISBT shown in Figure 5.1, are shown in Figure 5.8.

5.5 MMIC DESIGN AND IMPLEMENTATION

The design of MMICs has been performed with particular care as circuit tuning is practically impossible after manufacture (even if in some cases is needed to tune circuit's response to the targeted application as is the case of the LNA, MPA and VCO). Some design guidelines should be taken into account to accomplish a successful design. For this reason, as a first step we followed the general guidelines for the design of circuits for space applications [5.7] taking into account the applicable de-rating [5.8].

Comprehensive electrical simulations, including DC, linear, non-linear, noise and thermal analysis were carried out in order to determine the performances of the main circuits as extensively shown in previous chapters. Transistor size and bias points were optimized to achieve minimum consumption while fulfilling the specifications in the thermal range from -30ºC to +70ºC.

Turn on/off response was also monitored by means of transient simulations, preventing the circuits from being damaged by unexpected current spikes during the switching-on of the power supply. Circuit stability was analyzed carefully to guarantee the correct functionality. Methods based on MU or K factors are often inoperative because of multi-loop paths and nonlinear effects, especially in complex circuits and assemblies. Advanced software techniques were used in some cases [5.9]-[5.12] to fully evaluate potential instability and prevent it by placing compensating circuitry in sensitive positions.

Yield tools, based on the statistical models of the fabrication process provided by the foundry, were used in order to predict the deviation in performance due to process variations. All the chips were designed to be tolerant to process variations. The influence of every circuit element was analyzed to determine its effect on circuit performance. If a small change in the element value caused a large change in the circuit performance, either the element or the circuit topology were modified to guarantee the maximum reliability. Finally, whenever possible, topologies that were proven to be

process tolerant were selected (as the case, for example, of the digital divider in chapter 3).

To check if each fabricated circuit is compliant with the expected behavior and facilitate chip selection, PCM (Process Control Monitoring) transistors were included in every MMIC.

Target single chip area was set to 2 mm x 2 mm to trade-off yield and fabrication costs without compromising functionality. However, for the first design iterations (e.g. LNA and MPA) different sizes were used to allow testing of additional function and to fit the chips into an intermediate Multi-Project-Wafer fabrication.

The number and locations of pins were chosen to simplify the interconnection and the integration into the micro-package. A summary of the simulation and measurement results for the MMICs which have been described in the previous chapters or in separate works is reported hereafter together with design and implementation details for the newly developed circuits (i.e. the LNA and the MPA). All the MMICs were assembled and tested in their final package.

5.5.1 **LNA**

5.5.1.1 **DESIGN**

A new circuit has been designed to meet system requirements. The topology chosen for the circuit implementation is illustrated in Figure 5.9.

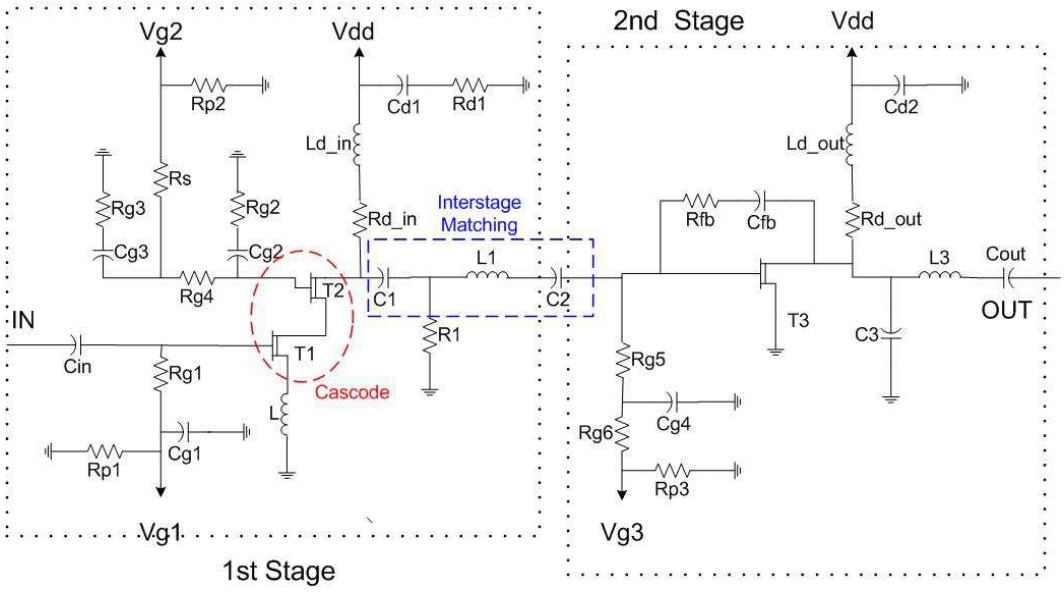


Figure 5.9: Input LNA schematic topology.

Main design specifications to be used for this input stage of the ISBT were the following:

- Gain between 28 and 32dB in the 1.97 - 2.17 GHz band
- Minimum +10dBm 1dB output compression point
- Minimum saturated output power of +12dBm and Output third order intercept of 20dBm
- < 1.5 dB Noise Figure in the 1.97 – 2.17 GHz band
- Power consumption between 28 and 35 mA at 3.5 V

The circuit designs relies on two stages optimized separately: the first one is in charge of providing the noise characteristics of the whole circuit, while the second is an output buffer stage which guarantees the power characteristics.

For the first stage a cascode configuration have been chosen to ensure enough gain and good noise with low power consumption. This choice was dictated by the fact that, due to the high losses and poor quality factor of the integrated spiral inductor (Ld_in) needed in the drain bias lines, an amplifying structure capable of providing enough gain was needed not to degrade the noise behavior.

The output buffer stage is a parallel feedback amplifier which has been selected because of its wide operating bandwidth and robust and stable performance.

The amplifier is DC decoupled by means of on-chip capacitors while the input noise matching network is implemented off-chip to guarantee better flexibility (tuning and re-configurability) and improved noise performance. The output power match (network C3, L3 and Cout) is on chip.

In the MMIC design, attention was mainly focused on achieving a low minimum noise figure (NFmin) in a broad bandwidth (0.5 to 2.5GHz) to allow the reusability of the design. The output buffer stage is optimized to give output power in excess of 10dBm.

Separate drain supplies have been used to allow individual checking of the two stages and possibly optimize power consumption in the second design iteration (as the designs have been a bit oversized to ensure full compliance at the first implementation).

The active layout area (including the PCM monitoring transistor) has been organized to fit an area of 2 mm^2, because this was the target final extension of a single chip. However, in order for the chip to fit with the mask organization of the wafer in

which will be fabricated this first prototype (together with the MPA described in section 5.5.6), the layout has been slightly modified (the output line and the gate and drain bias lines of the output stage have been lengthen) to occupy an area of 3x3mm2 (Figure 5.10).

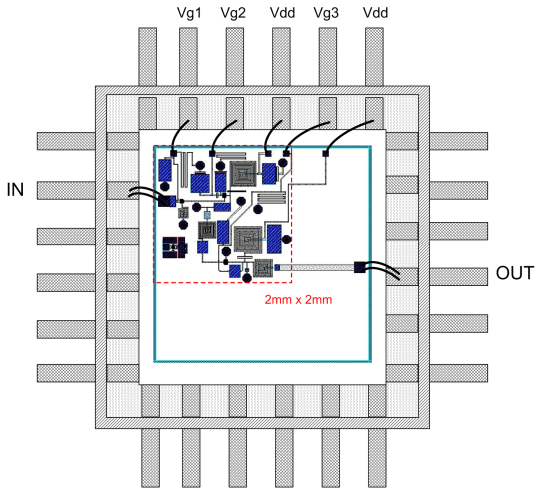


Figure 5.10: Layout and chip positioning inside a 24-pin package

The rest of the chip has been used to house multiple test circuits, and additional PCM transistors. Final implementation (next fabrication run for the flight version) will fit in the target configuration and package (Figure 5.11).

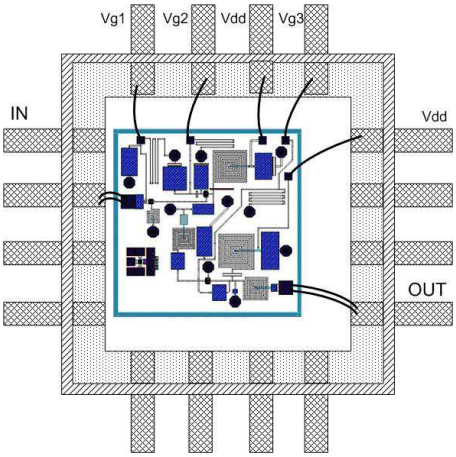


Figure 5.11: LNA target layout and positioning inside a 16-pin package.

Each gate is protected against electrostatic discharges by way of >40KOhm grounded resistors. Input and output pins sizes have been doubled to allow a double bond wiring to reduce inductance and minimize effects of the bonding length on the RF performance of the circuit.

5.5.1.2 SIMULATIONS

The off-chip input match can be implemented in different ways by using high quality lumped passives and microstrip networks. Due to some limitations in components for use in the space mission, we were forced to opt for the microstrip solution using a space qualified substrate (Polyamide: heigh=1.57mmm, ε_r=4.7, Conductivity=8.47e6, metal thickness=0.05mm, Tanδ=0.0016, Rough=0.00042mm). Both open and short stub solution were evaluated, but considering implementation aspects and easiness of adjustment an open stub solution has been considered in all the simulations.

Modelled package effects are included in the schematic for the simulations. As far as the solution adopted for the input matching network, its dimensions have been optimized to guarantee a satisfactory trade-off in terms of noise, matching, and operating bandwidth. If better noise (but worse input matching) would be necessary, different solutions should be used.

All the results shown in the following figures are relative to the configuration in Figure 5.10 including the 1mm long output line necessary to fit with a 3mm^2 area. The only remarkable difference between the simulations with and without output line, is a negligible change in the output match (the output line is close to a 50Ohm impedance and the LNA output is very well matched to this value) and 0.2dB output compression due to transmission line losses. All the other parameters remain substantially unchanged. The reported results are relative to the worst case simulations at 70º.

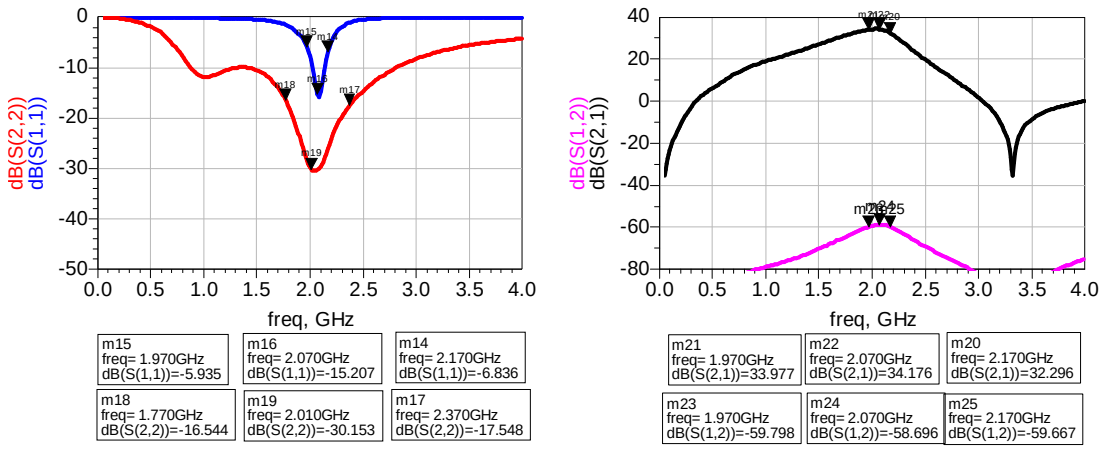


Figure 5.12: Small signal scattering parameters simulated at 70ºC

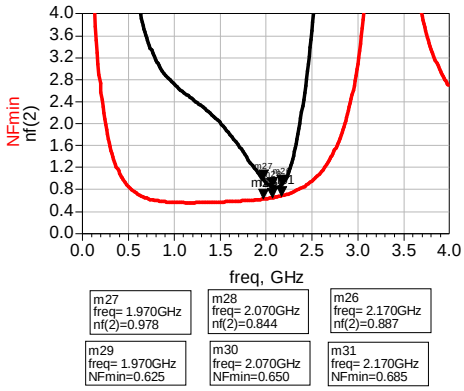


Figure 5.13: Minimum noise figure (NFmin) and Noise figure of the amplifier (distributed matching network) at 70ºC

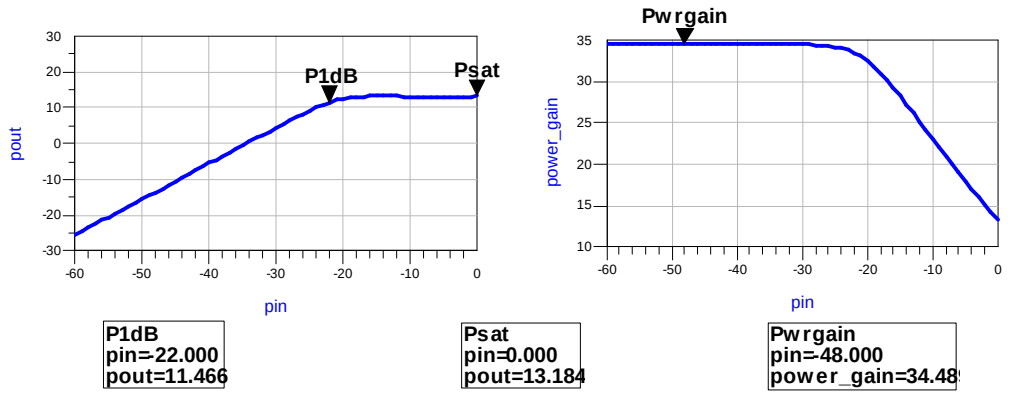


Figure 5.14: Pin-Pout curve and power gain at mid-band (2.07GHz) @70ºC. Markers indicate the Output 1 dB Compression, the Saturated Output Power and the Linear Power Gain

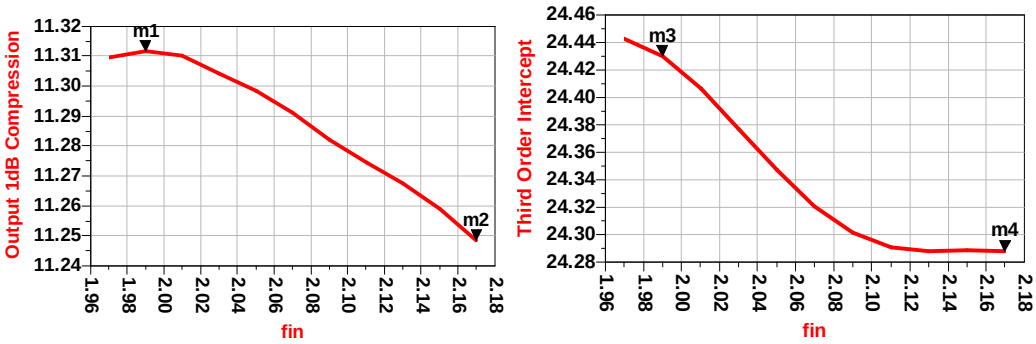
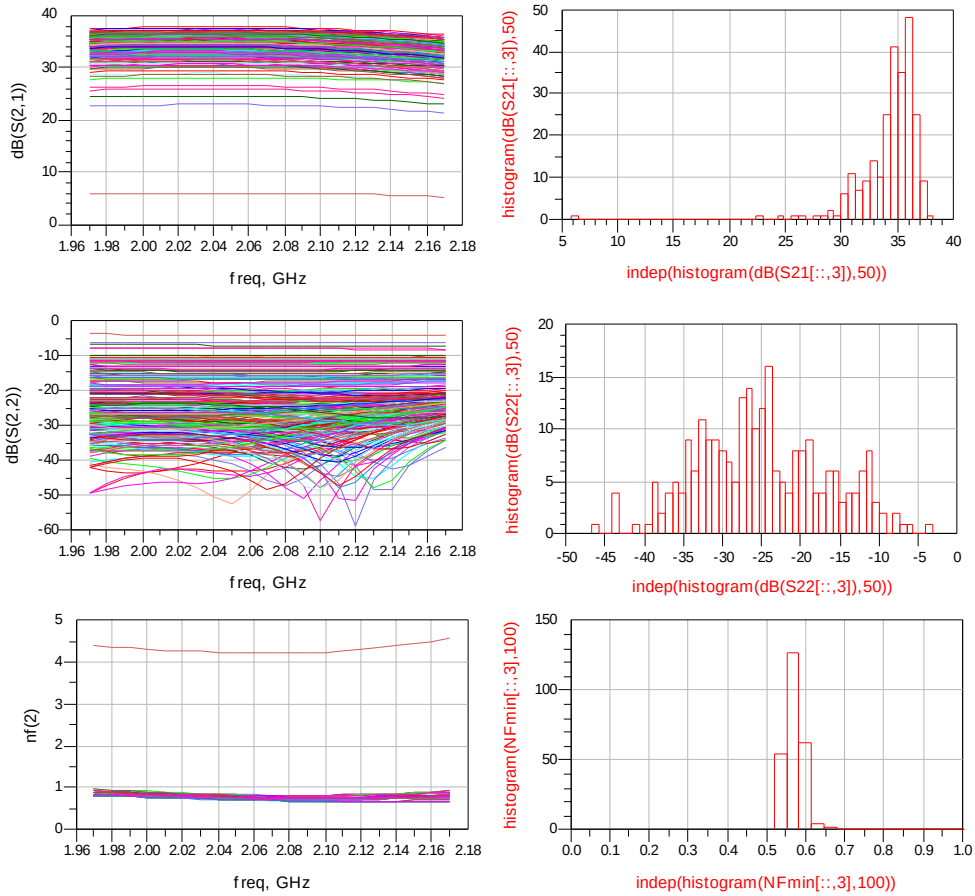


Figure 5.15: Output 1-dB compression and Third Order Intercept point variation (dBm) against frequency (GHz) @70ºC

Yield analysis was carried out for both the small signal and large signal behavior. Because of the lack of statistical parameters for the substrate and the PCB fabrication (input matching network), the simulations focused on the parameters which are mainly determined by the chip process variations, that is output match, minimum noise figure (NFmin), small signal gain and output 1-dB compression. All the analyses include a

post production tuning, explained as follows. During the Yield (Monte Carlo) analysis, the process parameters are varied accordingly to the statistical distributions provided by the foundry. The result of this simulation is referred as the Pre-tune Yield. But, once the chip is fabricated, it is possible to act on the supply voltages (only gate bias, because the drain supply voltage is fixed and the gate bias will be adjusted automatically by means of external circuitry aiming at maintaining nominal supply current) and tune the circuit to meet the specifications. So it is possible that some trials which originally fail to meet the specifications (Pre tune fails), after the tuning process can be converted into successful trials (PPT_converts or Post-tune converted), giving rise to a different and more realistic yield result (Post tune Yield).



PreTuneFail	PreTunePass	PreTuneYield	PPT_Converts
65.000	185.000	74.000	28.000

Post Tuning Yield

85.200

Figure 5.16: Small signal yield results. Number of trials=250. For each parameter (gain, output match and minimum noise figure) are plotted the value for every trial, and the histogram relative to the mid-band frequency (2.07GHz).

In the small signal yield analysis, the specifications were set to: S_{21}>30dB S_{22}<-15dB and NF_{min}<0.65dB, within the operating bandwidth.

The results were deemed satisfactory with a post tune yield of more than 85% and a calculated estimated prediction error of less than 7% for a CL of 99.9% (see also chapter 2). Keeping in mind that the input match is external, it is important to ensure that the chip itself is stable; regardless the type of passive external match is employed. This can be accomplished with the analysis of the stability parameters k, Mu and Mu' ([5.13], [5.14]). If all parameters are greater than one, then the chip is unconditionally stable. The worst case corresponds to a temperature of -30ºC, where the gain is greater (with 70ºC and 25ºC the stability is more robust). To ensure a stable behavior up to 50 GHz, a separate yield analysis was performed for all the stability factors. The results of this analysis are plotted in Figure 5.17: a 100% yield is obtained ensuring unconditional stability.

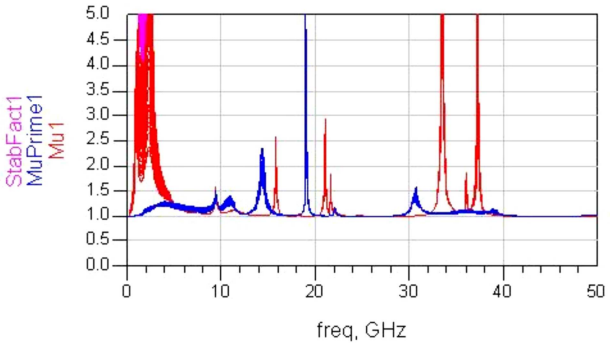


Figure 5.17: Stability yield results. Number of trials=250.T=70º

The large signal yield results at the upper frequency band (where the output compression power performance is worse) are illustrated in Figure 5.18 for a yield specification set to OP1dB>10dBm .

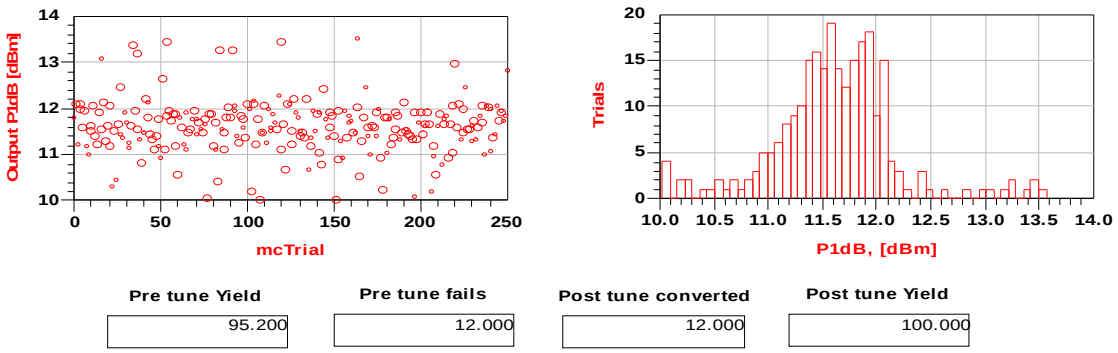


Figure 5.18: OP1dB yield results. Number of trials=250. In the figures are represented the OP1dB at upper-band (2.17GHz) for every trial and the complete histogram.

Analyzing the yield results it has been noticed that the trials which fails to meet the P1dB yield specification can be adjusted to satisfy the requirement just by changing the gate bias of the third stage (Vg3).

As a consequence of the 100% post tuning large signal yield, the overall yield (small and large signal) coincides with the case of the small signal reported in Figure 5.16.

As in real operations, the circuit will be used in a narrow bandwidth configuration (in the order of 25MHz), yield analysis including the possibility of tuning the input matching network to achieve good input match and noise figure in a limited frequency range have also been performed. The simulations have been limited to a 40 MHz bandwidth around the frequency at which the input matching network shows its minimum (i.e. 2.08GHz). Results could be easily extended to any other network capable of achieving a 40MHz matching bandwidth around a specified frequency. Two more degrees of freedom have been added at the post production tuning, that is the width and length of the open circuited stub which could be eventually modified on the PCB.

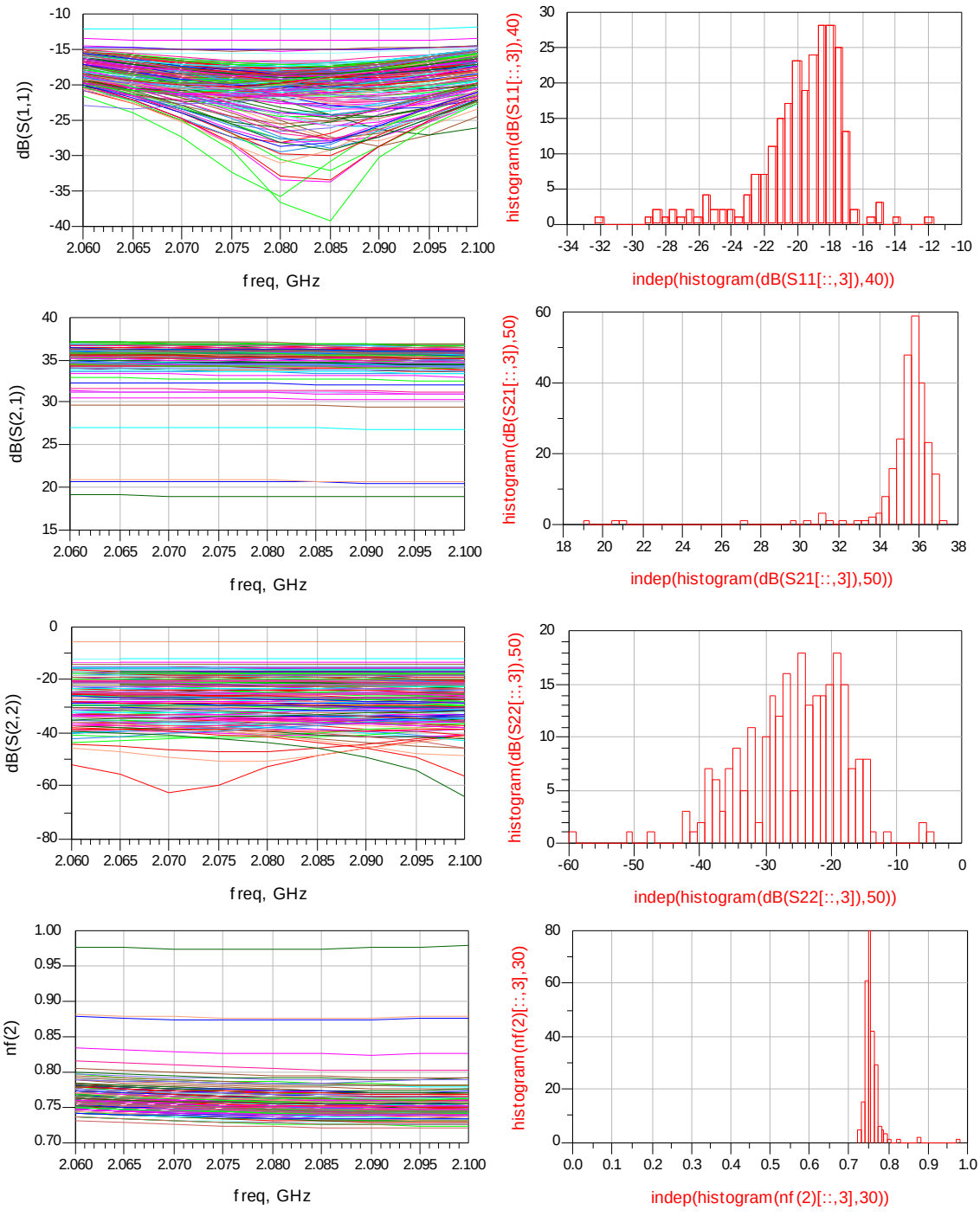
The specifications were set to:

- dB (S21)>30dB
- dB(S11)<-15dB
- dB(S22)<-15dB
- Noise Figure<0.8dB
- Frequency [2.06 GHz, 2.1GHz]

The results are plotted in Figure 5.19. Even if the simple yield gives a poor result of 44%, it can be noted that almost all the circuits (95.6%) can be adjusted to meet the specification within the specified bandwidth.

An additional yield analysis performed was the combination of narrowband input (depending on the input network) and broadband output (depending on the chip) parameters. Even in this case the post processing tune gives a very good result (Figure 5.20). In this case the specifications were set to:

- dB (S21)>30dB [1.97 GHz, 2.17GHz]
- dB(S22)<-15dB [1.97 GHz, 2.17GHz]
- NFmin<0.6dB [1.97 GHz, 2.17GHz]
- dB(S11)<-15dB [2.06 GHz, 2.1GHz]
- Noise figure<0.8dB [2.06 GHz, 2.1GHz]



PreTuneFail	PreTunePass	PreTuneYield	PPT_Converts
139.000	111.000	44.400	128.000

Post Tuning Yield

95.600

Figure 5.19: Narrow-band yield results. Number of trials=250. For each parameter are plotted the value for every trial, and the histogram relative to the centre of the simulated bandwidth (2.08GHz).

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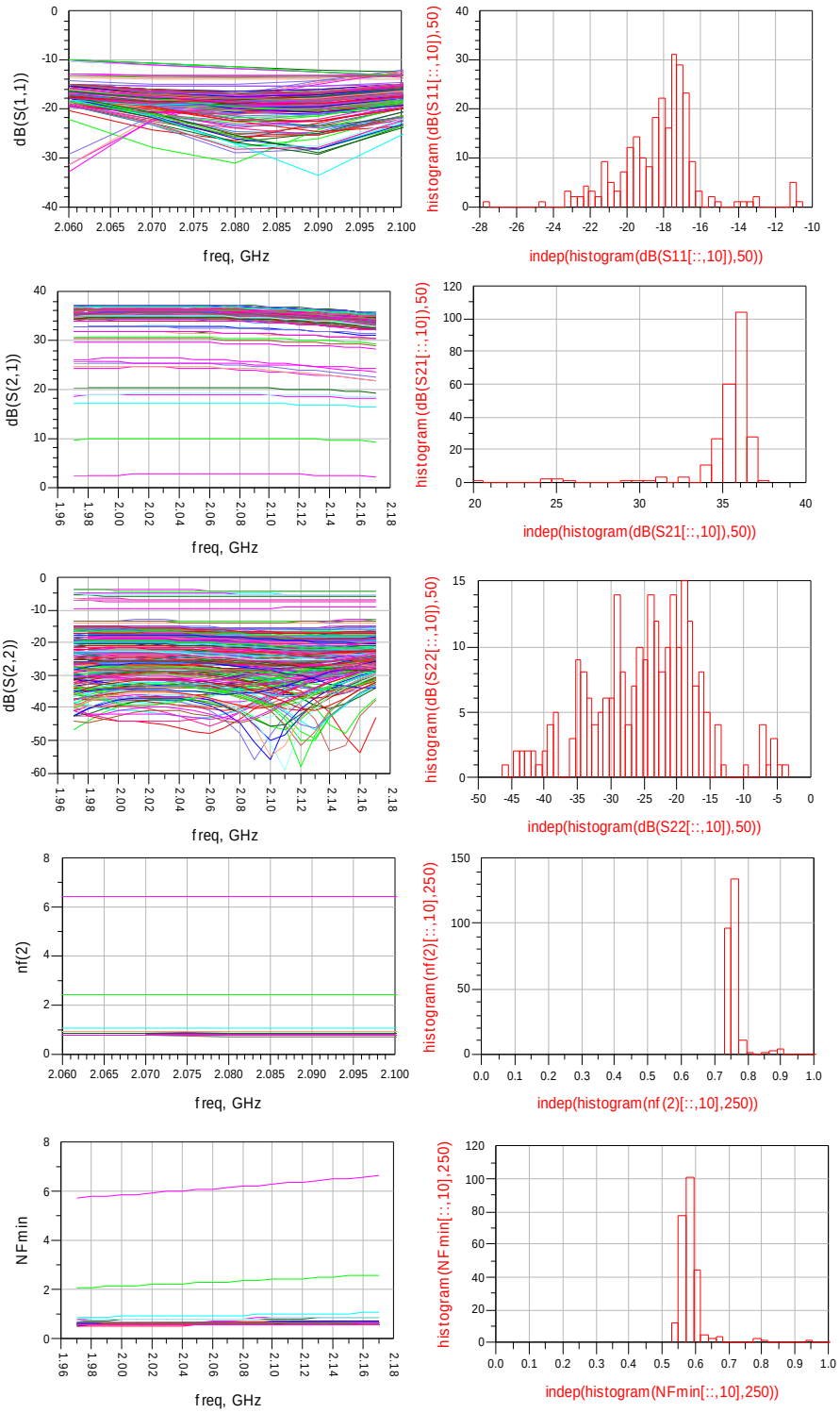


PreTuneFail	PreTunePass	PreTuneYield	PPT_Converts
133.000	117.000	46.800	110.000

Post Tuning Yield

90.800

Figure 5.20: Narrow-input matching and broad-output matching yield results. Number of trials=250. For each parameter the value for every trial, and the histogram relative to the centre of the simulated bandwidth (2.08GHz) are plotted.

Analyzing the yield results, it has been noticed that the reason for which a circuits may fail to meet the specifications even after tuning are those for which the Vt_{ON} (pinch-off voltage of the normally on transistor which can be monitored directly on the PCM transistor) is greater than -0.7V. When its value is greater than -0.7 V (approximately), then it is not possible to adjust the performance to meet the specifications. For this reason it was suggested to discard from the wafer every circuit for which the process parameters of the monitoring transistor placed on the chip showed a Vt_{ON} > -0.7V.

Additional simulations have been carried out in order to ensure a safe behavior of the circuit during the switch-on/off of the positive supply voltage due to the sensitivity of the cascade topology to the appearance of big voltage and current spikes. Basic assumption is that the negative gate voltage Vg1 (applied to the gate of Input transistor) is fixed prior to the switching up of the positive supply through the circuit of Figure 5.21. The resistive divider is used to obtain the positive voltage (Vaux=Vg2) required to bias the second transistor in the cascade input amplifier.

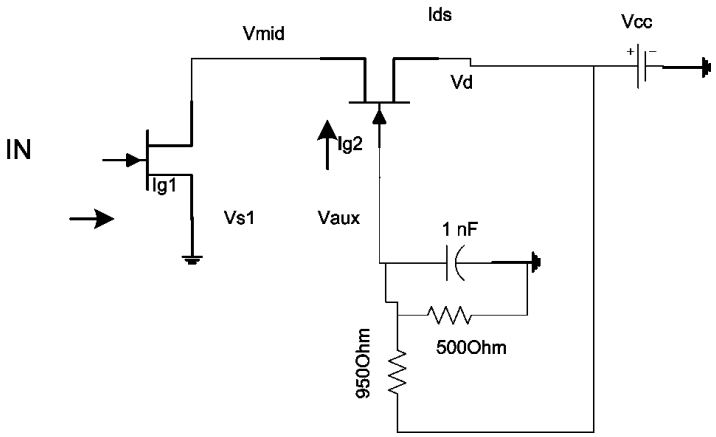


Figure 5.21: Circuit implementation used to simulate the switching on/off of the transistors.

In the switching-on case the supply voltage (Vcc) has the following characteristics.

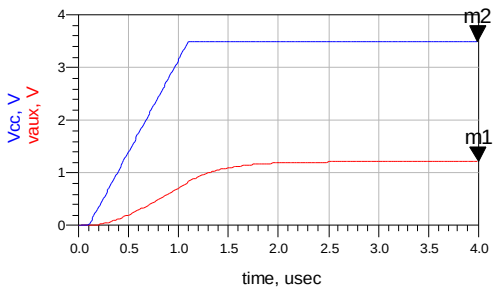


Figure 5.22: Positive supply voltages behavior at switch-on

The responses of the voltage and current of the two transistors are illustrated in the following figures (in all the cases has been used an input signal with -40dBm power and 2.07 GHz frequency).

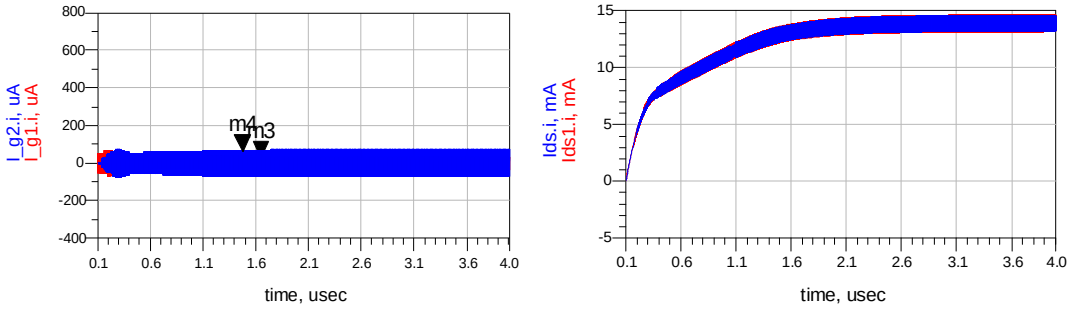


Figure 5.23: Gate and Drain current behavior during switch-on of the Vcc

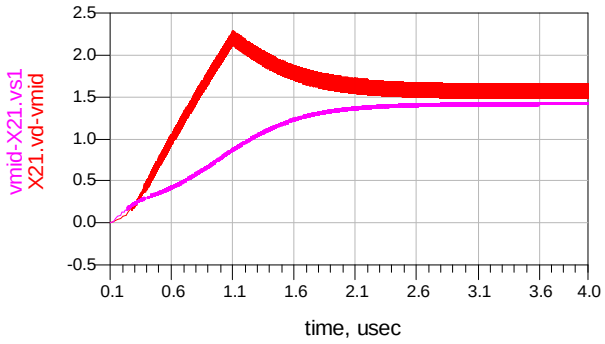


Figure 5.24: Voltage swings across cascaded transistors during switch-on of the Vcc

In the Vcc switch-off case the results are illustrated in the following figures, confirming a safe operation in all the cases.

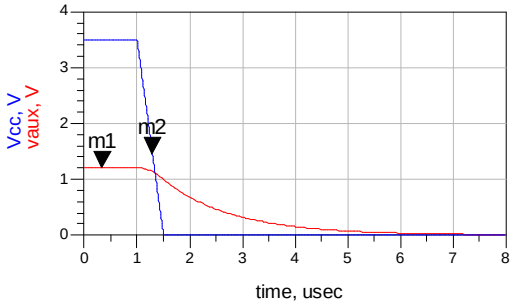


Figure 5.25: Positive supply voltages behavior at switch-off

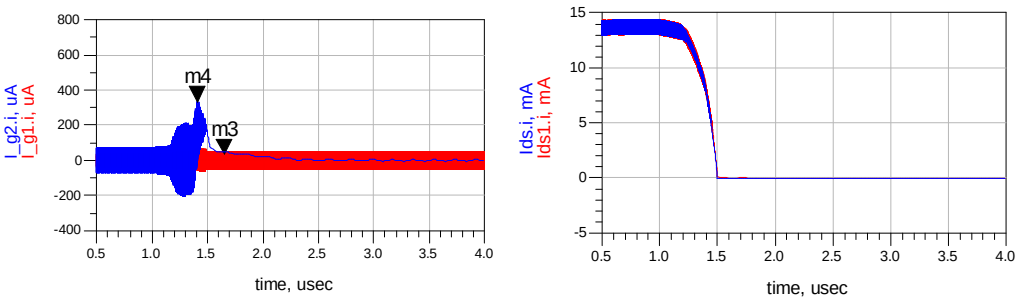


Figure 5.26: Gate and Drain current behavior during switch-off of the Vcc

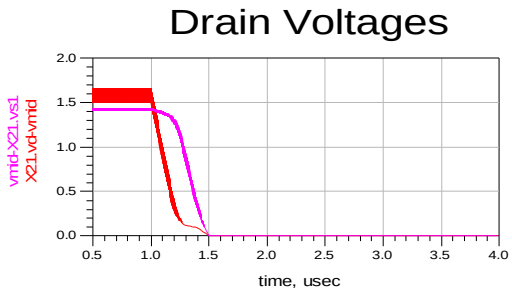


Figure 5.27: Voltage swings across cascaded transistors during switch-off of the Vcc

5.5.1.3 IMPLEMENTATION AND MEASUREMENTS

Once fabricated, multiple units of the LNA were sent to TAS-E for packaging (Figure 5.28) and assembly on the test PCB (Figure 5.29). Input and output 50Ohm coaxial connectors were used to interface the circuit with the instrumentation.

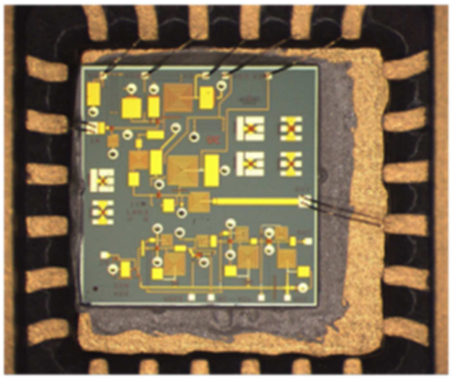


Figure 5.28: Microphotograph of the packaged LNA

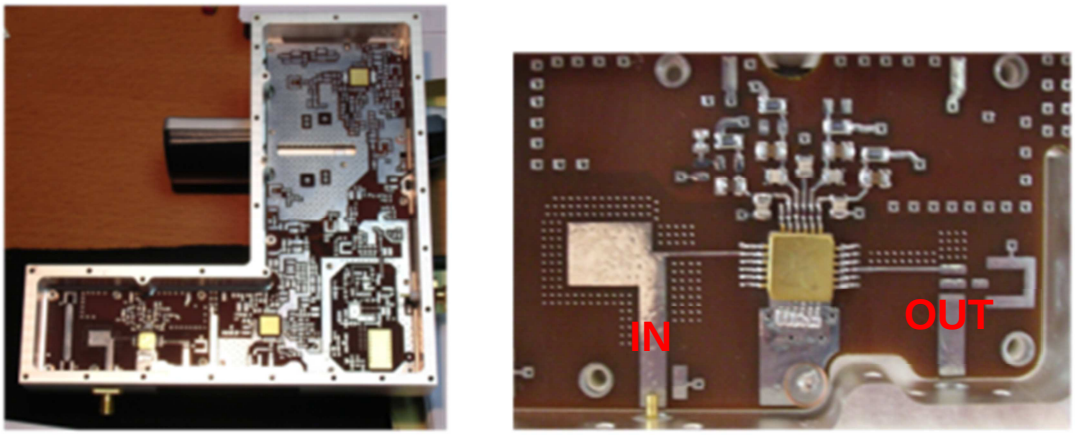


Figure 5.29: Photo of the RF transceiver (left) and detail (right) of the assembled LNA.

Good agreement between simulation and measurements is reported in Figure 5.30 and Figure 5.31. Some potential instability problems have been detected in the assembly provided by TAS-E around 2GHz, but it was later discovered it was associated to a poor grounding offered by the package lid and solved (measurement not reported in the figure) through proper grounding by means of a copper ribbon (Figure 5.34) in the following assemblies. The worsening in input and output match performance was discovered to be associated to the different epoxy used by TAS-E with respect to the one used in the modelling of the package resulting in a higher value of the grounding inductor. The different simulations reported (in red and black solid lines) are relative to the nominal (0.025nH, red) and updated (0.1nH, black) die attach inductance L_{gnd}.

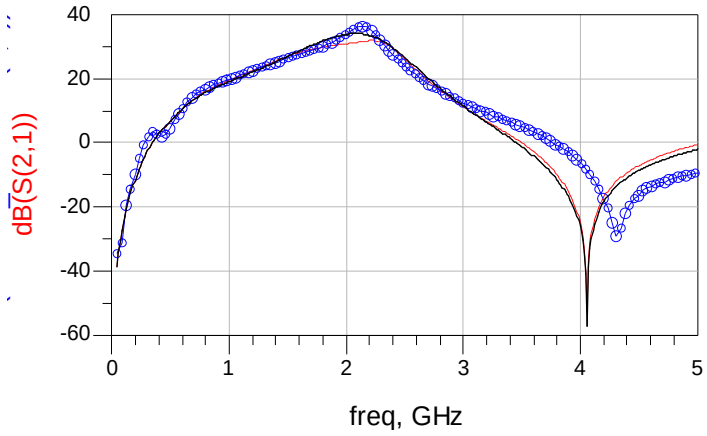


Figure 5.30: Comparison between simulated (solid lines) and measured(dotted) Gain

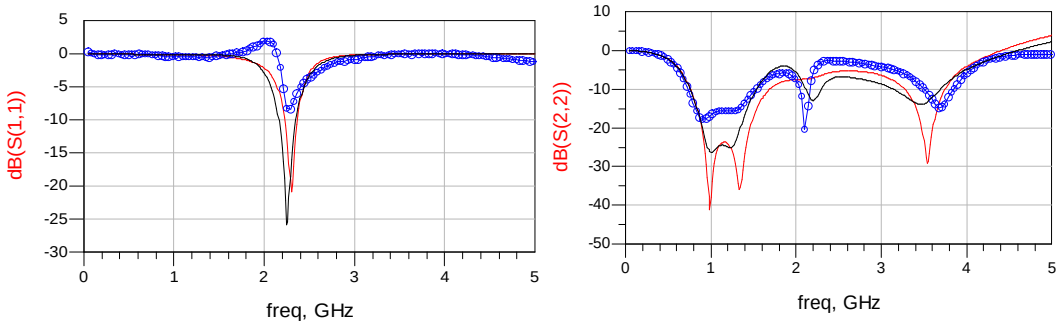


Figure 5.31:Simulated (solid lines) and Measured (dotted) input (left) and output (right) match

The measured noise figure (Figure 5.32) is slightly higher than the simulated value. This is due to the presence of the coaxial connectors in the test PCB with losses not accounted for in the simulations.

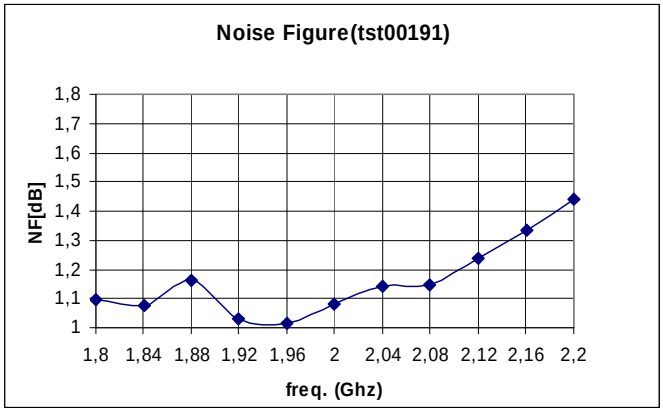


Figure 5.32: Measured NF, with narrowband matching

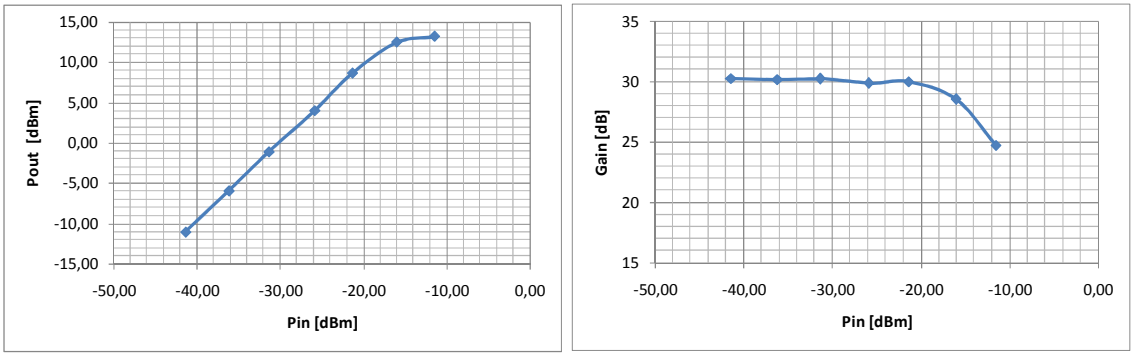


Figure 5.33: Measured output power compression.

In order to improve the input match and to achieve a broader frequency response, different solutions were tested by TAS-E by modifying the supporting PCB. An example of an "empirical" matching network which provides a good match in a broader bandwidth is shown in Figure 5.34.

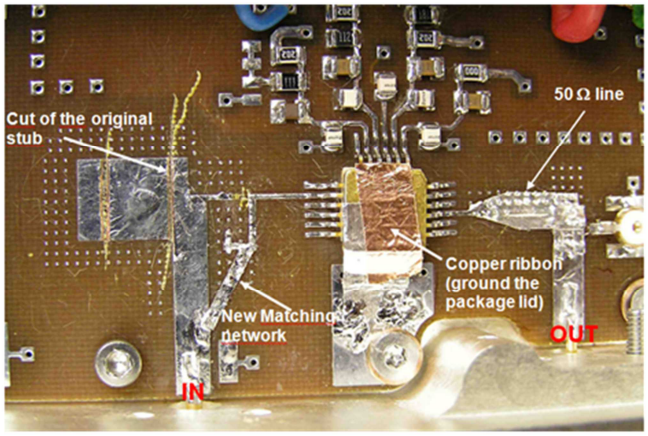


Figure 5.34: Modified matching network.

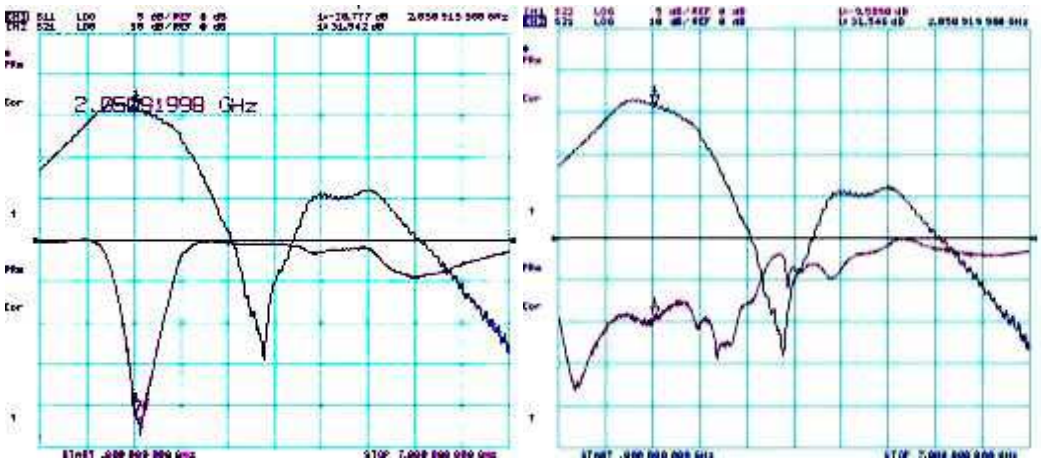


Figure 5.35: Measured Gain and input (left) and output (right) match for the circuit in Fig5.34

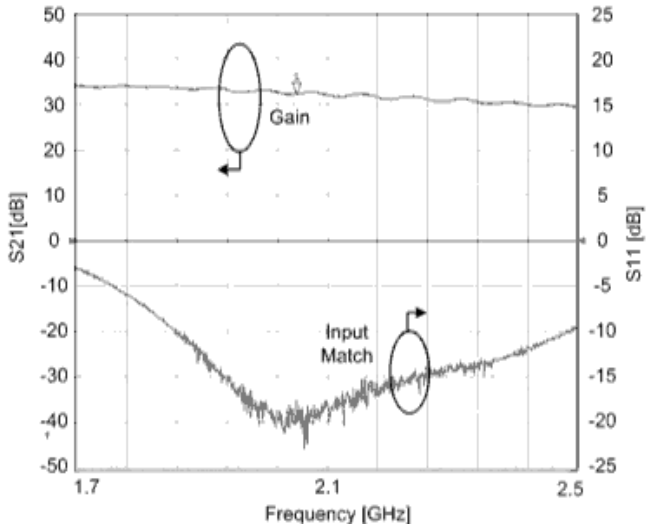


Figure 5.36: Detail of the LNA gain and input match with the broadband matching network

The measured results in Figure 5.35 have been also reproduced in the simulation environment (Figure 5.37) adapting the matching network to the physical parameters observed in the assembly.

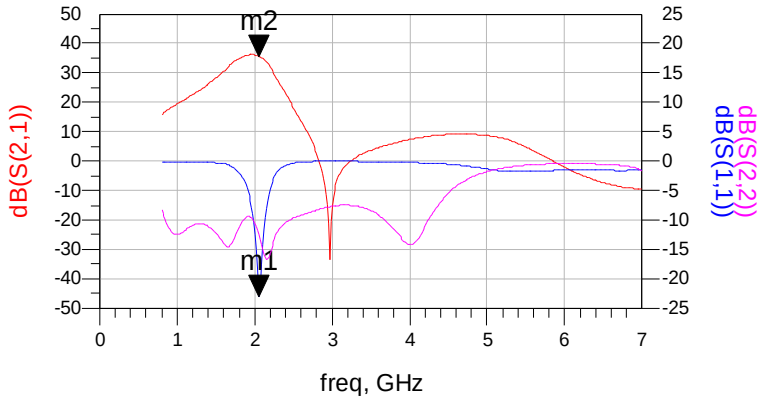


Figure 5.37: Simulation results of the LNA with the implemented broadband network.

Despite a worsening in NF with respect to the narrowband solution (*Figure **5.38***), the overall performance meets all specification parameters. A summary of the main parameters is detailed in Table 5.2. The functional yield obtained for this circuit for the first fabrication run was close to 87%. As the circuit performance well fully compliant with the design specification, the final implementation of the circuit simply consisted in the optimization of the layout area in order to fit within the specified area.

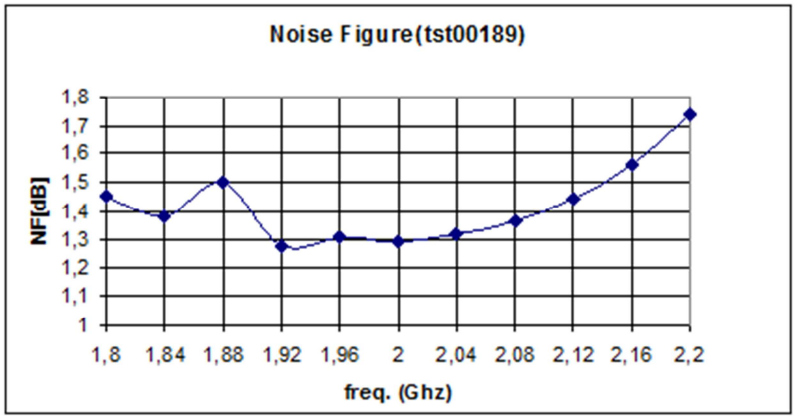


Figure 5.38: Measured NF with the broadband matching network

Table 5.2: Results vs. requirements for the input LNA

Parameter	Simulation	Measurement	Units
Center Frequency	2070	2070	MHz
BW	160	200 (*)	MHz
Current	30	32	mA
Power Supply	+3.5	+3.5	V
Gain	34	>30(*)	dB
OP1dB	10	11	dBm
NF	0.9	1.3(*)	dB
Input Match	<-15	<-17(*)	dB

(*) These values depend on the external matching network

5.5.2 **Variable Gain Amplifiers**

5.5.2.1 **RF VGA**

The RF VGA is used to control the signal at the transmitter input for gain or power-variation compensation. This circuit is used only for specific transponder applications. Full detail of this circuit implementation have been given in chapter 2.

5.5.2.2 **IF VGA**

The IF VGAs have been implemented by means of a single Dual-Band IF VGA shown in Figure 5.39 which is used at both IF1 and IF2. This circuit has been developed in a parallel work [5.15] within the same project MORFEO, but will be briefly described as it was used in the final transponder implementation and testing.

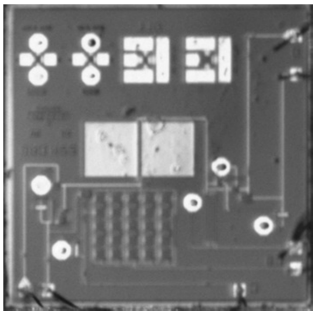


Figure 5.39: Photograph of the dual-band IF VGA

The VGA consists of three amplification stages: the first one provides good input matching, the second one the majority of the gain and the third one the required output power. The gain control is carried out by means of several parallel optimized switches at the second stage to reduce non-linearities at high level attenuation.

The circuit shows dual-band performance (at 9MHz and 200MHz), with a wide operating bandwidth, (broader than 55% at 9 MHz, and 20% at 200 MHz). At both frequency bands, the gain control is better than 24 dB maintaining high output P1dB of about 6dBm.

The IF bandwidth is set for the signal requirements of dual mode operation. As an example, one typical dual mode combination is: spread-spectrum plus PM mode. With the spread-spectrum, a suppressed carrier scheme with 3-4MChip/s allows accurate ranging, low emission density and spurious added resilience.

The group delay degradation (which was critical mainly at 9 MHz, because of the lower frequency value and the broader relative bandwidth) has been minimized by DC-

coupling 2nd and 3rd stages and properly designing the internal RF chokes. The group delay obtained was better than 0.9 ns. Simulation and measurement results at both frequency bands are summarized in Table 5.3. The yield of this circuit was around 84%.

Table 5.3: Results vs. requirements for the dual-band VGA

Parameter	Sim(I)	Meas(I)	Units	Sim(II)	Meas(II)
Center Freq.	178	178	MHz	9	9
BW	20	20	MHz	5	5
Current	33	33.4	mA	33	33.4
Power Supply	+3.5	+3.5	V	+3.5	+3.5
Dynamic Range	30	24	dB	30	28
Control Voltage	1.5→3.5	0→2	V	1.5→3.5	0→2
Input/Output Match	<-15	<-15	dB	<-15	<-15
OP1dB	8.5	6	dBm	8.5	8
OIP3	18.5	16	dBm	19	18.8
Max. Group Delay Variation in BW	0.025	0.05	nsec	0.58	0.9

5.5.3 **Frequency Converters**

The two Converters (Figure 5.40) have been developed with the same architecture, but using different matching networks and design techniques, given that there was a factor of ten between the two working frequencies. Full description of the implementation of the two circuits is given in ([4.16]). Each MMIC includes five different functions: RF amplification, LO amplification, phase shifting, double balanced conversion and IF amplification. The mixers have been implemented with a FET resistive ring configuration due to its very low distortion and rejection of even-order inter-modulation products.

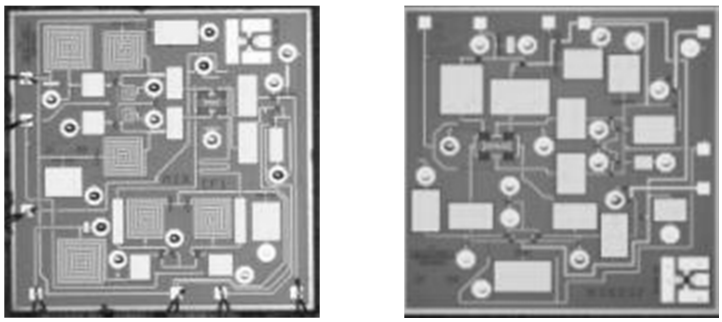


Figure 5.40: RF (left) and IF (right) converters

Differential amplifiers have been used at both the RF and LO ports as on-chip active baluns, enabling double balanced topology. A push-pull amplifier is used at IF to provide an active combination of the out-of-phase signals at the resistive mixer outputs, improving the gain and the efficiency of the converter. Only four pins have been left accessible for biasing and fine tuning (to improve post production yield).

The RF converter can be used with low level (2dBm) LO power, providing more than 5dB conversion gain and 3dBm P1dB, and maintaining very good LO/IF isolation, better than 35dB. Both gain and P1dB can be controlled by means of two pins, which provide flexibility during the integration, allowing adaptability to the transponder characteristics. The main simulation and measurement results are summarized in Table III. The yield of the chips meeting the specifications was about 90%.

Table 5.4:Results vs. requirements of the RF converter

Parameter	Simulation	Measurement	Units	
RF Frequency	2070	2070	MHz	
LO Frequency	2240	2240	MHz	
Current	45	46	mA	
Power Supply	+3.5	+3.5	V	
Conversion Gain	5.5	5.6	dB	Plo=2dBm
NF(SSB)	10	10.4	dBm	
OP1dB	3.6	3.1	dBm	Plo=2dBm
PSAT	4.6	4.8	dBm	Plo=2dBm
LO-IF Isol.	45.3	37.5	dB	RF Matched
LO-RF Isol.	50	45	dB	IF Matched

Table 5.5: Results vs. requirements of the IF converter

Parameter	Simulation	Measurement	Units	
RF Frequency	170	170	MHz	
LO Frequency	180	180	MHz	
Current	36.8	38.6	mA	
Power Supply	+3.5	+3.5	V	
Conversion Gain	21.5	21.8	dB	Plo=0dBm
OP1dB	1.3	1.0	dBm	Plo=0dBm
PSAT	4.3	3.7	dBm	Plo=0dBm
LO-IF Isol.	45.3	37.5	dB	RF Matched
LO-RF Isol.	50	45	dB	IF Matched

The IF converter is designed in order to provide high gain (>21dB), and output P1dB with 0dBm LO drive level. The gain can be adjusted with just one pin. The IF chip shows RF and OL bandwidths broader than 1GHz, which enables its use in different applications. A summary of the simulation and measurement results for the final circuits implementation are reported in Table 5.4 and Table 5.5 . The functional yield of both MMICs was about 85%.

5.5.4 **Oscillator and Multiplier**

The Voltage controlled oscillator and frequency multiplier have been obtained by optimizing and implementing in separate MMICs the preliminary versions of the circuits described in chapter 3 which were already fully functional. Details of the design of these circuits is out of scope of the present work as was object of a separate research activity, and only the main features of each implementation and performance will be reported hereafter for sake of completeness.

5.5.4.1 **VCO**

The Voltage Controlled Oscillator consists of a multifunction MMIC, which includes a negatron, a buffer amplifier, a power splitter and two output buffer amplifiers, along with an external resonator and a varactor tank circuit. This structure allows high degree of configurability in terms of output frequency and bandwidth. The general operational configuration and a photograph of the final circuit are shown in Figure 5.41 and Figure 5.42 respectively.

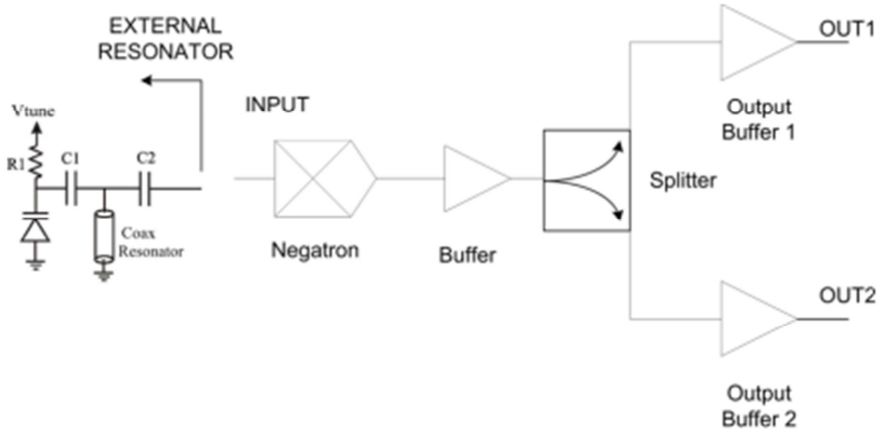


Figure 5.41: High level block diagram of the negatron with the resonant circuit

The topology is the same as the previous implementation but performance have been substantially improved with a reduction of power consumption of more than 25%.

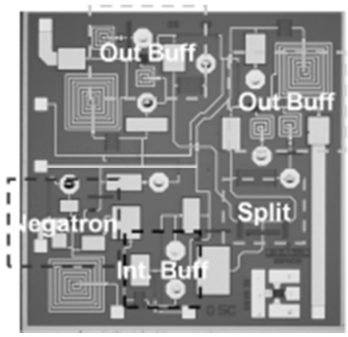


Figure 5.42: Microphotograph of the VCO MMIC

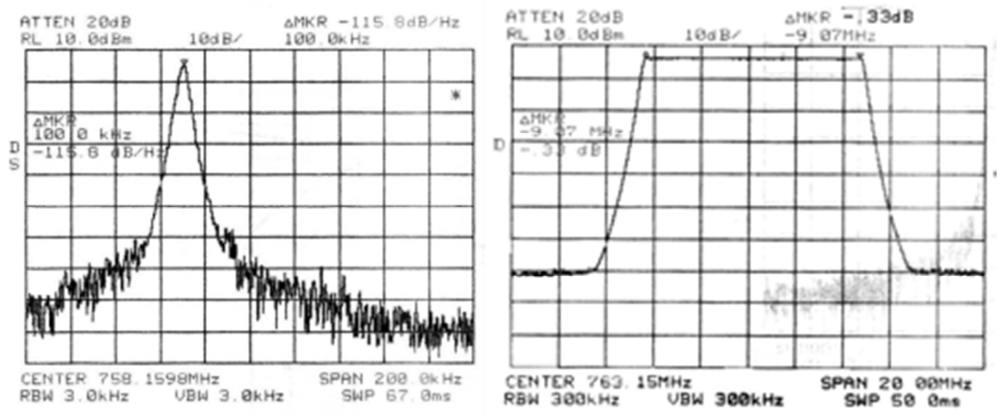


Figure 5.43: Measured Phase noise (left) and output power (righ) with a coaxial resonator

The negatron provides negative resistance from 256 MHz to 1830 MHz. The measured phase noise of the oscillator with an external coaxial resonator tuned at 700 MHz is around -115dBc/Hz@100KHz (Figure 5.43). This value is in line with the ones observed for the first implementation and is affected by the type of resonator used.

The output power is constant and higher than +5dBm for both outputs.

Simulation and measurement results are shown in Table 5.6. The yield of this chip was better than 90%.

Table 5.6: Simulation and measurement results for the negatron

Parameter	Simulation	Measurement	Units	
Negative Resistance Freq. Band	256 - 1830		MHz	
Current	29	35	mA	
Power Supply	+3.5	+3.5	V	
Pushing	0.003	N.A.	%	@Vcc±5%
Output power O1	6.9	5.9	dBm	Fout=700 MHz
Output power O2	6.8	5.8	dBm	Fout=700 MHz
Phase Noise	N.A.	-115	dBc/Hz	@100KHz
Isolation	73.4	N.A.	dB	Fout=700 MHz

5.5.4.2 FREQUENCY MULTIPLIER

The Multiplier (Figure 5.44) includes four different RF functions: a tripler, a buffer amplifier, a power splitter and two output buffers.

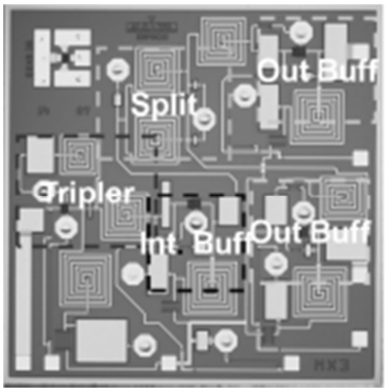


Figure 5.44: Photograph of the frequency multiplier

Also in this case, the frequency tripler MMIC used the same topology of the prototype circuit presented in chapter 3 consisting in transistor that works as a harmonic generator, whose bias point has been optimised to obtain maximum power at the third harmonic.

The measured output power is greater than 5dBm, whereas the 2nd harmonic output is 8.3dBc below the desired signal. This level can be further decreased by external filtering. A summary of the simulation and measurement results is given in Table 5.7. In this case the yield was around 80%.

Table 5.7: Simulation and measurement results for the frequency multiplier

Parameter	Simulation	Measurement	Units	
Input Freq. Band	660-780	660-780	MHz	
Current	58	49	mA	
Power Supply	+3.5	+3.5	V	
Input power	5	5	dBm	Fin=780 MHz
Output power O1	9.3	5.3	dBm	
Output power O2	9.2	5.3	dBm	
Harmonics	9	8.3	dBc	Worst case. 2nd harmonic

5.5.5 Dual Modulus Divider

The MMIC used to perform the variable frequency division within the MCM OL2K is based on the implementation which has been described in chapter 4.

Minor updates were required in the input buffers and logic cells for the flight version of the MMIC in order to further reduce the power consumption, avoid slight excess voltage in selected components to meet de-rating requirements [5.8] for space applications and reduce the stress in some critical components.

In particular, all the source follower current sources were modified by introducing a source degeneration resistor to further reduce the current source consumption (by modifying the biasing point without the need of introducing an additional bias voltage) and a gain equalizing network was added to the input buffer to ensure a similar sensitivity window for the two division ratios.

The resulting layout (photo is not available) is shown in Figure 5.45. It must be noted that even if the number of pads in the bottom part of the chip has been maintained, one is now connected to the output buffer to allow controlling the output power level. Both stages of the input buffer are now controlled by means of a single voltage.

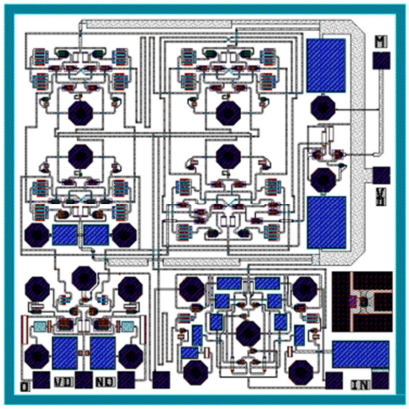


Figure 5.45: Layout of the dual modulus prescaler for the flight tests

Overall performance is in line with previous implementation. The new sensitivity windows are reported in Figure 5.46.

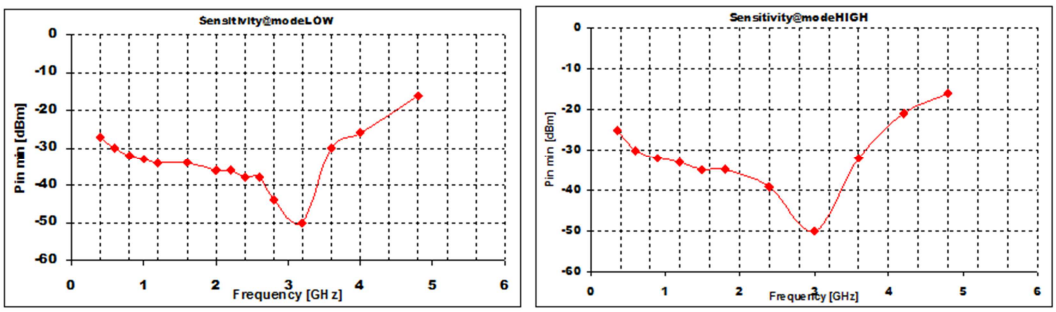


Figure 5.46: Dual modulus divider input sensitivity in divide-by four (left) and divide-by-three (right) mode

Unfortunately the flight run chips were sent directly for characterization to TAS-E and full details of the final measurements are not available. Based on the information received from TAS-E the final circuit´s performance is reported in Table 5.8 with an overall yield of 85%. The power consumption of 250mW represents a reduction of about the half with respect to the previously employed generation of prescalers, with additionally improved performance.

Table 5.8: Simulated results and measurement summary for the dual-modulus divider

Parameter	Simulation	Measurement	Units
Input Freq.	<400 - 4900	500 - 4500 (*)	MHz
Current	75	70 (**)	mA
Power Supply	+3.5	+3.5	V
Input/output Match	-10/-20	n.a	dB
Output Pwr	3.5	2-4	dBm
Division Ratios	3-4	3-4	

(*) Characterization limited to this frequency range
(**) Optimizing Buffer bias

5.5.6 **Medium Power VGA**

The amplifier design targets a medium power amplifier (MPA) with output power level control capability delivering an output power that can be configured by the selection of few external passive parts.

This circuit design was imposed by an update in the system specification (associated to a lower gain in the selected output power amplifier) which would have prevented the use of the RF VGA in the transmitting chain.

The main MMIC MPA characteristics can be summarized as follows:

- Nominal bandwidth of about 400 MHz centered at 2.1 GHz (target highest frequency of operation at 2.25GHz).
- Maximum Gain ≥35 dB and gain control range >10dB.
- Maximum Power Consumption 2W@3.5V

A summary of the full requirement specification is reported in the following table for sake of completeness.

Table 5.9: Medium power VGA specifications.

Símb.	Caracteristics	Goal			Units.	Conditions
		Mín.	Typ.	Max		
V_{cc}	Power Supply		3.5		V	Tolerance ± 3%
Pd	Power consumption			2	W	
F_{center}	Operating Frequency	1.9	2.25	2.3	GHz	10MHz signal Bandwidth
S11	Input match	-10			dB	at any Gain, 50Ω source
Z_{out}	MMIC Output Impedance		TBD		Ω	Impedance transformer to 50Ω if used shall be defined
G_{PMAX}	Maximum Power Gain	35			dB	V_{ALC}= Max gain
G_{PMAX}	Minimum Power Gain			27	dB	V_{ALC}= Min gain
GCR	VGA Dynamic Range	10			dB	V_{AGC}=Full
G_{FLAT}	Gain Flatness			0.3	dB	in the signal Bandwidth
G_{SLOPE}	Gain Slope			0.03	dB/MHz	in the signal Bandwidth
NF	Noise Figure			25	dB	@MAX Gain
P_{1dB}	Normal drive configuration Output Power at 1 dB gain compression	18			dBm	@ MAX Gain and nominal load
P_{1dB}	Normal drive configuration Output Power at 1 dB gain compression	24			dBm	at MAX Gain and nominal load
P_{SAT}	Saturated Output Power			30	dBm	at MAX Gain and Extended drive
Smx	Maximum input level			5	dBm	Overdrive analysis shall be provided

5.5.6.1 CIRCUIT DESIGN

The Amplifier is divided in three main stages (Figure 5.47): a first Variable Gain stage (two differential stages that provide most of the gain and the gain control functionality, plus a differential to single ended converter based on a push-pull topology), an inter-stage driver and the output buffer

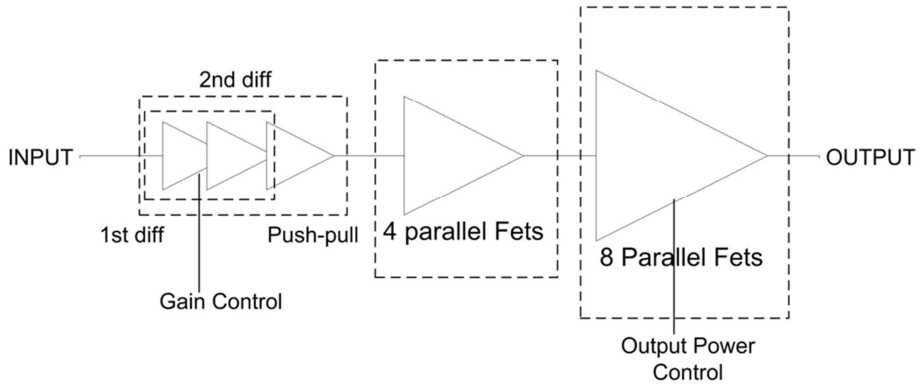


Figure 5.47: Block diagram of the MPA

To allow a flexible use of the amplifier in different configurations, the output matching has not been optimized to achieve the maximum output power in order to

reduce the thermal gradients with a design adapted to the process capabilities. The output working impedance was selected to be very low (about 5Ω) to reduce the drain voltage excursion to match with the fabrication process capabilities (which is not designed for very high power applications), as the process was selected to be common for the different transponder functions.

With the proposed solution, the transistors of the output stage are kept always well below the specified maximum ratings and within the space de-rating margins. By simply changing the value of a biasing resistor (Rp1dB in what follows) and the gate voltage of the last stage (Vl_{ow}), the output compression can be configured to a value of +19dBm (normal or *nominal drive*) up to +24dBm (*extended drive*). The reason of different biasing conditions study is to allow the MMIC to be used in different missions, indeed it is a design specification.

Some mission examples and its configuration:

- LEO, medium bit rate: output level up to 24dBm.
- GEO, medium to high bit rates (most common up to 10Mbps GMSK): output is 38dBm, uses the MMIC biased in normal drive (at 19dBm 1dB or lower) and a commercially available space qualified transistor as the output HPA elements.
- MEO/LEO links to relay systems: a low gain external HPA is used to reach 30dBm of output power and can use the same configuration that LEO.

In the following figures are reported the schematic of the different stages of the designed MPA.

The gain adjusting capability of the MPA is provided by the first amplifier by varying the gate voltage Vg1 (Figure 5.48). A differential configuration has been selected to provide backward compatibility with the I/Q modulator which could be used at the input of the MPA in Figure 5.1.

OUT1 and OUT2 in Figure 5.48 are inputs to the next differential stage while R_{ext} is an external resistor to control input match when the circuit is used in single-ended input configuration (as shown in the figure). To achieve maximum gain for the level control the transistors are operating at Vds ~1V. The biasing of this stage is controlled by V_{gdif1}, nominally at V_{gs}=0, setting Q_{d1} drain current to a DC level of about 8mA.

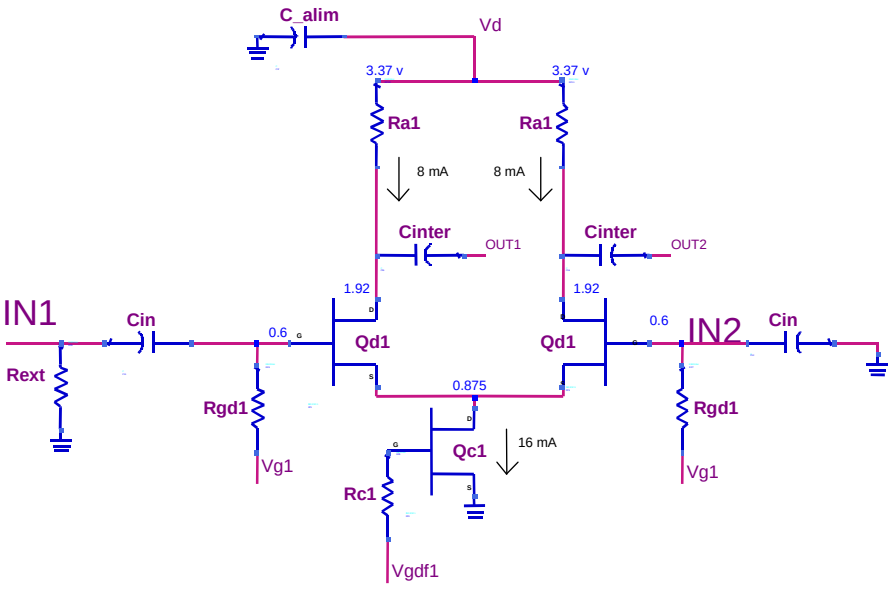


Figure 5.48: First Differential amplifier.

In Figure 5.49 OUT1 y OUT2 are inputs to the differential to single ended converter (push-pull). Also in this case maximum gain is obtained when transistors are operating at Vds ~1V. The biasing of this stage is controlled by V_{gdif2}, nominally at V_{gs}=0, setting Q_{d1} drain current to a DC level of about 16mA.

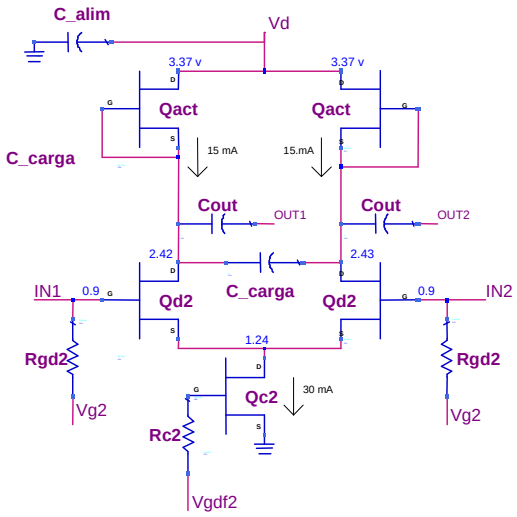


Figure 5.49: Second Differential stage

The push-pull stage (Figure 5.50) is used as a differential-to-single-ended amplifier (with around unity gain).The operating point is set by V_{gpp}, which should ensure that transistors´ operating point is around 0…-0.3V of V_{gs} and $V_{dd}/2$ of V_{ds}. At that point the current biasing of the push-pull is about 17mA.

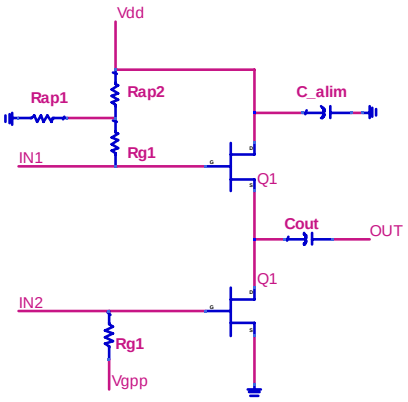


Figure 5.50: Third stage (push-pull)

The two resistors Rap1, and Rap2 are used as a voltage divider to fix the DC level at the output.

The overall DC current drawn by the first three stages including the two differential amplifiers and the push pull is about 60mA @V_{dd}=3.5V.

Once the signal is converted to single-ended, the power level is increased through a driver and an output stage. Each stage is composed by a number of parallel transistors, the number of which has been selected trading-off transistor to transistor dispersion and thermal reduction due to power split by more area usage.

The pre-amplifier stage is built-up of four parallel transistors (Figure 5.51). The same configuration is repeated in the four branches:

- Input de-coupling capacitor;
- A parallel RC equalizer;
- Gate bias resistance and drain RF choker;
- RC feedback to ensure broadband response.

The overall current consumption is set by an external biasing resistor (at the V_d supply pin) and the gate tuning voltage V_{gi}. In normal drive the drain resistor is 20Ω and current consumption is 17mA each transistor; 45 mA total. In extended drive the drain resistor is 10Ω and current consumption is 24mA each transistor; 91 mA total.

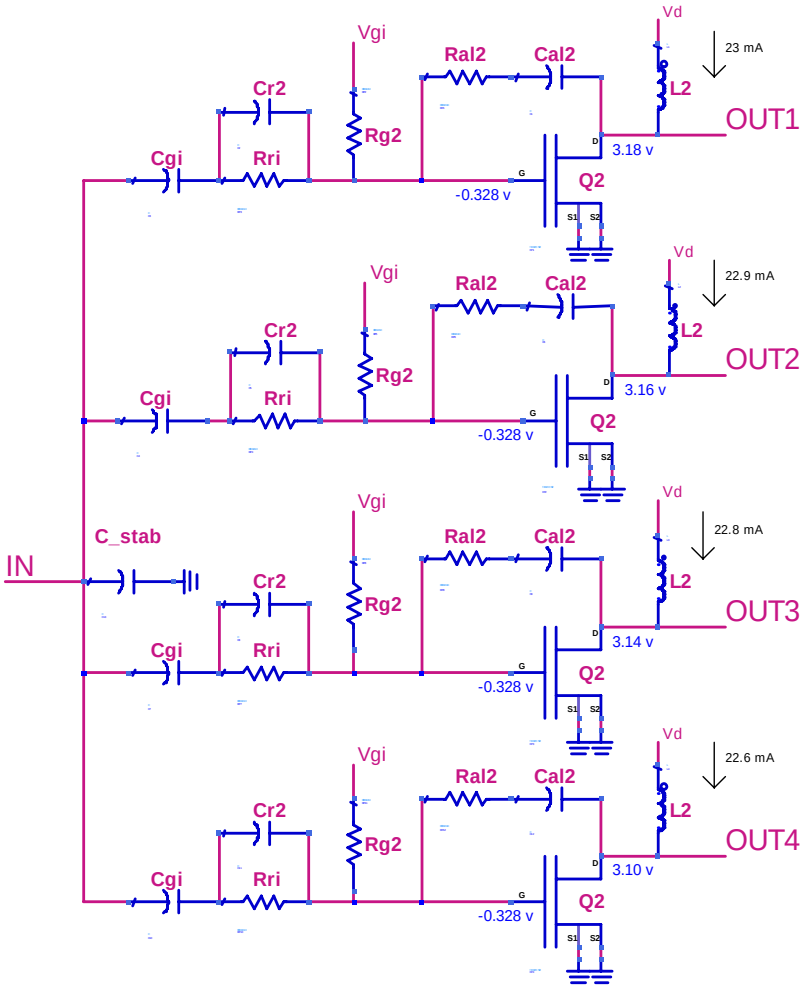


Figure 5.51: MPA Driver amplifier

Even if drain current is subject to transistor-to-transistor dispersion due to process parameter variations, the maximum extra current has been simulated to be of 12mA in the extended drive configuration. Simulations (sec. 5.5.6.2.4) confirmed that the feedback network compensates such dispersion and prevents from affecting the RF behaviour.

The last amplifying stage is in charge of providing the amount of output power to the load. Main design target has been to lower the transistor to transistor dispersion and to optimize the area used to spread the heat flux and reduce the thermal step. 8 “oversized” transistors have been used (Figure 5.52) in the output section to reach the required output power of 24dBm for the extended drive with enough margins to meet de-rating requirements. Further clarifications to numerically justify the transistor over sizing are provided in section 5.5.6.2.2.

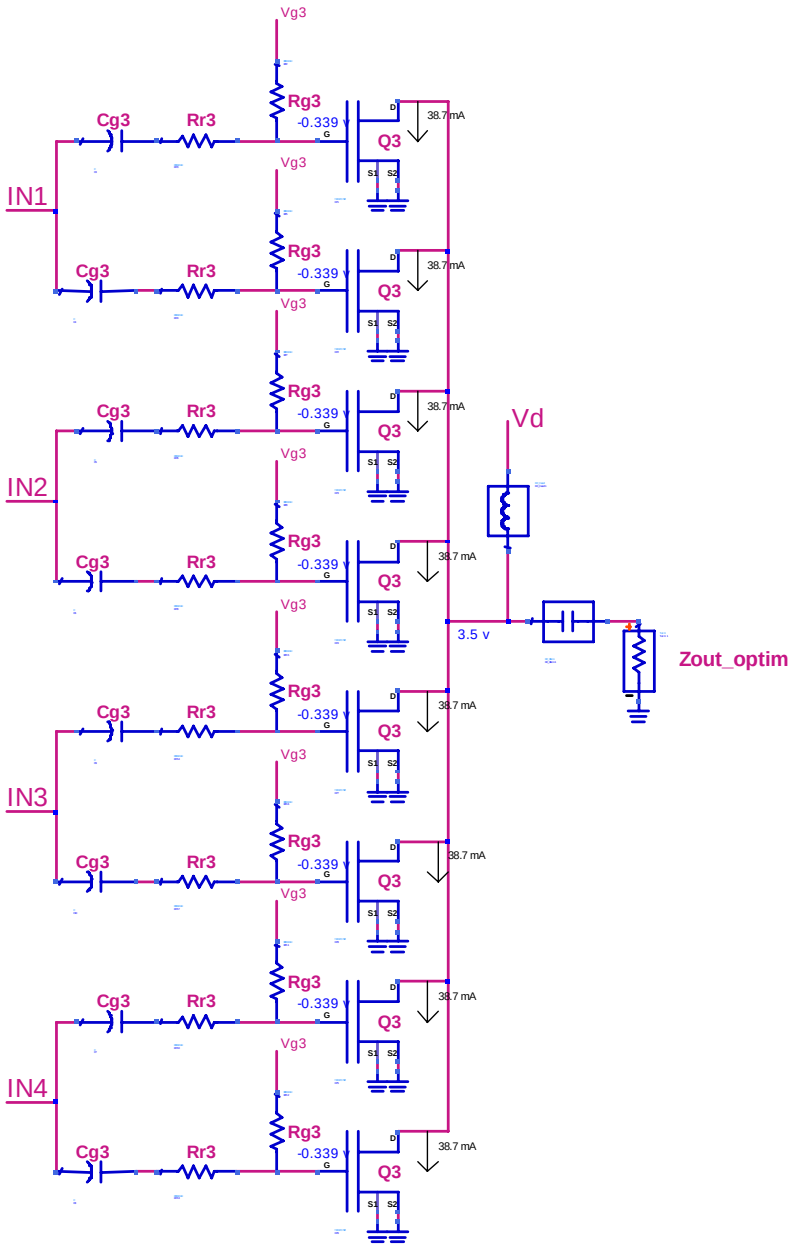


Figure 5.52: Output power stage

Also in this case the same configuration is used for the eight branches:

- Decoupling capacitor;
- Stabilizing resistor;
- Gate bias resistor.

The drain bias voltage is supplied through the output RF pad via an external inductor. To allow transistors to work with safer voltage levels, the Zout_optim is set to approximately 5Ω (the optimum value is determined through load-pull simulations) and

an external impedance matching network was implemented to transforms into 50Ω for testing purposes.

The overall current drive, when biased for the 19dBm case, is slightly less than 20mA each transistor; ~160mA total, with a drain external resistor of 2.8Ω (Vds=2.8V). For the extended drive case (fixed at 25dBm minimum to cope with possible implementation losses) the current consumption is about 40mA each transistor, then ≈320mA total current, with a drain voltage of 2.3V with the external resistor set to ~1.5Ω. Adjustment is made using Vg3. As described previously the drain current is possibly subject to dispersion due process variations, but the extra current is expected (section 5.5.6.2.4) to be less than 18mA for the highest drive biasing on a single transistor as worst case.

Summing up all the current consumption of the 3 stages of the amplifier we have a total current consumption of less than 500mA in the extended drive. Using an external 3.5V drain supply this is well below the targeted value of 2W even for the extended drive (less than 1W in normal operation).

The complete layout of the MPA MMIC is shown in Figure 5.53. The die size has been set to 3mm x 3mm to maintain a regular pattern in the wafer as the circuit was fabricated on the same wafer as the LNA described in section 5.5.1.

The input of the MPA is situated on the bottom left corner, where the input stages have been placed.

At the output of the amplifier, a power detector (top right, which will not be described in the present work) has been placed in order to facilitate the automatic gain control of the ISBT transmission module improving the integration level.

The layout of the driver and power stage has been fitted into a 2mmx2mm layout area (identified in the figure) as the final version of the circuit will be built-up by two 2mmx2mm chips, one containing the output stages and another containing the input amplifiers and the power detector.

In addition to the sections of the VGA and the power detector, it is included a test transistor for dynamic wafer evaluation in every chip, this PCM like transistor will allow a rapid wafer screening and the process evaluation.

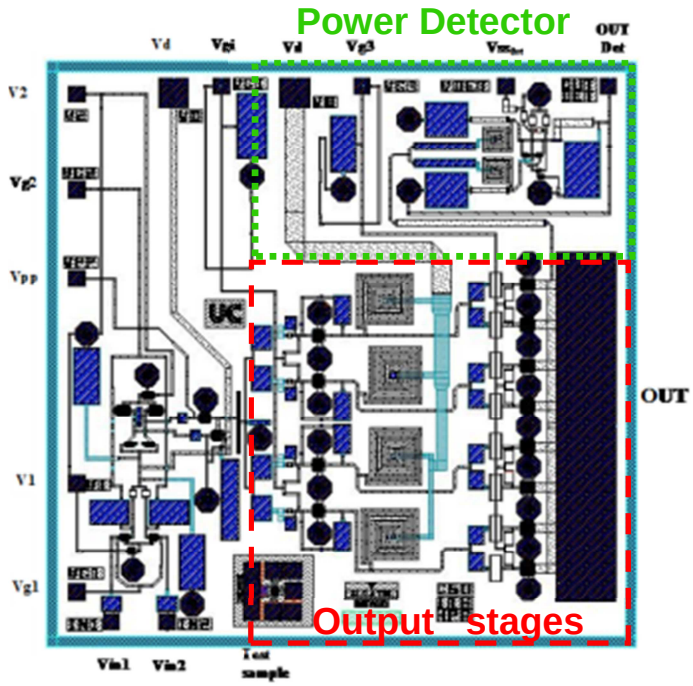


Figure 5.53: Layout of the fabricated circuit

5.5.6.2 SIMULATIONS

In the following sections, the results relatives to the most relevant simulations of the MPA will be presented. All the results have been obtained through ADS.

The value used for the external supply voltage has been fixed to 3.5V to be compliant with the available supply voltages.

The optimal load impedance has been selected with load-pull simulation test bench to allow the maximum output power in the extended drive configuration. Simplified schematic of the output matching network is illustrated in Figure 5.54.

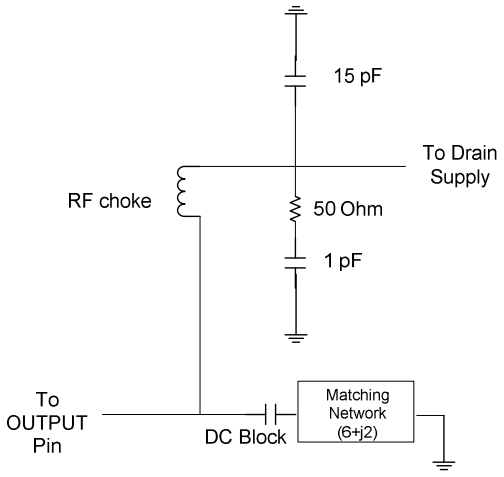


Figure 5.54: Schematic of the optimal output load and drain bias network

The external matching network that allows the impedance transformation to 50Ω can be implemented either by means of microstrip lines and lumped elements (an example of broadband network used in the simulations to cover the operating bandwidth is shown in Figure 5.55). The package model described in section 5.4 has been used throughout the simulations to take into account the effects associated to the final assembly on the package.

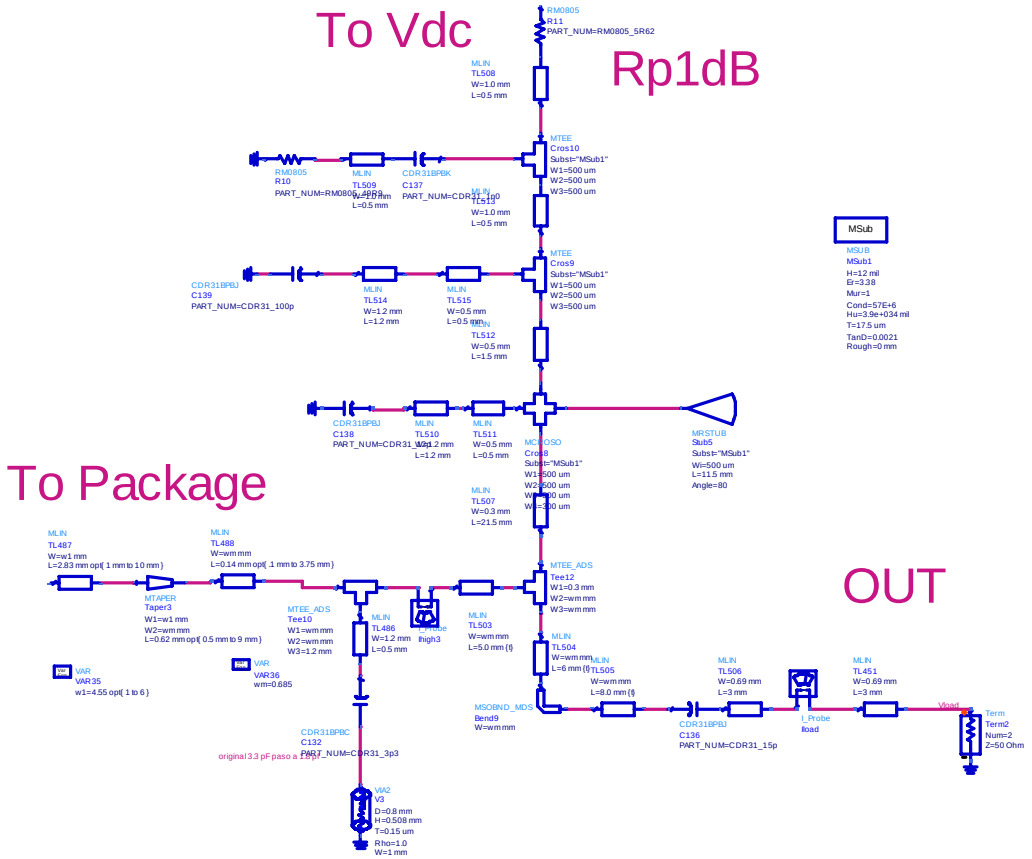


Figure 5.55: Output matching Network used in simulation

5.5.6.2.1 Small and Large signal Simulations

The results of the simulations will be illustrated only for a limited set of test cases as the full analysis is far too extensive and would not bring added value for the scope of the present work. Details of the simulated differences between the two cases will be addressed on a case-by-case basis.

The MPA gain range is controlled by changing the value of Vg1 from 0.6V (Max. Gain) to ~1.55V (Min. Gain) even if lower gain values can be obtained for higher values of Vg1. The simulated dynamic range can reach 20dB for both cases, even if

most of the simulations have been carried out keeping the $V_{control}$ between 0.6V and 1.4V which is sufficient to cover the requested gain variation range. Varying the temperature between -30º and +70º only affects the dynamic range (±2dB) and the maximum gain (±1dB), maintaining the circuit performance well above the design target.

Results of the scattering parameters simulations at 25º are reported in Figure 5.56 and Figure 5.57. Input/output match is reported only for one case as the result are substantially the same. Output load was set to the optimal power load.

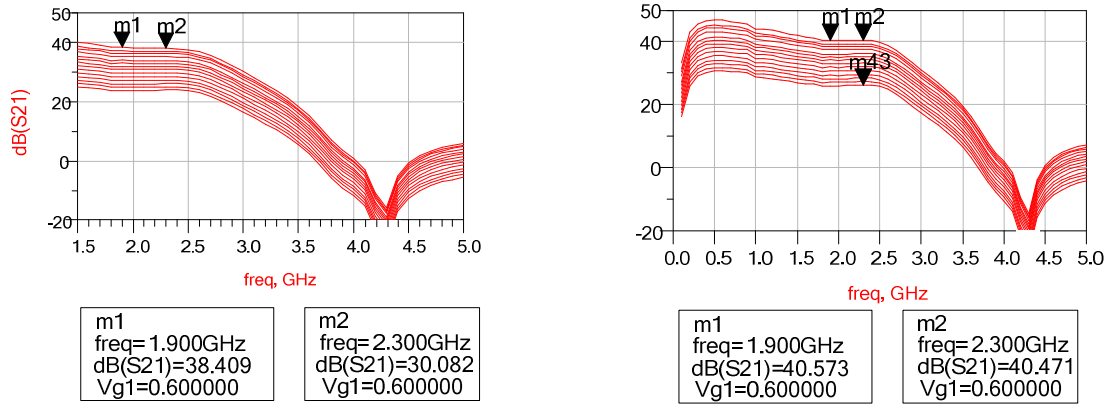


Figure 5.56: Small signal gain variation as a function of the control voltage Vg1=0.6-1,4V) at 25º. Normal drive (left) and extended drive (right)

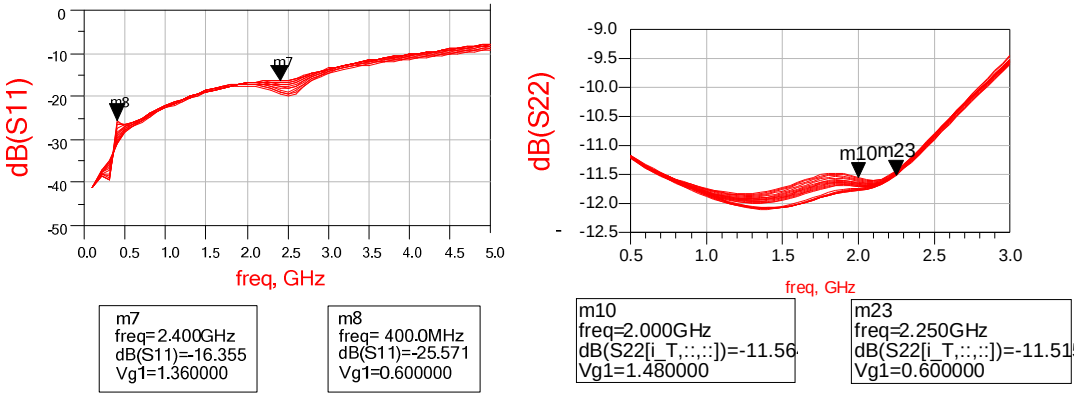


Figure 5.57: Input (left) and output (right) match (extended drive) as a function of the control voltage (Vg1,V) at 25ºC

The input match is mainly driven by the input external resistors driving the input differential amplifier (R_{ext} in Figure 5.48) when used in single ended configuration. Output match can be adjusted for each specific application simply by changing the

matching network (Figure 5.55) with a narrowband network targeting the specific application.

Variation of the Maximum Gain with temperature, are reported in Figure 5.58 for the extended drive configuration. Results for the normal drive conditions are analogous but with a lower maximum gain of 38dB at room temperature.

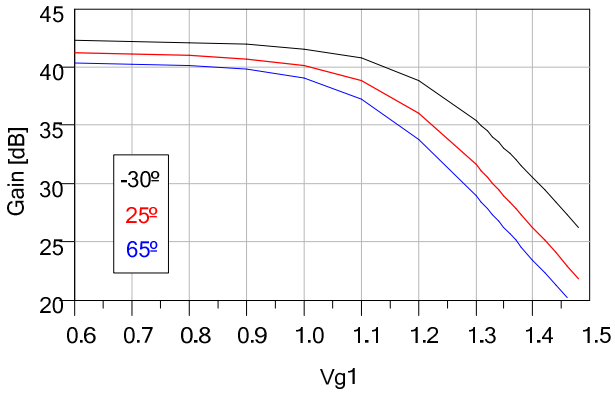


Figure 5.58: Gain dynamic range as a function of the control voltage at three temperatures for the extended drive configuration.

The stability simulations include the modeled package and ground effect for unconditional stability. Mu, Mu', and Rollet stability have been evaluated at the different temperatures and for each value of the control voltage, but only the worst case (T=-30ºC, extended drive) is displayed (Figure 5.59).

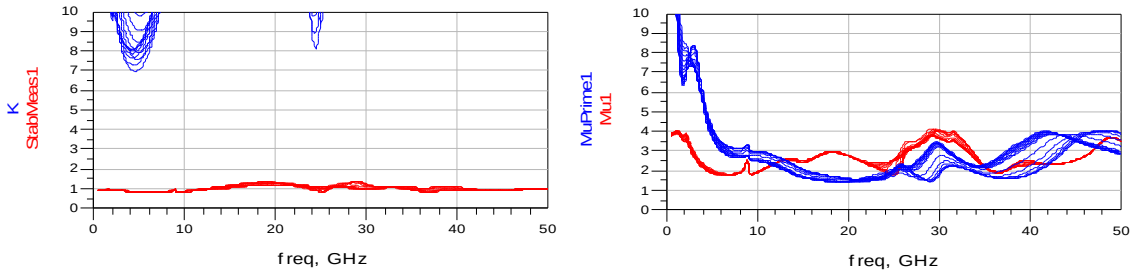


Figure 5.59: Stability parameters in the worst case (T=-30ºC, extended drive) as a function of the control voltage

The circuit behavior has been simulated for increased parasitic inductance, to double check the stability not only for the amplifier itself but to characterize the circuit tolerance to the presence of potential parasitic inductances associated to the imperfect assembly on the ground plane. Temperature of –30C is selected for the simulation as the lowering the temperature tends to reduce stability margins. As reported in Figure 5.60,

the circuit remains stable for inductances values up to 0.035nH, four times higher the expected attachment plus package inductance parasitic effect (which is around 0.008nH in the case of power epoxy, sec. 5.4) hence ensuring a quite large safety margin.

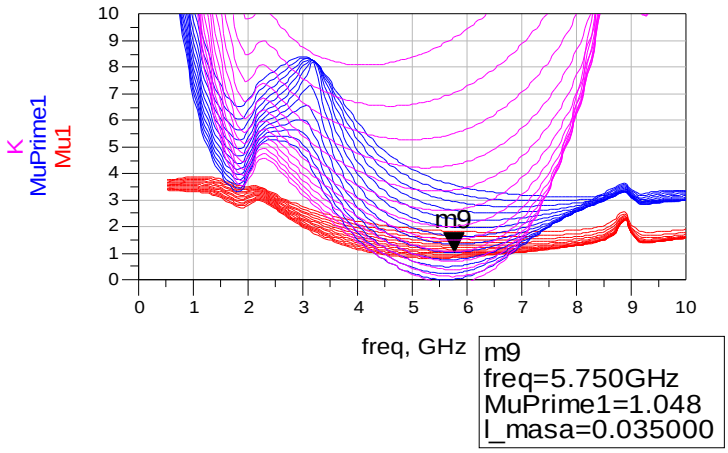


Figure 5.60: Stability parameters in the worst case (T=-30ºC) as a function of the control voltage for different value of the parasitic ground inductance (sweep: [0.01-0.1nH]).

Large signal HB simulation results are illustrated in Figure 5.61 and Figure 5.62 for the extended drive bias. The MPA control voltage was varied to monitor P1dB evolution at the different gain settings. It can be noticed (Table 5.10) how the P1dB is quite insensitive of the Gain control point. The 1dB compression point is evaluated at 2.25GHz but remains within ±0.5dB for the same bias settings along within a >50MHz span.

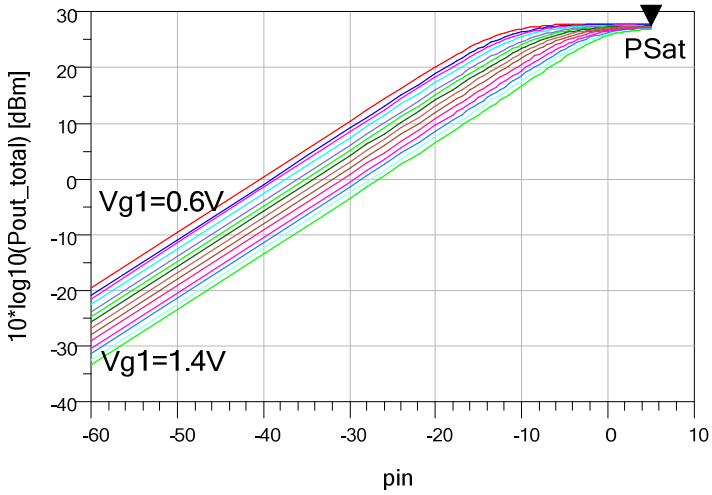


Figure 5.61: Pin-Pout curve (extended drive) as a function of the control voltage at room temperature. Psat=27.5dBm.

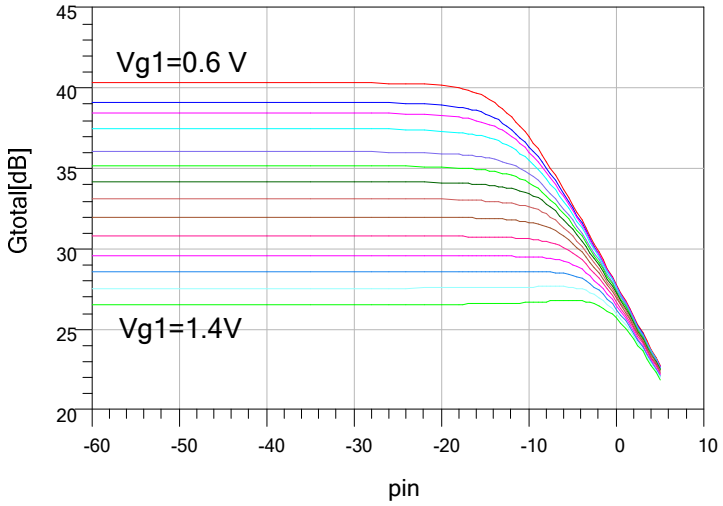


Figure 5.62: Power gain (extended drive) as a function of the control voltage (vg1=0.6-1,4V) at room temperature.

Table 5.10: Power Gain and 1dB compression values for different control voltages (fin=2.25 GHz)

$V_{control}$	Gain	P1dB
0.6	40.46	24.8
1.0	39.13	24.7
1.1	37.4	24,5
1.2	34	24.7
1.30	29.1	25.0
1.35	27.5	25.5
1.4	26.1	25.8

The simulated performance variation with temperature is minimum (±0.6dB). In normal drive, the saturated output power is 25dBm and similar performances as in the extended drive configuration are observed around 19dBm of P1dB.

5.5.6.2.2 Component stress

Maximum ratings for the pHEMT transistors in the selected technology are detailed in the following table (similar considerations have been applied to all the circuits presented in this work and to all the components used both active and passive). In principle each of parameter should be checked in the worst case operating conditions with limit imposed by EECS de-rating standard [5.8]. This has been extensively checked for all the components (not only transistors) and for the different operating

conditions. Only some relevant results will be detailed in this section whereas in reality the same tests have been applied to all the components in all the circuits.

Table 5.11: Maximum ratings for OMMIC pHEMT transistors

Limited param.	Unit	Value for "ON" devices	Value for "OFF" devices
Vds	DC V	4	4
Vds	RF Peak V	7	7
Vgd	DC V	-5	-5
Vgd	RF Peak V	-7	-7
Vgs	DC V	-5 to +0.9 (check the maximum current)	-5 to +0.9 (check the maximum current)
Vgs	RF Peak V	-6 to +1.0	-6 to +1
Ig	DC mA/finger	0.45	0.45
Ig	RF Peak mA/finger	1	1
Power	DC mW/µm width	0.6	0.6

Maximum DC power consumption for a transistor is set to 0.6 mW/um. To be compliant with the ECSS de-rating for a FET, the maximum DC power consumption shall be kept always below 80% of the maximum rating. In the case of the last stage 8x50um transistor (Pd = 0.6 *400um = 240mW) this means a maximum de-rated power value of 192mW.

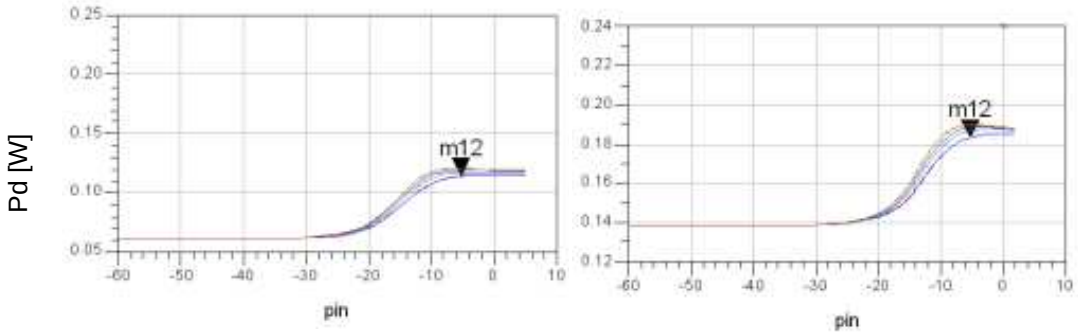


Figure 5.63: Power consumption as a function of the input power overdrive for the output stage transistors with the MPA configured for Max, Gain . Normal (left) and Extended (right) drive. Previous stage consumption is not affected.

The worst cases of dissipated power in the normal and extended drive situation have been simulated (Figure 5.63) for a Pin=+5dBm (overdrive, more than 15dB of compression) and maximum gain giving 125mW (<100mW@p1dB) and 190mW(<180mW@P1dB) in normal and extended drive respectively, so in both cases meeting the de-rating requirement well above the normal operating conditions (assumed to be below the P1dB point), especially for the normal case which represent the

common configuration for the amplifier (the extended drive is intended for use only is specific and experimental configurations).

The maximum safe RF Vds excursion is 7 Volts. In this case [5.8] imposes a 75% de-rating resulting in 5.25 Volts as maximum safe operating voltage. As shown in the load contours plots of Figure 5.64 it can be noted that 4.4 Volts is obtained as max Vds excursion in the normal drive case and 5.5 Volts in the Extended drive operation with 15dB compression (DC value is always well below the de-rated value of 3V). In this case the overdrive with 5dBm input power can cause some stress in the last stage transistors in extended drive, however at P1dB 3.6 Volts is reached for normal drive and 4.2V in extended drive operation at less than 60% de-rating.

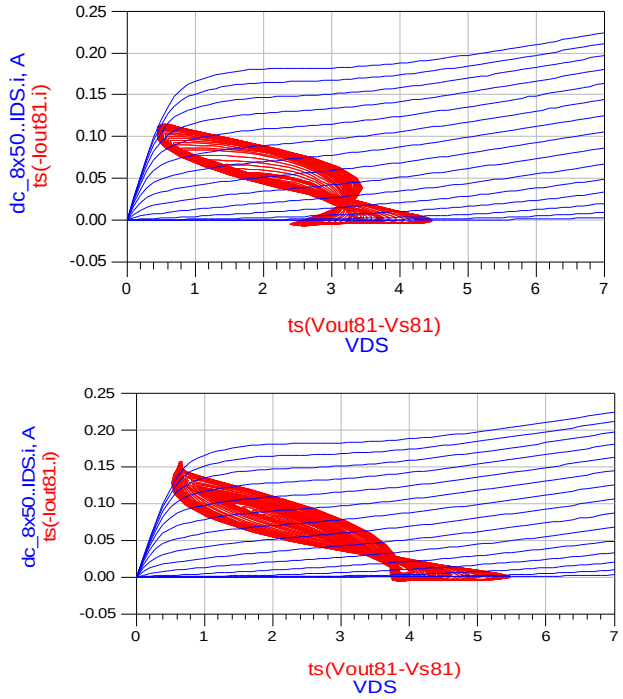


Figure 5.64: Load contours last stage transistors as a function of the input power

Similar analysis have been carried out for all the circuit components of the MPA, and for all the parameters demonstrating that EECS de-rating are met with a huge margin in normal drive, but that the design allows for its safe use also for the extended drive, making the designed amplifier suitable for a plurality of applications.

5.5.6.2.3 Yield

Yield figures have been evaluated for small signal and large signal performances. In small signal, main parameters to be monitored were the maximum gain and the gain

control range sensitivity with process variations, whereas in large signal simulation 1dB compression point sensitivity.

Small signal analysis specifications were set to achieve a >39dB gain (only extended drive is reported). Results are shown in Figure 5.65. As far as the gain control range is concerned, all the samples were able to provide at least 15dB of control range.

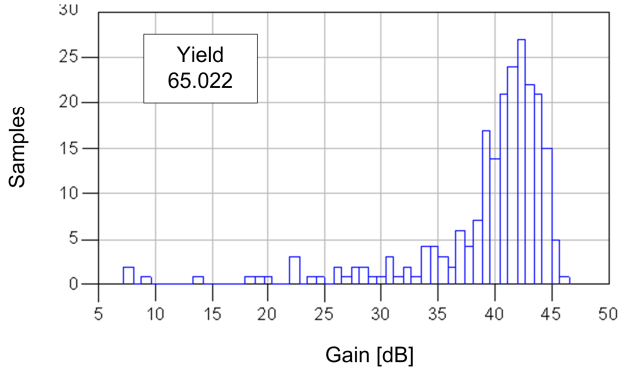
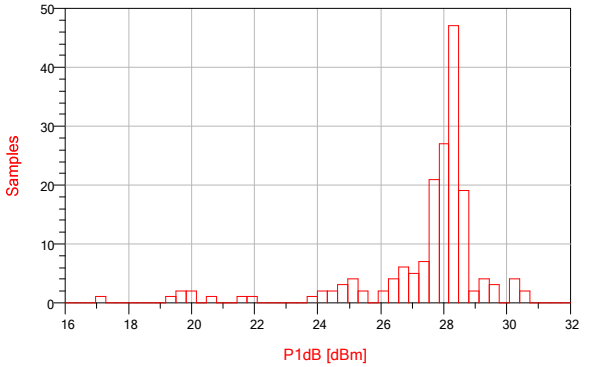


Figure 5.65: Small signal yield results without Post Production Tuning. Number of trials=250. S21 histogram relative to the mid-band frequency (2.25GHz) value

The large signal yield results refer to XdB simulations performed with ADS at room temperature. The specifications were set to obtain an output P1dB higher than 25dBm at the upper frequency where the performance is slightly worst.



numpass_tot	numfail_tot	yield_tot
150.000	20.000	88.235

Figure 5.66: XdB yield results. Number of trials=170. Histogram relative to the output compression 1dB at 2.25GHz and room temperature without Post Production Tuning

Either small signal or large signal yield results can reach values very close to 100% through proper post production adjustments acting on the accessible control voltages and/or on the matching networks. Additionally it must be noted that all the simulations

have been carried out with an output broadband matching network which offers a compromise performance throughout 300MHz operating bandwidth (in normal operations the MPA will be used in 50MHz bandwidth).

5.5.6.2.4 Amplifier stages dispersion

In the case of the MPA, special care has to be taken in order to ensure that the dispersion of process parameters across the chip will not cause an excess of heating in some of the transistors and keep all the devices within the de-rating specifications.

The dispersion simulations take into account measured dispersion values on previous wafer of process variation within any two circuits across the wafer and the dispersion between two adjacent dies (to have an upper bound of the dispersion between two adjacent transistors). Those results have been obtained thanks to the inclusion in every die of a PCM transistor to evaluate and confirm the process performances against the value claimed by the manufacturer.

The absolute value dispersion is evaluated on the variation of the transistor's threshold voltage (V_t): the parameter which mostly affects performance of all the circuits and was normally used to select compliant or non-compliant dies. Dispersion on the threshold voltage is quite large (varying from -0.65V to -0.99V) if compared on different wafers, however the wafer-to-wafer dispersion is not the driver for the wafer homogeneity as the target is mainly to bound the dispersion of transistors spaced less than 100um of the same wafer (the case of the MPA).

As an example, Figure 5.67 summarizes the absolute V_t dispersion of data collected from the PCM test transistors within any dice in 2 different fabrication runs with the selected process. The sample is based on 225 tested dies, the computed mean is 0.78V.

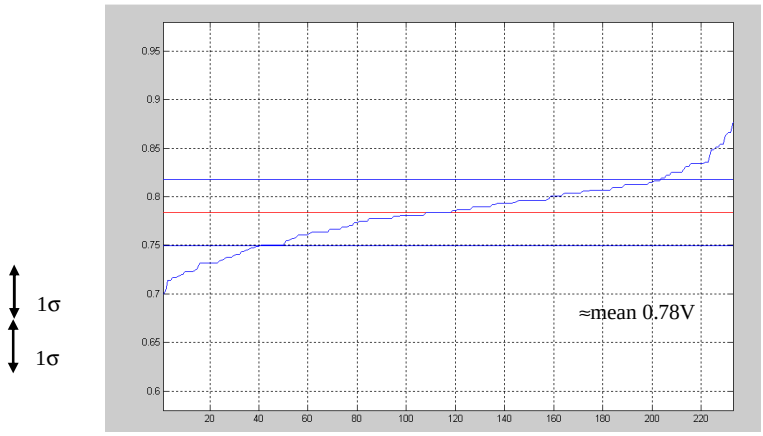


Figure 5.67: /Vt/ distribution across all measured PCM transistor samples.

The measured results indicate about 4% 1 σ dispersion, however a 3% bound was taken after evaluating the relative position on the wafer and considering the variation between two adjacent parts. These results are quite conservative with respect to the real circuit behaviour for what concerns the dispersion, as the real spacing between MPA transistors is much lower than the spacing between test transistors (~200um in the last stage vs. the 3.5mm of PCM transistor spacing). Dispersion is likely to be lower, but the modelling was based on the available data.

For the dispersion performance calculation, it has been assumed as a worst case that of one out of 8 transistors in the last stage to have the maximum measured variation of V_t (3σ=0.21V, even if the worst measured variation between adjacent dies was less than 2σ) while the other 7 maintaining the mean value. This represents the worst case as any other combination will reduce the drain current from the deviated selected transistor. The excess of current from that transistor has been used to evaluate the delta power and the additional de-rating (if any) to be applied to account for the extra drain current and the delta temperature to check any appreciable thermal stress.

With the nominal transistor parameter setting, the circuit is biased at the nominal and extended cases:

- Nominal bias : I_d (total for 8 trans) ≈160mA /V_{ds} =2.5V for P_{out} 19dBm
- Extended drive bias: I_d (total for 8 trans) ≈ 320mA /V_{ds} =2.8V for P_{out} 25dBm

Only the extended drive case is analyzed as represents the worst case bias. Once the transistors have been configured with the "worst dispersion" configuration (7 transistors with -0.78V V_t, and one with -0.99V V_t) two cases have been analyzed: one without re-tuning the bias and a second forcing biasing to readjust to the nominal 320mA current (more realistic as in normal operating condition an active external biasing circuit is being implemented to maintain constant the current).

It was checked through easy DC simulations that the "deviated" transistor presents a maximum of 18mA extra current. This amount is inside budgets as transistor is sized to withstand those extra current safely along with the extra power. Similar results, with an extra current of maximum 12mA were carried out also for the driver stage. Simulations carried out with those dispersions indicate minor P1dB and gain dispersion thanks to the feedback and RC networks which have been used across the amplifying stages.

5.5.6.2.5 Thermal Dissipation

As the MPA design makes use of a technology which is not intended for power applications (and GaAs is a quite bad thermal conductor) it was important to evaluate if the power levels at which the device will be operating can cause transistor overheating.

A detailed thermal dissipation analysis of each element has been carried out to verify that the power is dissipated correctly by checking that the temperature of the upper side of the chip corresponds approximately with the bottom side temperature to ensure a proper heating flux toward the backside heat-sink. The results depend on the size of the device as well as on the temperature of operation, the input and output power and the DC power consumption.

The temperature rise of a device of thermal resistance R_{th} (ºC/W) and dissipating an effective power P_d (W) can be obtained by:

$$\Delta T = R_{th}\left(^{o}C/W\right) * P_d\left(W\right) \tag{5.1}$$

The thermal resistance of a transistor depends on the total gate width W_{tot}, the number of gate fingers N_{bd}, and the gate to gate spacing:

$$R_{th}\left(^{o}C/W\right) = K_{edge}\frac{R_{tho}\left(^{o}Cmm/W\right)}{W_{total}\left(mm\right)} \tag{5.2}$$

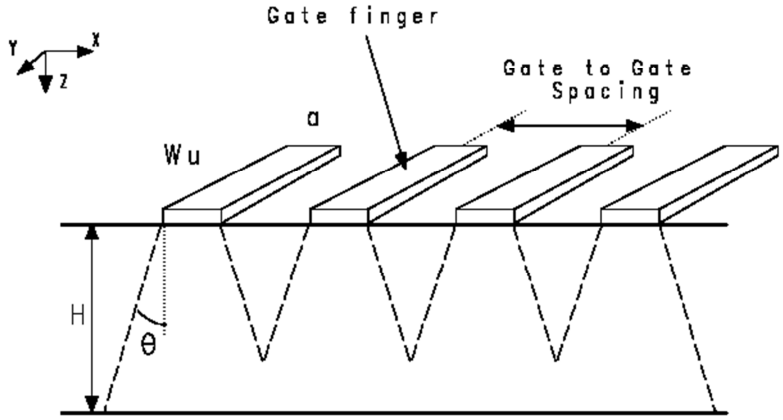


Figure 5.68: Schematic cross section of a multi-finger transistor. Each finger is a heating element of width $Wu = W_{tot}/N_{bd}$ (a=15µm for the selected technology)

The effective dissipated power is given by:

$$P_d(W) = P_{dc} + \sum(P_{in(W)}) - \sum(P_{out(W)}) \tag{5.3}$$

R_{tho} is the Thermal resistance Normalized to 1mm and K_{edge} is the thermal resistance decrease due to the edge effect along the Y-axis. Both values are provided by the MMIC foundry manuals (Figure 5.69 and Figure 5.70) as a function of transistor layout (e.g. number and length of fingers) and geometry (e.g. gate to gate distance).

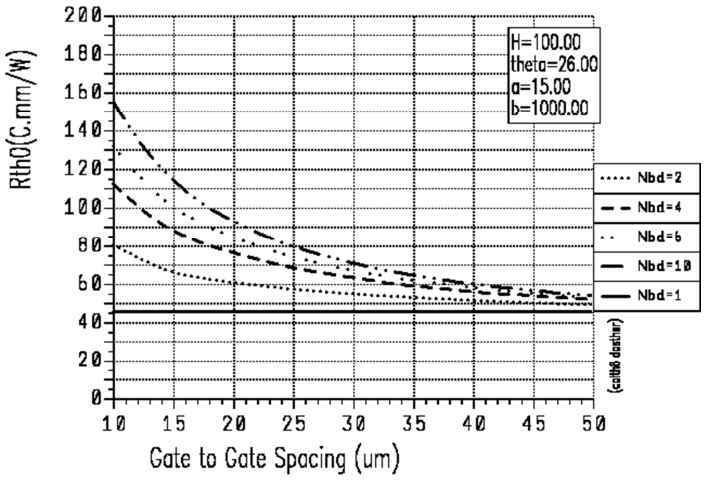


Figure 5.69: Normalized thermal resistance as a function of device geometry.

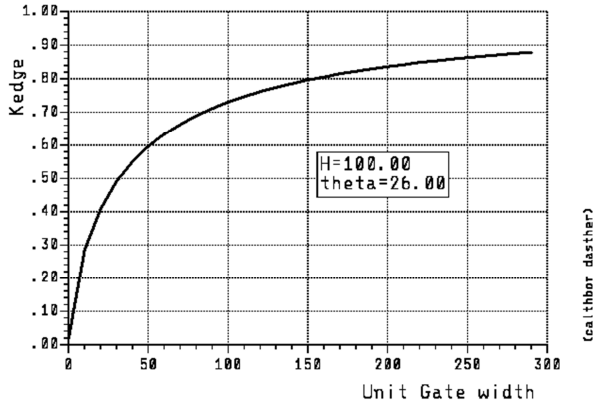


Figure 5.70: Thermal resistance decrease for an OMMIC transistor due to the edge effect along the Y-axis

However, as the thermal resistance of GaAs depends on temperature, equation (5.1) should be integrated along the heat flow. The exact heat flow calculation is not provided on the foundry design manual, but it can be demonstrated that the channel temperature can be approximated as:

$$T_{top(K)} = T_{bot(K)} \cdot \exp\left(\frac{R_{th}(T_o) \cdot P_d}{T_o(K)}\right) \tag{5.4}$$

T_{bot} is the backside temperature, T_{top} is the device temperature, P_d is the total power dissipated by the device, T_0 is the ambient temperature, and $R_{th}(T_0)$ can be deduced using (5.2).

The calculations of thermal dissipation for each transistor of the MPA at 2.25 GHz are shown below. The results are presented at maximum and minimum gain and the power dissipated P_d is calculated at 1dB compression. Normal drive operation for the worst case (85º ambient temperature) is presented.

Thermal resistance for a transistor of the last stage (8x50μm) is 210 ºC/W, this value does not take into account the source vias and the output pad thermal reduction (about 75 K/W) hence the results can be considered as an upper bound.

Table 5.12: Thermal calculations for the last stage transistors. T=85º C @ P1dB

FETs	R_{th} (ºC/W)	P_d (W)		ΔT		T_{top}/T_{bot}	
		G_{max}	G_{min}	G_{max}	G_{min}	G_{max}	G_{min}
Q1	210	0.101	0.137	18.191	28.754	1.052	1.084
Q2	210	0.100	0.137	18.150	28.693	1.052	1.083
Q3	210	0.105	0.142	18.738	29.876	1.054	1.087
Q4	210	0.105	0.142	18.729	29.858	1.054	1.087
Q5	210	0.107	0.146	19.127	30.630	1.055	1.089
Q6	210	0.107	0.146	19.125	30.625	1.055	1.089
Q7	210	0.093	0.149	19.535	31.300	1.056	1.091
Q8	210	0.093	0.149	19.576	31.351	1.056	1.091

The thermal resistance for a transistor in the driver stage (8x30μm) is 262.5 ºC/W and thermal calculations are shown hereafter:

Table 5.13: Thermal calculations for the driver stage transistors. T=85º C @P1dB

FETs	R_{th} (ºC/W)	P_d (W)		ΔT		T_{top}/T_{bot}	
		G_{max}	G_{min}	G_{max}	G_{min}	G_{max}	G_{min}
Q4_1	262.5	0.033	0.038	8.751	10.059	1.025	**1.028**
Q4_2	262.5	0.033	0.038	8.641	9.913	1.024	**1.028**
Q4_3	262.5	0.032	0.037	8.505	9.743	1.024	**1.028**
Q4_4	262.5	0.032	0.036	8.295	9.492	1.023	**1.027**

The calculations have been repeated for the overdrive case (Max. Gain, Pin=+5dBm).

Table 5.14: Thermal calculations for the driver stage transistors. T=85º C @ Pin=+5dBm

FETs	R_{th} (ºC/W)	P_d (W)		ΔT		T_{top}/T_{bot}	
		G_{max}	G_{min}	G_{max}	G_{min}	G_{max}	G_{min}
Q1	210	0.165	0.141	34.626	29.643	1.102	1.086
Q2	210	0.165	0.141	34.617	29.587	1.101	1.086

Q3	210	0.169	0.147	35.437	30.775	1.104	1.090
Q4	210	0.169	0.146	35.419	30.757	1.104	1.090
Q5	210	0.171	0.150	35.809	31.521	1.105	1.092
Q6	210	0.171	0.150	35.808	31.517	1.105	1.092
Q7	210	0.172	0.153	36.049	32.171	1.106	1.094
Q8	210	0.172	0.153	36.049	32.216	1.106	1.094

Table 5.15: Thermal calculations for the driver stage transistors. T=85º C @Pin=+5dBm

FETs	R_{th} (ºC/W)	P_d (W)		ΔT		T_{top}/T_{bot}	
		G_{max}	G_{min}	G_{max}	G_{min}	G_{max}	G_{min}
Q4_1	262.5	0.045	0.039	11.747	10.247	1.033	1.029
Q4_2	262.5	0.044	0.038	11.465	10.094	1.033	1.029
Q4_3	262.5	0.042	0.038	11.147	9.916	1.032	1.028
Q4_4	262.5	0.041	0.037	10.748	9.657	1.030	1.027

In this specific case transistors can be treated as independent and without correlation (because they are spaced more than 100um due to the presence of the via-holes in the layout, Figure 5.53). The worst case power values are observed (as it was to be expected) for G_{max} and overdrive (Pin=+5 dBm) in the last stage with ΔT of more than 36 º C. According to the ECSS standard the maximum FET channel temperature should be maintained below 125º, implying maximum T_{bot} of 89º C for overdrive and G_{max}. In nominal P1dB operation @ G_{min} a ΔT of 31º is calculated so max value for T_{bot} is 94ºC. For the driver stage the maximum increase is less than 12º hence a maximum T_{bot} in excess of 110 ºC can be assumed.

The increase of temperature in each sub-circuit has been also calculated on the assumption that each block (input VGA stage, driver, output stage) has no correlation with the others.

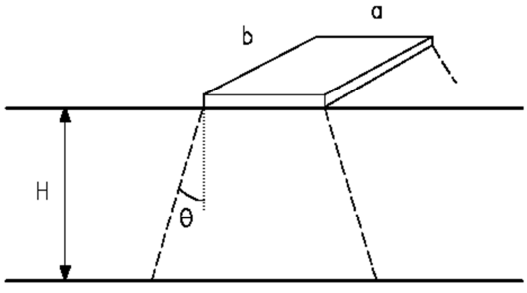


Figure 5.71: Simplified assumption for the thermal calculation of a sub-circuit

In this case the thermal resistance is calculated through the following equation:

$$R_{th}(^{o}C/W) = \int_{0}^{H} \frac{dh}{K_{th} \cdot Area} = \frac{1}{K_{th}\, 2tg\theta (b-a)} \ln\left(\frac{1+\frac{2Htg\theta}{a}}{1+\frac{2Htg\theta}{b}} \right) \qquad (5.5)$$

K_{th}: GaAs thermal conductivity→ above 100K K_{th} = 132/T ; K_{th} = 0.44295 W/Kcm @ 25ºC

H: Substrate thickness (100 μm).

θ: spread angle of the heat flow (26 degrees for a 100μm GaAs wafer)

The rest of the equations are the same that for the individual transistor. Results for the 3 sub-circuits are detailed in the following tables.

Table 5.16: Thermal calculations for the 3 stages of the MPA. T=85º C @ P1dB

FETs	Area (a cm x b cm)	R_{th} (ºC/W)	Pd (W)		T_{top}/T_{bot}		ΔT	
			G_{max}	G_{min}	G_{max}	G_{min}	G_{max}	G_{min}
Input VGA	0.1800 x 0.0950	8.648	0.198	0.204	1.005	1.005	1.018	1.765
Driver stage	0.1200 x 0.1700	8.012	0.131	0.143	1.003	1.003	1.047	1.143
Output stage	0.0800 x 0.1800	9.328	0.695	1.098	1.018	1.029	6.485	10.238

Table 5.17: Thermal calculations for the 3 stages of the MPA. T=85º C @ Pin=+5dBm

FETs	Area (a cm x b cm)	R_{th} (ºC/W)	Pd (W)		T_{top}/T_{bot}		ΔT	
			G_{max}	G_{min}	G_{max}	G_{min}	G_{max}	G_{min}
Input VGA	0.1800 x 0.0950	8.648	0.209	0.204	1.005	1.005	1.808	1.764
Driver stage	0.1200 x 0.1700	8.012	0.157	0.144	1.004	1.003	1.258	1.156
Output stage	0.0800 x 0.1800	9.328	1.304	1.130	1.035	1.030	12.166	10.543

As a conclusion it is possible to say that for a sub-circuit the worst case is in overdrive condition at 85º C, where the last stage can have a ΔT of 12.166 º which is much less than the single transistor case as was to be expected as the main thermal path is below the transistor fingers.

The thermal resistance and contribution of the selected mounting components is illustrated in the following table.

LAYER	l: (in m)	l: (in um)	k: (in W/m.ºK)	A: (in um2)	A: (in um2)	Rth = l/(k*A) in ºK/W	Power (W)	Temperature step (ºC)
GeAu die back metalisation	1.50E-06	1.5	88	6.37E-08	63720.0	0.2665	0.125	0.03
AuSn 80/20 Eutectic (10% voids)	3.00E-05	2.5	272	6.37E-08	63720.0	1.7338	0.125	0.22
QFP28 package base. Top Au plate	1.50E-06	1.5	297	8.00E-06	8.0	0.0006	1.5	0.00
QFP28 package base. Top Ni underplate	5.00E-06	5.0	92	8.00E-06	8.0	0.0068	1.5	0.01
QFP28 package base. Cu/W 15/85	2.54E-04	254.0	209	8.00E-06	8.0	0.1519	1.5	0.23
QFP28 package base. Bottom Ni underplate	5.00E-06	5.0	92	8.00E-06	8.0	0.0068	1.5	0.01
QFP28 package base. Bottom Au plate	1.50E-06	1.5	297	8.00E-06	8.0	0.0006	1.5	0.00
Conductive package bonding paste (ABLEFILM 5025E; Silver filled)	1.52E-04	152.4	4	8.00E-06	8.0	5.4429	1.5	8.16
Total Mounting thermal step								8.66

Figure 5.72: Thermal characteristic of the assembly components.

Discounting the mounting thermal step and considering the single transistor case, the maximum hybrid acceptance temperature is 80ºC.

Heat sinks should be designed in order to ensure that these conditions are verified. Special care has to be taken when using the transistor in extended drive as the temperature rise is higher reaching ΔT values of more than 45ºC in the worst case.

5.5.6.2.6 Even and Odd mode Stability analysis

It is well known that in a multi-stage amplifier especially when multiple parallel transistors are used several oscillation modes can occur. The multistage topology makes amplifier very prone to parametric oscillations due to the presence of multiple non-linear elements and feedback loops. In addition, if with n parallel transistor, n possible oscillation modes exist. The even mode is when all the transistors are oscillating in-phase (a condition similar to what happens in oscillators and the condition which is identified by conventional stability analysis), but the other n-1 modes are odd-oscillating modes originated by the possibility of internal loops in which different transistors are oscillating in phase opposition.

In this cases the K factor [5.13] analysis (or the equivalents Mu and Mu` analysis, [5.14]) is only capable of determining if the circuit has an even mode oscillation. The following considerations are based on the work developed by [5.17] which makes use of the STAN (Stability Analysis, [5.18]) tools for the Scilab simulation Environment [5.19].

The method has been successfully used to individuate and prevent even and odd mode and parametric oscillation in S [5.20], X and Ku [5.21] band power amplifiers. It is based on the analysis of a transfer function of the circuit (evaluated in different points properly selected) to individuate the possible presence of complex poles with positive real part. This method is, in theory, capable of revealing any possible cause of instability. Without entering in detail (refer to [5.17]-[5.19] for an in-depth explanation), the results of the analysis applied to the worst case stability conditions (operating temperature of -30º and the worst parameter dispersion) will be presented.

The stability analysis consists of a two step process:

1. Obtaining a frequency response in a given bandwidth (i.e. admittance of a node), corresponding to the circuit linearization about its steady-state (either DC or large signal);
2. Applying STAN to this frequency response to obtain the corresponding factorized transfer function to identify the poles- zeroes plots

Firstly, the circuit was checked for a stable DC operating point obtaining the transfer function for all the frequencies at which the circuit is capable of producing an oscillation (hence up to f_{max}=60GHz for the selected technology). In this case no input signal, but only supply voltages are applied.

The transfer function obtained with STAN and the proposed methodology has been evaluated in several points of the circuit (generally as close as possible to any non-linear source, i.e. gate and drains of FETs, and at least for a couple of transistors per stage) and the presence of poles with a positive real part (condition required for the presence of oscillation) was never observed, implying that the circuit has a stable DC operating point. As an example, in Figure 5.73, magnitudes and phase of the amplifier transfer function (calculated between the second and the output stage) are compared with the extrapolated and perfectly fitted (x) transfer function.

As can be noted in the correspondent pole-zero map (Figure 5.74) there is no pole with a positive real part.

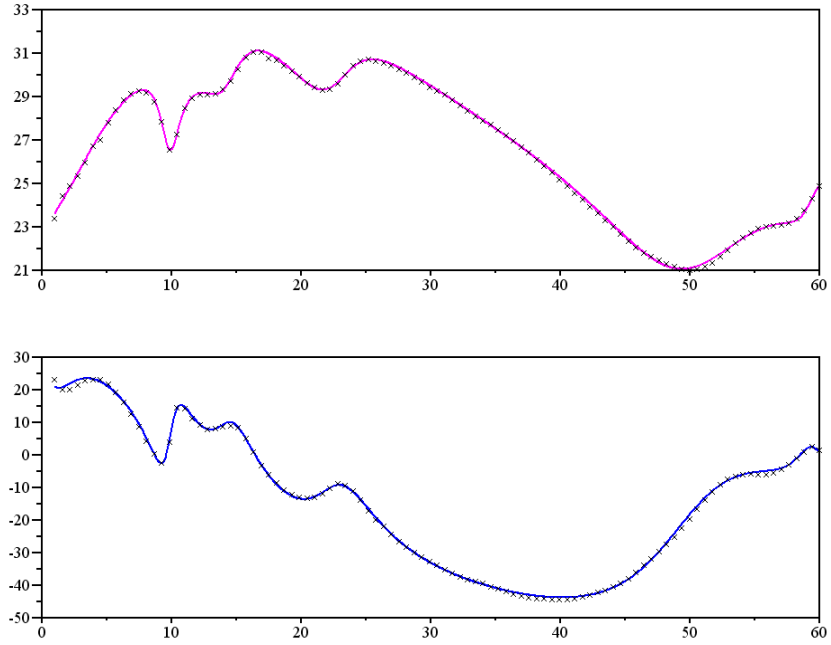


Figure 5.73: Magnitude (up) and Phase (down) of the amplifier transfer function between 0 and 60GHz, compared with the extrapolated one (x)

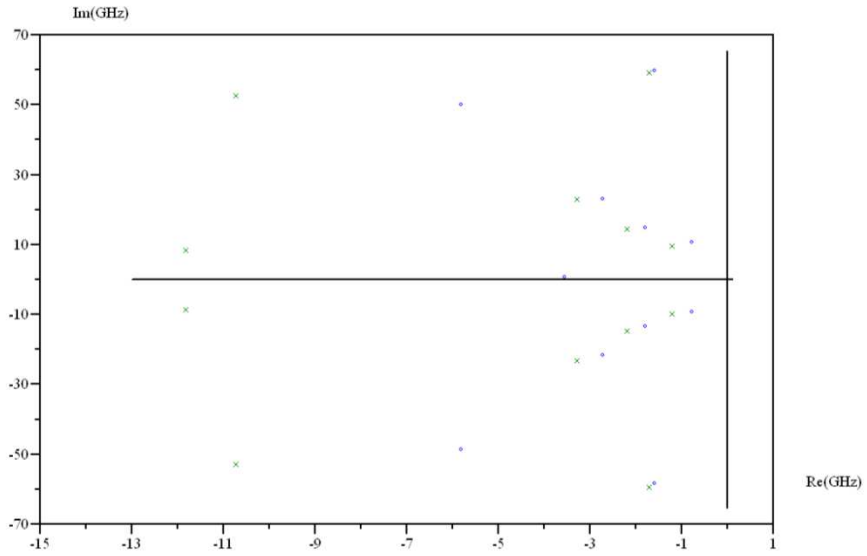


Figure 5.74: Pole-zero map of the frequency response showed in Figure 5.73

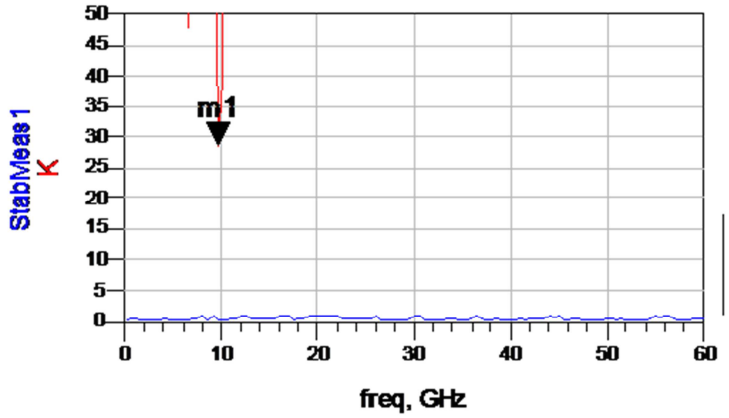


Figure 5.75: Figure 74. Rollet Stability factor (K) and Stability Measure of the amplifier.

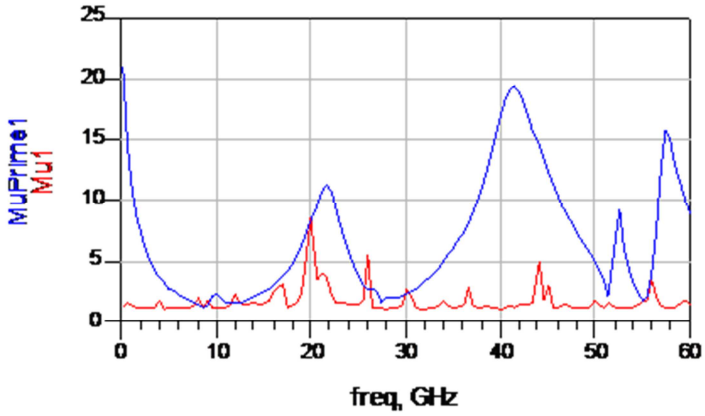


Figure 5.76: Figure 75. Mu and Mu' of the amplifier.

These results, jointly with the Fact that the stability factors Mu and Mu` are greater than 1 from 0 to 60 GHz (or equivalently k>1 and the Stability Measure greater than 0), ensure that the circuit has a stable DC operating point with any output load. In the following graphs the stability parameters for the MMIC amplifier are showed, confirming the amplifier unconditional stability with a sufficient margin even in the worst case.

Once verified the stable DC behavior of the amplifier it is necessary to check the behavior under real operating conditions (i.e. large signal pumping). The response has been characterized with input signals between 1.5GHz to 2.5GHz, and an input power varying from -40 to 0dBm (for higher values the simulator showed convergence problems). Moreover simulations with higher input frequencies were run to check for potential parametric divisions (which have been observed for this type of circuits). In all the cases the frequency considered in the analyses span the entire 0-60GHz range.

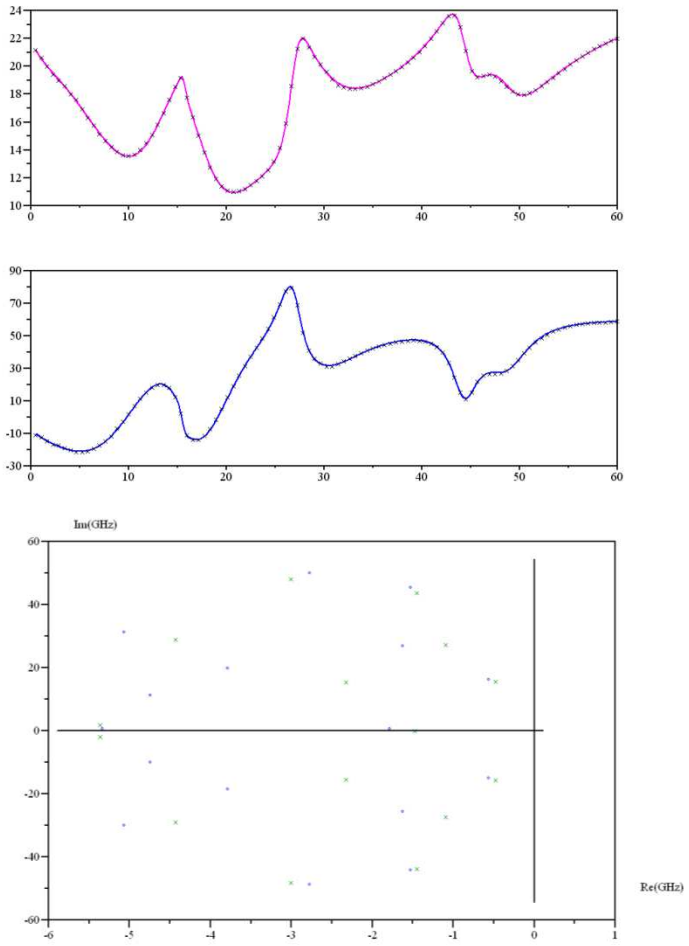


Figure 5.77: Figure 76. Amplifier transfer function (magnitude and phase) evaluated in the gate of one of the transistors of the inter-stage amplifier, and relative pole-zero plot

All the critical points of the circuit were considered to evaluate the corresponding transfer functions, and in none of the simulations the presence of poles with a positive real part was observed. Moreover, in all the cases the poles showed a safe stability margin, being the maximum value observed for the real part of the poles in the order of -0.3. A complete simulation report of these tests is out of the scope of this document, so as an example of the obtained results, only one of the computed frequency response with its relative pole-zero plot is showed in Figure 5.77.

All the results confirm the absence of any type of oscillation in the designed amplifier.

5.5.6.3 IMPLEMENTATION AND MEASUREMENTS

The designed amplified has been mounted inside the selected 24-pin QFN package (Figure 5.78). DC bypass dielectric parallel plate capacitors (http://www.knowlescapacitors.com/dilabs/en/gn/products/single-layer-capacitors) have been mounted close to the supply pads inside the package before connecting to package leads in order to minimize the risks of signal leakage in the supply lines.

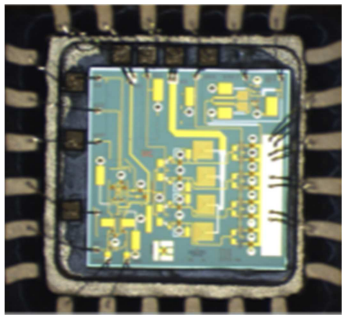


Figure 5.78: Packaged MPA

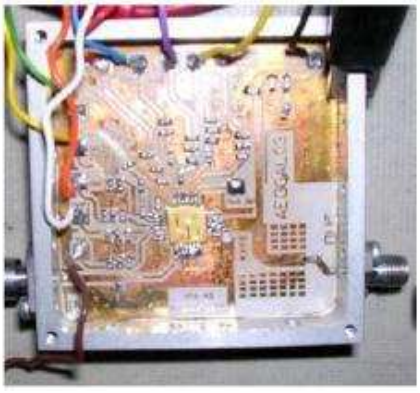
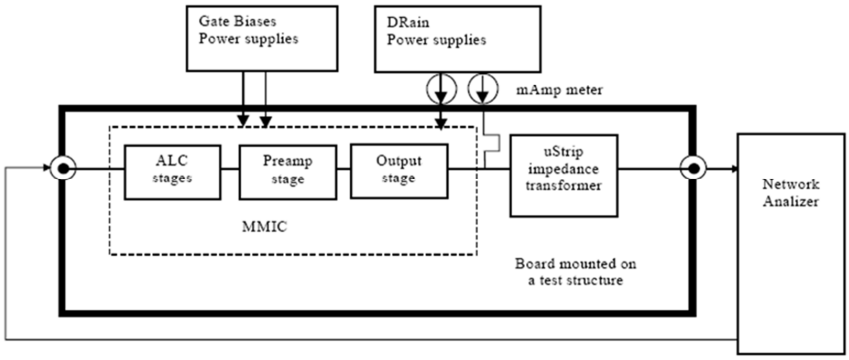


Figure 5.79: Photo of the test board assembled inside the metallic box.

In order to measure the MMIC, a board based on microstrip technology was designed. The selected substrate used was Duroid 6002 (https://www.rogerscorp.com/documents/609/acm/RT-duroid-6002-laminate-data-sheet.pdf). The test board has a microstrip line to connect the input, and an output microstrip matching network to match the low optimal load impedance to the 50 Ohm load which the network analyzer has. The board was housed inside a metallic box with input/output 50Ω coaxial connectors for testing purposes.

The MMIC package was glued with a conducting epoxy directly to the metallic structure in order to obtain a better heat dissipation and optimal RF ground contact to minimize the parasitic inductance which could cause high frequency oscillations.

The test set-up for s-parameter measurements is shown in Figure 5.80.



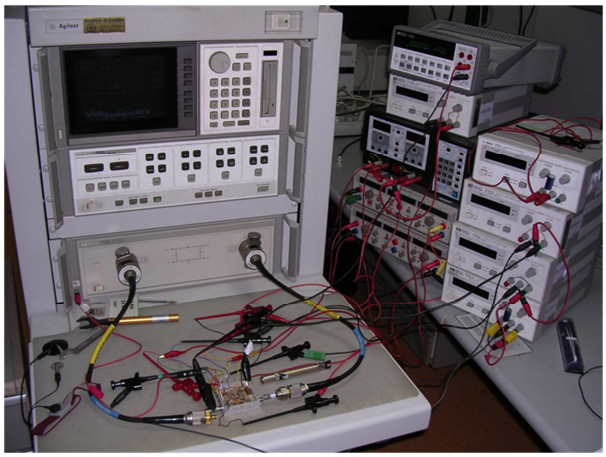


Figure 5.80: S-parameters measurements set-up

The VGA has two possible working modes. In the normal mode its P1dB is about 19dBm while in the extended mode it's possible to obtain up to 25dBm. The difference between the two operating modes is the biasing point. The measurements have been carried out with "nominal bias" condition (i.e. adjusting the gate control voltage so that

each of the sub-circuit in the amplifier consumes the same current as per the simulated value). The following figures summarize some of the measurement results.

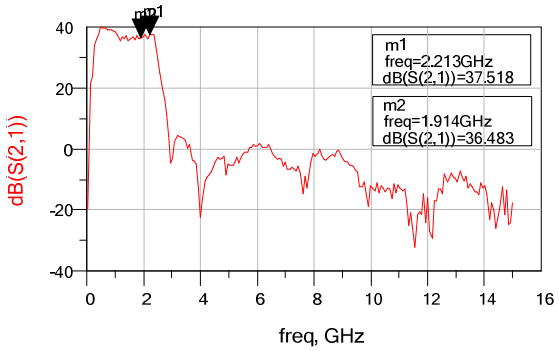


Figure 5.81: Maximum gain for the extended drive bias.

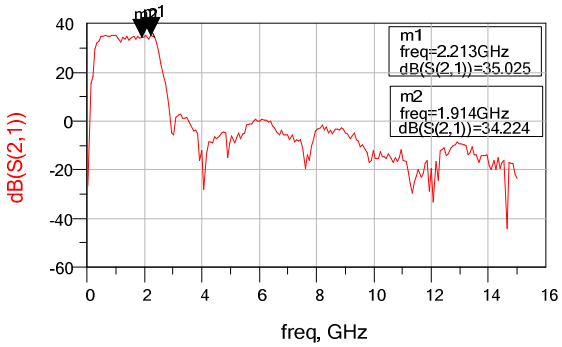


Figure 5.82: Maximum gain for the normal drive bias.

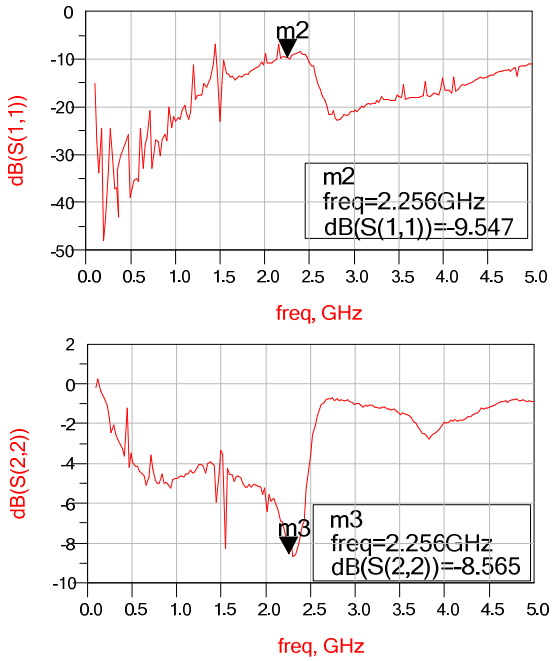


Figure 5.83: Input and Output match for the extended drive bias at maximum gain

As can be observed in Figure 5.81-Figure 5.83, the shape of the frequency response is quite close to the simulated results. Minor divergences (around 3dB lowering) are

observed in the absolute gain values in both cases. This can be partly associated to assembly losses (input/output lines, RF connectors and transition) and partly to the inaccuracies of the modeling (matching network, amplifier and packages), but in any case the performance are kept well above the requirements.

The S11 and S22 parameters are extracted for several control voltages, but as the match is basically related to the output microstrip transformer on the PCB, the results are almost constant varying the control voltage. Input match results are worst with respect to the simulations due to an error in the PCB as the input line width has been erroneously sized with respect to the package lead. The multiple peaks in the measured s-parameter response are associated to the poor calibration performance. In fact, to safely carry out the measurements with the network analyzer (which tolerates a maximum of 15dBm of input power), the calibration has to be performed with very low input power (<-30dBm), with consequences on quality of the calibration itself.

The gain dynamic range has been evaluated varying the control voltage from 0.6V to 1.55V (higher than the simulated values). Results for the normal drive condition are shown in Figure 5.84 with good agreement with the simulations. The three markers are relative to Vg1=0.6V (m_HIGH), 1.4V (m_MID) and 1.55V (m_LOW). Figure 5.85 gives a detail of the gain flatness of the amplifier response over a 200MHz bandwidth.

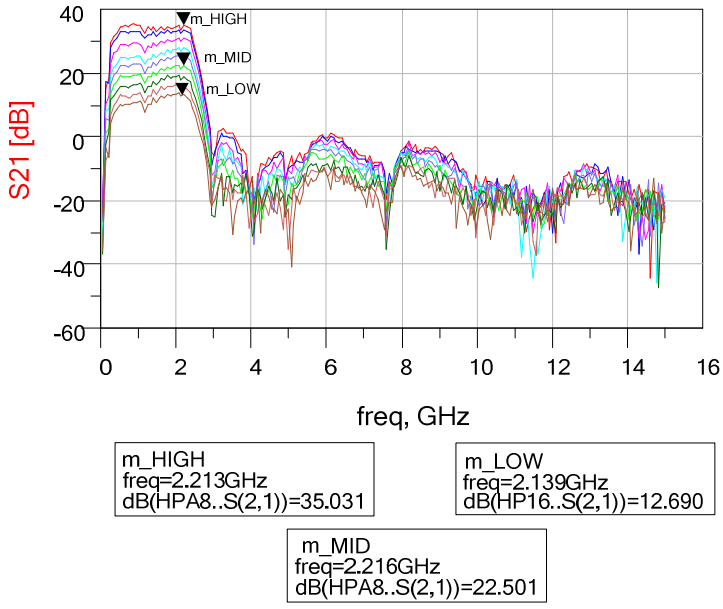


Figure 5.84: Amplifier frequency response for different gain values.(Normal drive).

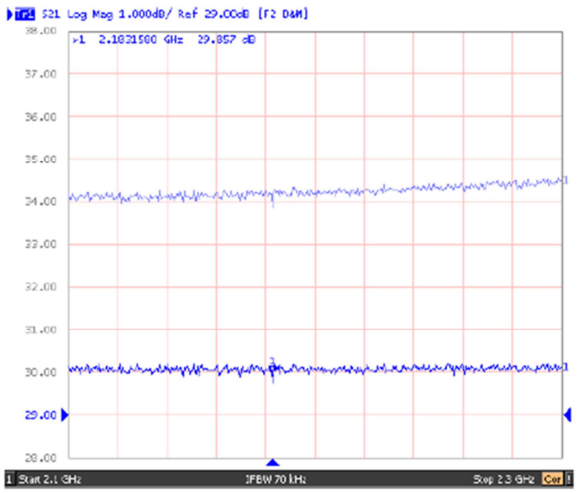


Figure 5.85: Gain flatness in 200MHz bandwidth for two gain values

Extensive power measurements were also carried out on the packaged amplifier for both configurations and different control voltages. Part of the results (the ones provided by TAS-E, who carried out the test on the final device) are shown in the following figures.

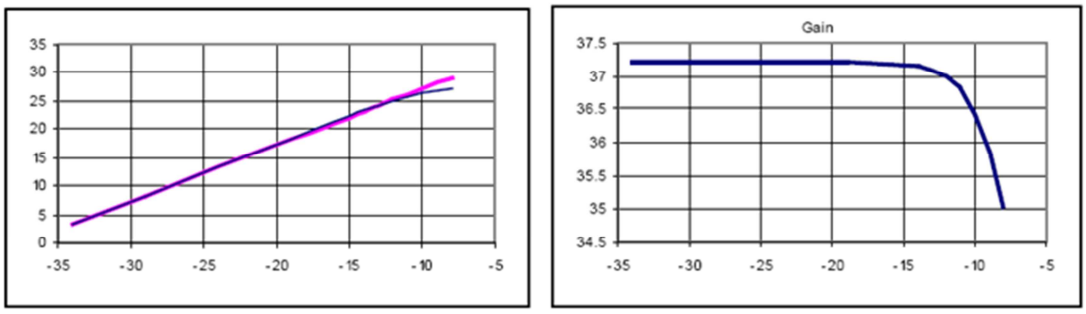


Figure 5.86: Power and gain curves at maximum gain (Vg1=0.6V) and extended drive configuration. P1dB≈25.4dB

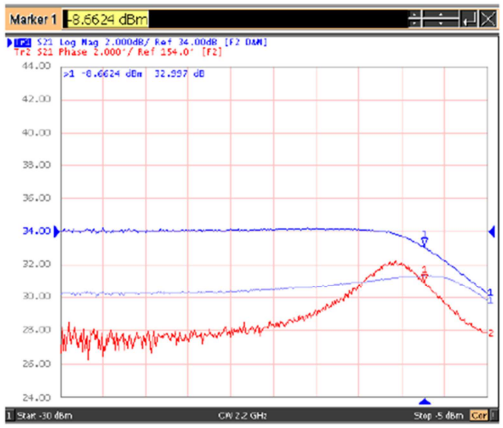


Figure 5.87: Power gain curves (30 and 34dB) and 1dB compression point (≈25dBm) for the extended drive (also shown in red the phase variation for 34dB gain configuration)

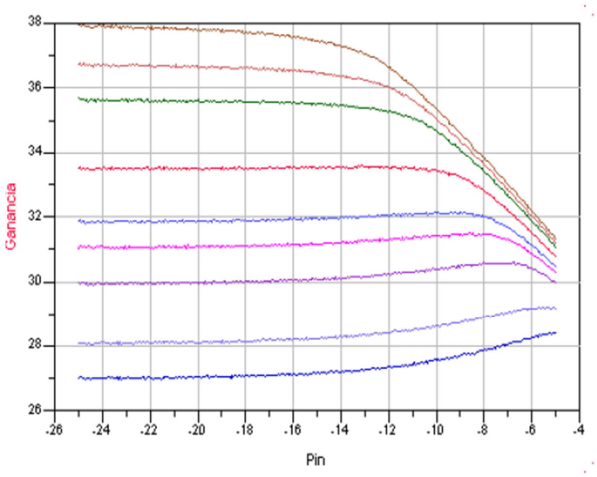


Figure 5.88: Power saturation curves and 1 dB compression point for the VGA in extended drive configuration at different control voltages. (P1dB is between 24.5 and 26dBm)

5.5.6.4 THERMAL ANALYSIS

As the amplifier´s output stages are operating at high current level and the selected technology, hence a detailed thermal characterization, following the preliminary analysis described in section5.5.6.2.5, was carried out in order to check the safe operating condition.

To carry out a detailed characterization of the VGA MMIC thermal behavior, the MPA die was attached directly to the heatsink and wire bonded to the PCB. Both the Die and the PCB were glued using conductive epoxy.

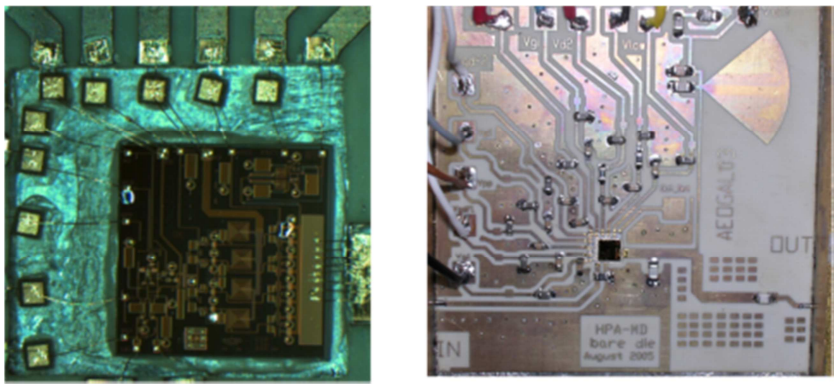
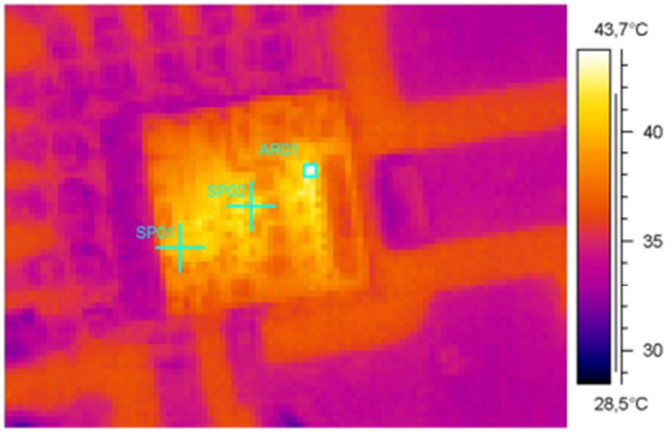


Figure 5.89: Assembly of the bare die on the test PCB used for the thermal analysis

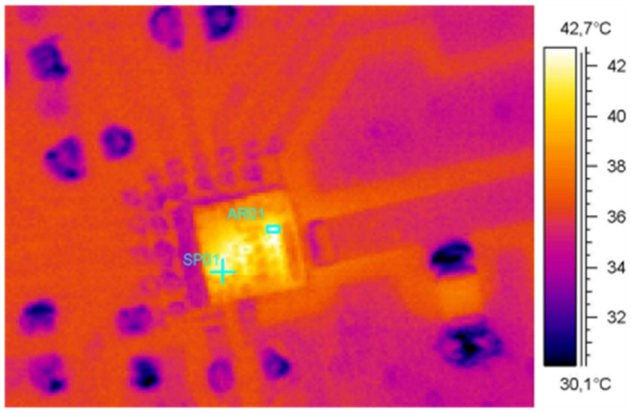
The thermal behavior was firstly checked with an infrared camera in different operating conditions (DC quiescent point, linear region, under large signal pumping, and saturation).

Examples of measurements are illustrated in Figure 5.90 (linear region) and Figure 5.91 (saturated amplifier). The hottest spot in the measures is localized over the transistors of the output stage as was to be expected. The observed temperature gradient between the hottest and coldest points in the surroundings gives an increase of less than 12 ºC.



Label	Value
IR : max	44,5°C
IR : min	28,7°C
SP01	40,6°C
SP02	41,6°C
AR01 : max	44,5°C

Figure 5.90: Infrared response of the MMIC MPA Fin=-2.25GHzm, Extended drive, Max. Gain, Pout=8dBm)



Label	Value
IR : max	44,6°C
IR : min	29,3°C
SP01	41,3°C
AR01 : max	44,6°C

Figure 5.91: Infrared response of the MMIC MPA (Fin=2.25GHz, Extended drive, Max. Gain, Pout=27.5dBm)

The infrared photo inspection presented however insufficient resolution to reach the transistor fingers for a detailed estimation of channel junction temperature by the drain metallization, which is the critical parameter to be monitored to ensure a safe operation to meet the spatial de-ratings. The available resolution does resolve the transistor area, and since the drain and source metal fingers can be considered at a nearly homogeneous temperature, it is an indication of the transistor temperature.

To improve the analysis a different technique (gate forward voltage test) was used to cross check the results of the infrared estimations and give an estimation of the effective temperature increase inside the transistor junction.

A transistor can be seen as equivalent to a device made up of two p-n junctions. Each p-n junction response can be separately measured and characterized by properly biasing the transistor (Figure 5.92). Measuring the I-V response for the transistor junction, we will be able to obtain a curve similar to a diode curve.

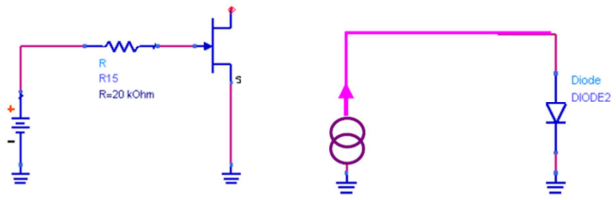


Figure 5.92: Transistor junction biasing and diode based equivalent model.

It's well known that the intrinsic potential of the p-n junction changes with temperature, so if the p-n I-V curve is measured for different temperatures, the V = f (I, T) relationship can be obtained. It is then possible to extract information on how much the forward junction voltage will change with temperature from the V-T slope at constant current. It is worth noting that it is necessary to make the junction work in forward mode in order to measure the intrinsic potential of the junction and its variation with temperature.

Now, if the pHEMT transistor is biased to work in nominal conditions, it will begin to dissipate power and will reach a final working temperature above the initial transistor rest temperature. The value to be extracted is this temperature increment.

Biasing the transistor and monitoring V_{GS}, it will be possible to measure how it changes when the transistor increases its temperature due to the power dissipation. The

temperature increase of the junction can, then, be extracted by comparing the measure with the V-T curves.

The main problem is associated to the fact that, with the gate forward biased, the transistor behaves as a very low Ohmic resistance at the drain port, being difficult to make it dissipate power, which, in turn is the target stimulus. To dissipate power the pHEMT transistor should be working in its nominal mode, with the gate-source junction inversely biased and, as a consequence, useful V_{GS} cannot be measured while the transistor is dissipating power. This problem can be solved switching between the biasing point where the transistor is dissipating power and another point where the gate-source junction is forward biased and measuring its potential while the transistor is still hot . Because the pHEMT transistor can switch its electrical response quicker than its thermal response, the obtained measure can give a very representative value of the transistor temperature.

A simple circuit has been developed to carry out the pHEMT transistor biasing, switching and V_{GS} measure. This circuit and the signal scheme are shown in Figure 5.93.

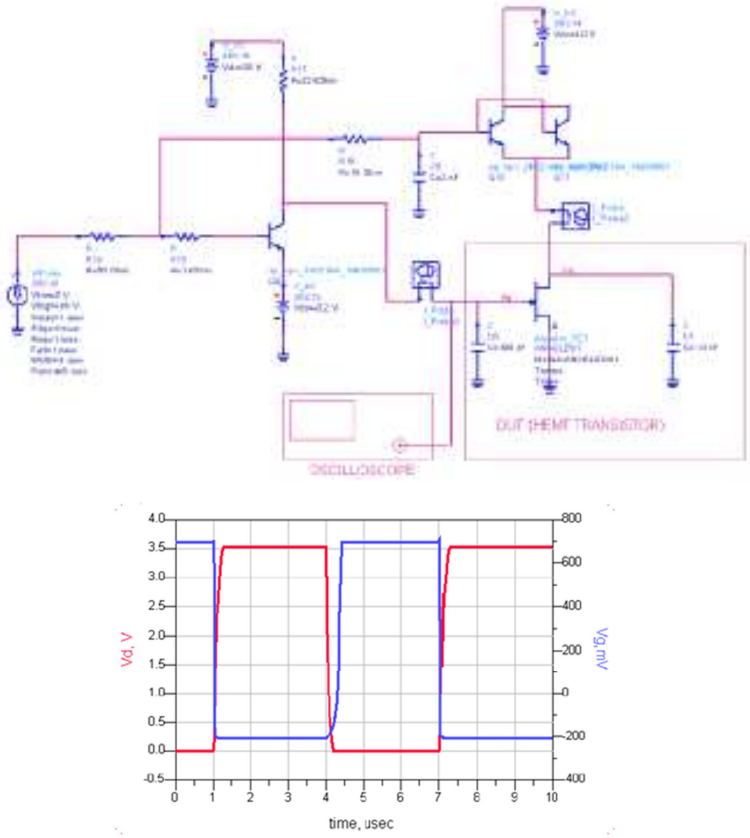


Figure 5.93: Test Circuit (left) and generated biasing signals used to characterize the pHEMT transistor.

According to this measurement procedure, some results were obtained when applied to the last stage of the MMIC built up of eight parallel transistors representing the hottest point inside the MMIC as confirmed also by the thermal imaging analysis.

Because the current design does not allow separating each transistor gate in order to measure it independently, so a unique measure for all the eight transistors was carried out.

Firstly, the I-V curves for different temperatures of the last stage forward biasing the date-source junction (with V_d left open) where obtained. The results are shown in Figure 5.94. With these values, a V-T slope of 1mV/ºC can be obtained (Figure 5.95).

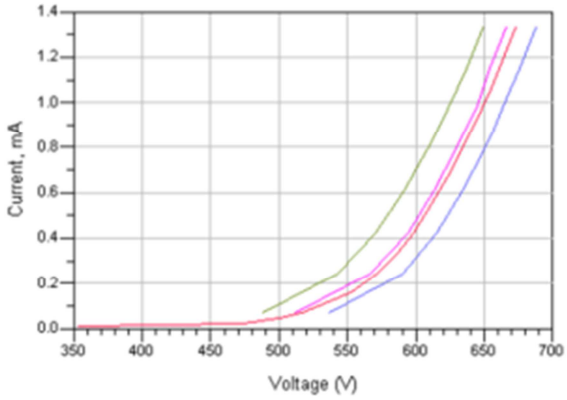


Figure 5.94: I-V measured response (last stage MPA transistors) for different temperatures.

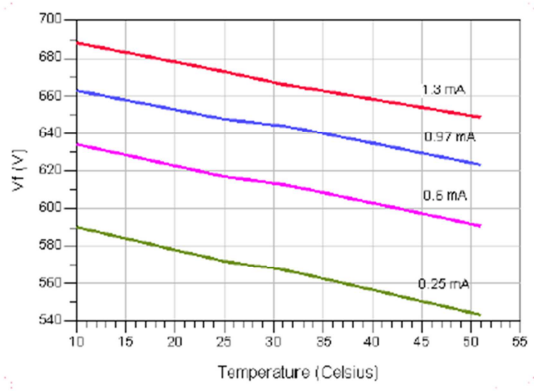


Figure 5.95: Forward voltage variation with Temperature.

Then, the circuit in Figure 5.93 was used to test the last stage of the MMIC while the other stages where not biased. By using an oscilloscope, the V_{GS} signal was monitored while applying a pulsed signal to switch between the two biasing states. Measurement results are shown in the following figures.

In Figure 5.96 and Figure 5.97 the gray curve represents the V_{GS} measure when the amplifier stage is turned off. The initial curve is due to the response of the circuit used

to bias the transistors and its shape is related to the time constant necessary to raise the square pulsed control signal, so only when the curve gets a constant value, can be considered as valid.

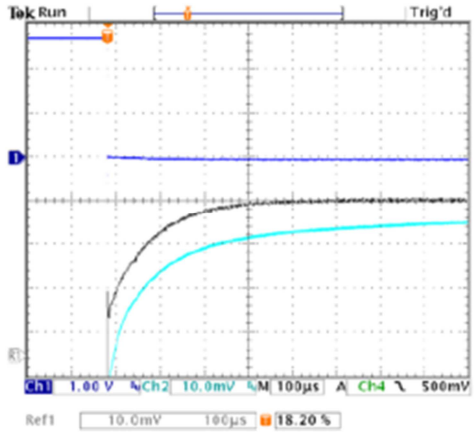


Figure 5.96: Measured response (cyan) for a power consumption of 900mW. Gap between HEMT turned on and off is about 12 mV (temperature increase of 12ºC).

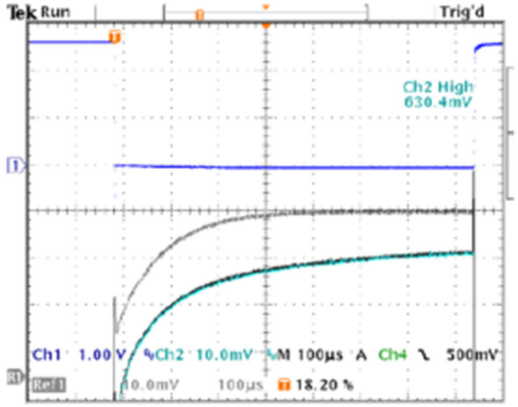


Figure 5.97: Measured response (green) for a power consumption of 1300mW. Gap between HEMT turned on and off is about 15 mV (temperature increase of 15ºC).

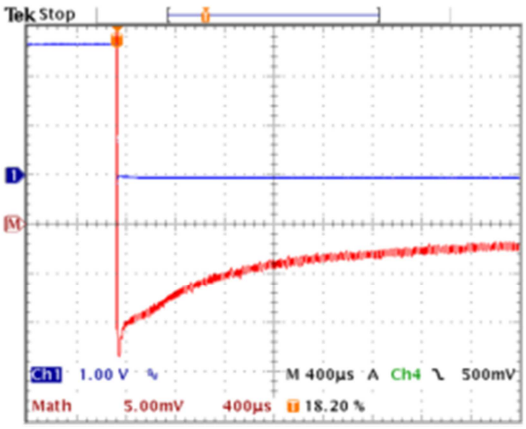


Figure 5.98: Measured response for a power consumption of 900mW. The red curve shows the temperature evolution with time to verify the thermal time constants

The cyan and green curves are the responses when the transistor is turned on. As they are also affected by the response of the bias circuit, only the subtraction with the initial curve gives the desired V_{GS} measure. This subtraction is presented in Figure 5.98 (red curve) and it also shows how the transistors cool with time. The thermal response with time is much slower than the electric response of the pulses, so the measure is representative of the temperature in the transistors.

The obtained results give an estimation of the temperature increase inside the transistors of the last amplification stage in the MMIC. These measures are also quite in line with that obtained with an infrared camera and the simulation results, hence confirming the usability of the circuit for the targeted application.

For sake of completeness a summary of the measured results is reported in the following table.

Table 5.18: Summary of the MPA VGA measured performances

Símb.	Caracteristics	Test Resuklt			Units.	Conditions
		Mín.	Typ.	Max		
V_{cc}	Power Supply		3.5		V	Tolerance ± 3%
Pd	Power consumption			1.6	W	
F_{center}	Operating Frequency	1.9	2.25	2.4	GHz	10MHz signal Bandwidth
S11	Input match			-9	dB	at any Gain, 50Ω source with broadband matching network
G_{PMAX}	Maximum Power Gain			37	dB	V_{ALC}= Max gain, extended drive
G_{PMAX}	Minimum Power Gain	12			dB	V_{ALC}= Min gain, normal drive
GCR	VGA Dynamic Range	12		>20	dB	V_{AGC}=Full
G_{FLAT}	Gain Flatness			0.15	dB	in the signal Bandwidth
G_{SLOPE}	Gain Slope			0.01	dB/MHz	in the signal Bandwidth
NF	Noise Figure			<15	dB	@MAX Gain
P_{1dB}	Normal drive configuration Output Power at 1 dB gain compression	19			dBm	@ MAX Gain and nominal load
P_{1dB}	Normal drive configuration Output Power at 1 dB gain compression	24.5			dBm	at MAX Gain and nominal load
P_{SAT}	Saturated Output Power			27	dBm	at MAX Gain and Extended drive
Smx	Maximum input level			5	dBm	Tested

5.6 SYSTEM INTEGRATION AND PERFORMANCE

The designed circuits have been integrated by TAS-E (either with MCM or single chip packages) with the base band chips so as to build the new compact S-band TT&C transponder to be tested in different operation modes.. A dramatic size and weight reduction has been achieved in comparison with the previous generation. This can be better understood observing Figure 5.99 and Figure 5.100, which compare the photographs of the previous and the first generation of new TT&C transponder respectively. The new transponder measures only 190x162x119 mm with the same transverse dimension (D=190mm) but with a weight of only 2.5 Kg, which represents a reduction of around 40% compared with the previous generations of TT&C transponders. These characteristics help to reduce the total cost of the missions. For example, with the proposed Integrated S-band Transponder the satellites can be launched by groups, keeping an affordable cost for the missions requiring large number of satellites to provide global Earth coverage.

Figure 5.99: Old generation of S-Band TT&C transponders

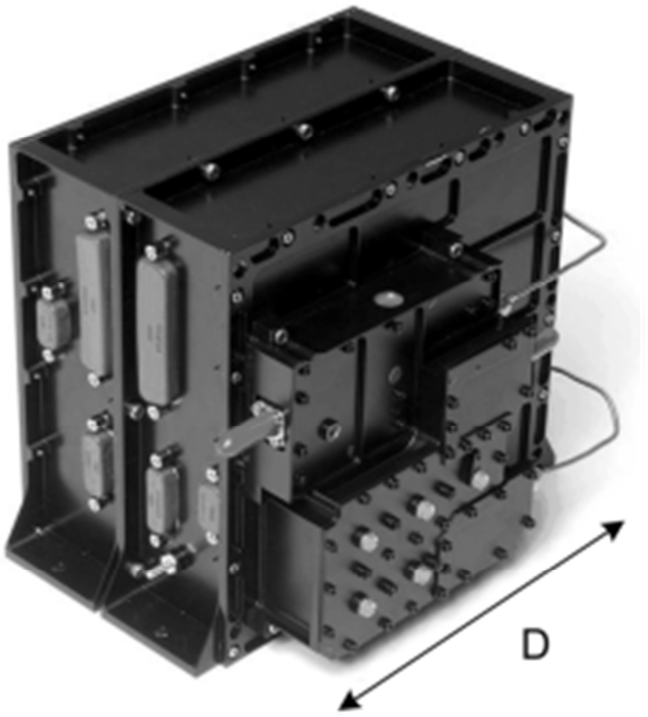


Figure 5.100: Engineering7structural module(matched to different mission requirements) of the new Integrated S-Band TT&C transponder using the developed set of MMICs.

The developed RF equipment performs optimally even in demanding conditions, while allowing flexibility and adaptability for different specifications depending on the mission. Hereafter are summarized some of the measured performance (at ambient temperature) of the entire transponder which have been provided by TAS-E.

Phase noise requirements depend on the TT&C operation mode. In coherent mode, especially close to the receiver acquisition threshold (C/N_0=30dBHz…40dBHz), the uplink thermal noise is dominant owing to the fact that the close-in noise is tracked by the receiver and then turnaround in the downlink as it is needed to be scaled in frequency but coherent in phase. In this case, typical phase noise requirements are 3ºrms integrated between 10Hz and 1MHz. In Figure 5.101 the VCO performance after the x3 multiplier with the loop cut at 30 kHz, is -105dBc/Hz at 100 kHz resulting in less than 2º rms integrated phase noise.

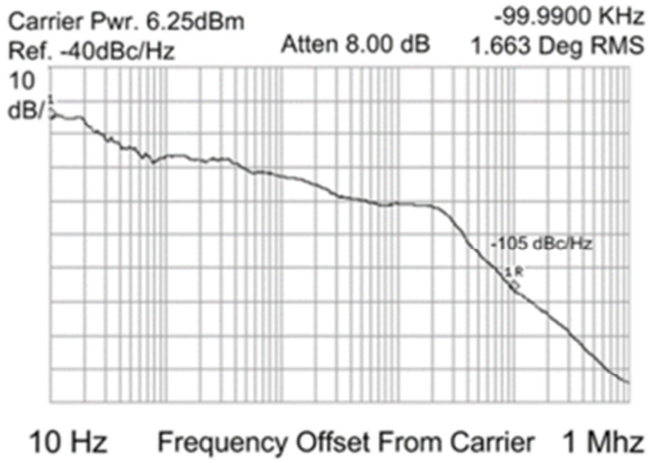


Figure 5.101: Measured Phase Noise performance of the Oscillator and Multiplier in coherent mode

When the signal is strong or when the downlink is asynchronous with respect to the uplink, the VCO and the synthesizer are typically the main contributors to phase noise and 1ºrms is required. In this case, the required performance is achieved with larger cut-off frequencies (~50Khz) as per the larger GaAs flicker corner frequency.

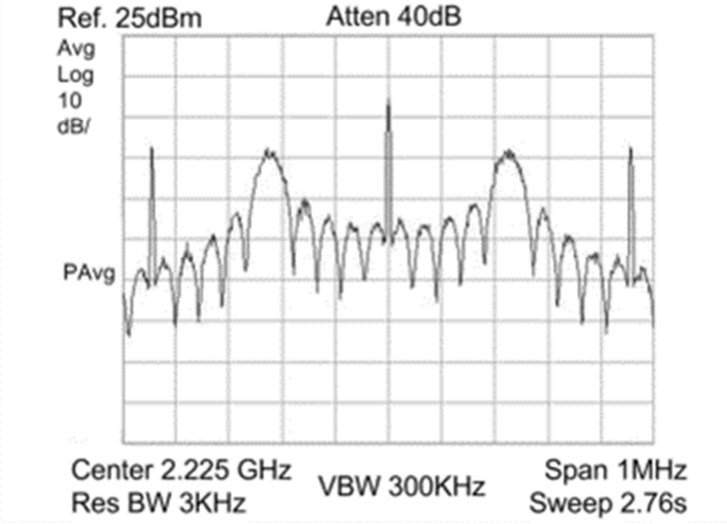


Figure 5.102: Transmitted Sub-carrier PM Modulation generated by the TX Chain.

Examples of different modulation formats that can be generated by the same hardware configuration (TX_GEN board in Figure 5.1) and measured after the MPA VGA are shown in Figure 5.102 and Figure 5.103. In the first case a low data rate standard TT&C PM modulation of a BPSK signal with PRB sequence as transmitted data is shown, while in the second demonstrates the generation capability of more

advanced GMSK modulation signals better suited for high data rates and increased spectral efficiency.

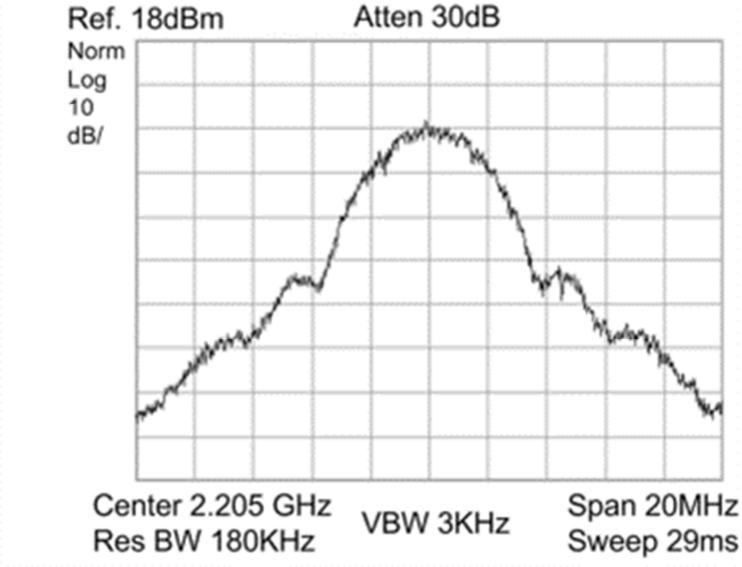


Figure 5.103: Transmitted GMSK Modulation generated by the TX. chain

An essential parameter for the transponder performance is the group delay stability of the whole system, as this impacts the turnaround delay measurement ability. As can be observed in Figure 5.104, although the signal dynamic to be compensated by the VGA IF chain is large (from –130dBm to –60dBm), the group delay variation due to VGA changes remains in the sub-nanosecond area. In this manner, satellite tracking is much more precise than with the previous generation, where the delay variation was ten times greater ($\tau \approx 30$ns).

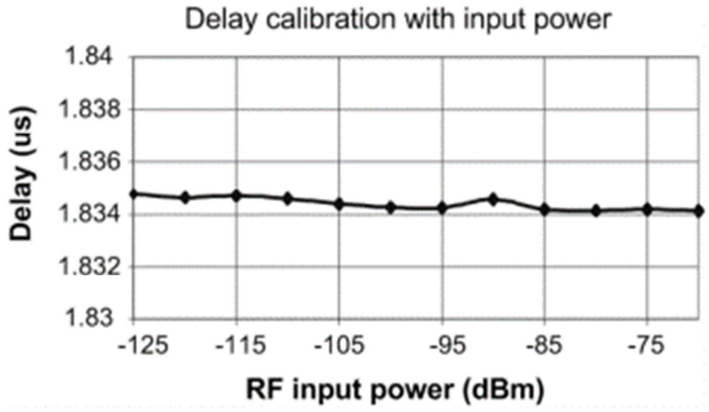


Figure 5.104: Group delay of the IF part of the ISBT transponder

5.7 CONCLUSIONS

The development of Multi-Chip Multifunction Modules and high performance MMIC, taking advantage of MMIC technology and advanced packaging techniques, has allowed the implementation of the RF part of a new Integrated S-band Transponder originally designed for the GALILEO mission ([5.22]) but suitable for many kind of mission scenarios.

The size and weight characteristics along with the compactness, flexibility and adaptability of the MMIC and modules have allowed a significant improvement of the transponder performance, allowing the configurability of the full system .

The resulting chip-set is currently in use in the new generation of telecommunications satellite equipments commercialized by TAS-E (ANNEX I)
The new generation of Integrated S Band Transponders (ISBT) developed by Thales Alenia Space España is now a reality with more than 60 units sold worldwide. At present CRYOSAT 2 and GALILEO IOV are in orbit and additional missions like SAC-D, SWARM and SAOCOM rely on the ISBT technology.

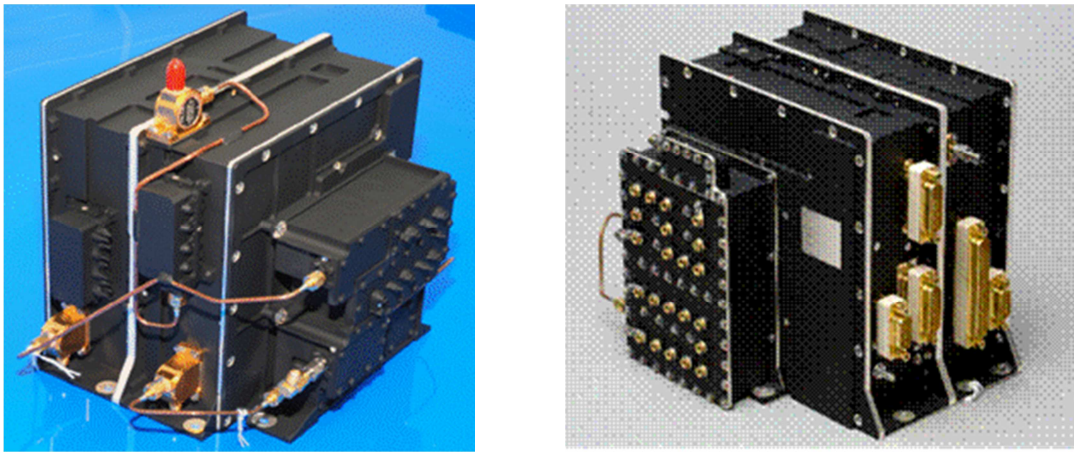


Figure 5.105: Flight Modules for the Cryosat 2 (left) and Galileo IOV (right) space missions

Moreover, within the framework of the GMES (Global Monitoring for Environment and Security) program of the European Union and ESA, for the SENTINEL satellites, TAS-E is continuing to improve ISBT with enhanced technical characteristics already tested by ESA with excellent results [5.23].

5.8 REFERENCES

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6 . Large Signal Three-port stability analysis: application to a mm-wave Mixer

6.1 INTRODUCTION

This chapter presents a methodology to determine stability in non linear three-port circuits based on a generalization of the three-port μ-stability factor applied to linearized S parameters under large-signal pumping.

A comparison with an extension of the Conversion Matrix-based, System Pole-Zero Identification used to analyze circuit stability is also presented. The relationship between the two techniques has been verified by means of an ideal two-port non linear circuit, and then applied to the design of a three-port mm-wave GaAs MMIC up-converter. By applying the proposed methodology the appearance of spurious oscillations was prevented ensuring proper functionality of the circuit.

The circuit was fabricated with the OMMIC GaAs foundry process used for the implementation of the circuits described in the previous sections. On-wafer measurements showed an average conversion loss about 3.5 dB at a RF bandwidth between 40.4 and 41.5 GHz with LO frequency fixed to 42.5 GHz. A RF/LO isolation better than 25 dB was measured in the whole band, showing also outstanding inter-modulation performance.

Section 2 gives an overview of different stability analysis techniques while in section 3 amplifier and mixer regimes are compared in terms of formulation and solutions stability. In section 4 the three-port linear stability theory is briefly described and then, extended to non linear circuits under large-signal pumping. In section 5, the interrelation among μ stability factor, negative resistance and Conversion Matrix based pole-zero identification under large-signal pumping is discussed and illustrated with a

simple non-linear two-port circuit with fixed poles and zeros, verifying the utility and the limitations of all the methods. Finally the design of a GaAs HEMT MMIC up-converter is presented in section 6 showing how the methods are applied to avoid spurious oscillations. In section 7 the performance of the fabricated prototype is summarized, confirming the absence of spurious oscillations. It´s worth noting that the design of the MMIC itself was not the main goal of the present work; the circuit was used to validate with a concrete example the stability check procedures. Nevertheless details of the designs and measured results have been presented for sake of completeness.

6.2 STABILITY FACTORS CONSIDERATIONS

The technique which will be presented in this chapter represents an extension of the three-port linear stability factor ([6.1], [6.2]), to non-linear circuits under large-signal regime. In two-port linear circuits, a third port may be introduced to take into account the effects of biasing on the stability performance and analyzed through the three-port μ stability factor [6.3]. In the design of non-linear circuits operating under large-signal stimuli, the power level of operation should be taken additionally into account in the stability analysis of the circuit.

Although it is virtually impossible to define a general procedure to guarantee the global stability of a complex circuit with many active devices (for all possible loads, frequencies, bias points, small/large signal, DC/periodic/quasi-periodic regimes, etc.) different techniques have been proposed, evolving with the complexity of circuits and the capabilities of CAD tools. Rollet stability factor [K, 6.5] (with the limitations discussed in [6.6] and [6.7]) and the more recently introduced μ stability factor [6.8] are extensively used to analyze and prevent instabilities or spurious oscillations in two-port linear circuits.

The μ factor is a geometric parameter which represents the distance from the centre of the Smith chart to the nearest load impedance which causes an input reflection coefficient equal to 1. For μ values greater than 1 no passive load will cause the two-port circuit to oscillate (unconditional stability), under the condition that that the two-port input is intrinsically stable (i.e. with no load). If μ is lower than 1, stability circles

are used to identify stability regions to avoid unstable loads (conditional stability). In two-port linear circuits, Nyquist criteria applied to S parameters [6.9] or through the insertion of a virtual ideal circulator [6.10] also prove to be useful to evaluate a circuit´s stability.

In the case of a three port circuit, a simplified approach to study stability is the loading of one of the ports with fixed impedance, and then applying linear stability factors analysis to the other two ports. This approach however is not practical for non-linear circuits as it would not take into account for example, the effect of LO pumping or the RF/IF input power level in a three-port mixer. In these cases, not only the stability of the DC point, but also the stability of a periodic or quasi-periodic regime should be verified, therefore non linear techniques are required. Return-Ratio Matrix formulation [6.11] has been proposed to unify linear and non linear analysis.. Examples of other techniques that are used in practice to search for oscillations are based on the use of the Normalized Determinant Function [6.12], an admittance probe [6.13], the use of a Conversion Matrix analysis [6.14], or through the transfer function of the linearized circuit with a single input and a single output (SISO), as a closed loop feedback system, by directly identifying its poles and zeros ([6.15] ,[6.16]). All these methods are especially well suited when searching for parametric oscillations which can appear, for example, in power amplifiers varying the input power level.

The aim of the work carried out was to identify an alternative method for stability analysis of 3 port non-linear circuit which could be easily implemented in any circuit simulator. The result was an extension of the concept of the linear three-port stability factor to three-port non linear circuits, taking advantage of large-signal linearized S parameter simulation tools based on Harmonic Balance (HB), implemented in many circuit simulators (ADS [6.17] was used in this specific case) and allowing the analysis and suppression of possible parametric oscillations. The procedure has been compared with pole and zero identification of a SISO transfer function obtained by Conversion Matrix analysis, previously applied to the study of stability in other circuits such as power amplifiers or oscillators [6.18].

Clearly the three-port μ stability factor applied to large-signal S parameters suffers from the same restrictions as the linear case(ensure stability of the circuit when loaded, but is not able to guarantee the intrinsic stability of the circuit). Nevertheless, it has been

shown how the method can provide a useful and easy to use tool to avoid instabilities considering all the possible passive loading impedances (useful e.g. when a MMIC mixer is connected to waveguides ports, as the impedance shown by the waveguide could be difficult to predict, especially outside the waveguide operating band)

6.3 TWO-PORT AMPLIFIER VERSUS THREE-PORT MIXER: OPERATION REGIMES AND SOLUTION STABILITY

6.3.1 Frequency Domain

The piece-wise Harmonic Balance formulation used to model a microwave amplifier or mixer behaviour in presence of a periodic RF input has usually the following form:

$$A(j\omega)\bar{X} + B(j\omega)\bar{Y}\left[\bar{X}\right] + \bar{G} = \bar{0} \tag{6.1}$$

where the vectors $\bar{X}$, $\bar{Y}$ and $\bar{G}$ contain the harmonics of the circuit state variables (voltages and currents), the nonlinear sources and the RF generators, respectively. The frequency-dependent matrixes $A(\omega)$ and $B(\omega)$ depend on the frequency basis used to expand the steady state solution in a Fourier series.

When applying this formulation to an amplifier, the steady state solution is periodic at the RF input frequency, f_{RF}. In order to study the amplifier stability, the circuit is analyzed in absence of the RF input, making $\bar{G} = \bar{0}$. In this case, there exists a steady state solution $\bar{X}_{DC}$ of DC type. If this solution is perturbed by a small-signal generator, the behaviour of the harmonic perturbation $\Delta\bar{X}(t)$ is ruled by the following linear differential equation in the Laplace-domain:

$$\left\{A(s) + B(s)J\bar{Y}\left[\bar{X}_{DC}\right]\right\}\Delta\bar{X}(s) = \Delta\bar{G}(s) \tag{6.2}$$

where $J\bar{Y}\left[\bar{X}_{DC}\right]$ is the Jacobian matrix of the vector function $\bar{Y}\left[\bar{X}\right]$, the vector $\Delta\bar{G}(t)$ contains the time-varying harmonic components of the small-signal generator.

When only the component ΔG_j is activated, this Multiple Input Multiple Output (MIMO) system can be compacted into a SISO system obtaining:

$$\Delta X_i(s) = F_{ij}(s)\Delta G_j(s) \tag{6.3}$$

where $F_{ij}(s)$ is usually and admittance or impedance, depending on the selected variables. The rising of an autonomous unstable solution in the amplifier is accompanied by an oscillation of the DC solution. The stability of this solution is determined by the poles of the transfer function $F_{ij}(s)$. When this function is not completely known in the whole range of s, conditions (6.4) are usually valid to determine if $F_{ij}(s)$ has unstable poles or not at $s=j\omega_0$ [6.19].

$$\begin{aligned} &\mathrm{Re}(F_{ij}(\omega_0)) < 0 \\ &\mathrm{Im}(F'_{ij}(\omega_0)) = 0 \\ &\left.\frac{\delta F_{ij}(\omega)}{\delta\omega}\right|_{\omega_0} > 0 \end{aligned} \tag{6.4}$$

On the other hand, when applying the formulation to a mixer, the steady state solution is quasi-periodic at the frequencies of the RF input and the local oscillator, f_{RF} and f_{LO}. In order to study the mixer stability, the circuit is analyzed in absence of the RF input. In this case, there exists a f_{LO}-periodic steady state solution $\bar{X}_0$. If this solution is perturbed by a small-signal generator, the behaviour of the harmonic perturbation $\Delta\bar{X}(t)$ is ruled by the following linear differential equation in the Laplace-domain:

$$\left\{A(j\omega_{LO}+s) + B(j\omega_{LO}+s)J\bar{Y}\left[\bar{X}_0\right]\right\}\Delta\bar{X}(s) = \Delta\bar{G}(s) \tag{6.5}$$

where the vector $\Delta\bar{G}(t)$ contains the time-varying harmonic components of the small-signal generator. When only the component ΔG_j is activated, this MIMO system can be compacted into a SISO system obtaining:

$$\Delta X_i(s) = F_{ij}(s)\Delta G_j(s) \tag{6.6}$$

where $F_{ij}(s)$ is usually and admittance or impedance, depending on the selected variables, including in this case the LO frequency, which makes formally different equations (6.3) and (6.6). The rising of an autonomous oscillating solution in the mixer is accompanied by an unstabilization of the periodic solution. The stability of this solution is determined by the poles of the transfer function $F_{ij}(s)$. Like in the amplifier case, when this function is not completely known in the whole range of s, the conditions (6.7), later discussed in section 5, are usually valid to determine if $F_{ij}(s)$ has unstable poles or not at $s=j\omega_0$ [6.19]. Notice that equation (6.7) is formally different from (4) due to the dependence of $F_{ij}(s)$ with LO frequency.

$$\begin{aligned} &\mathrm{Re}(F_{ij}(\omega_0)) < 0 \\ &\mathrm{Im}(F_{ij}(\omega_0)) = 0 \\ &\left.\frac{\delta F_{ij}(\omega)}{\delta\omega}\right|_{\omega_0} > 0 \end{aligned} \tag{6.7}$$

6.3.2 **Time Domain**

In absence of distributed elements, the amplifier and mixer behaviours can be modelled without approximation by a system of nonlinear differential equations of the form:

$$\dot{\bar{x}}(t) = \bar{F}\left[\bar{x}(t), t\right] \tag{6.8}$$

where $\bar{x}(t)$ represents the set of state variables and $\bar{F}$ is a nonlinear vector function. The explicit time dependence of $\bar{F}$ on the time variable is due to the presence of RF generators. In the case of the amplifier, when analyzing the stability of the DC solution $\bar{x}_{DC}$ the time dependence in $\bar{F}$ disappears when the RF generator is removed, and the perturbation dynamics is ruled by:

$$\Delta\dot{\bar{x}}(t) = D_X\bar{F}\left[\bar{x}_{DC}\right]\Delta\bar{x}(t) + D_g\bar{F}\left[\bar{x}_{DC}\right]\Delta\bar{g}(t) \tag{6.9}$$

where $\Delta\bar{g}(t)$ is the vector of small-signal perturbation generators. The system (9) is Linear Time Invariant (LTI), and its frequency-domain representation is equivalent to (6.2). In the case of the mixer, when analyzing the stability of the periodic solution $\bar{x}_0(t)$ the perturbation dynamics is ruled by:

$$\Delta\dot{\bar{x}}(t) = D_X \bar{F}\left[\bar{x}_0(t), t\right]\Delta\bar{x}(t) + D_g \bar{F}\left[\bar{x}_0(t), t\right]\Delta\bar{g}(t) \tag{6.10}$$

where $\Delta\bar{g}(t)$ is the vector of small-signal perturbation generators. The system (6.10) is Linear Time Variant (LTV), with the matrixes $D_X \bar{F}\left[\bar{x}_0(t), t\right]$, $D_g \bar{F}\left[\bar{x}_0(t), t\right]$ being f_{LO}-periodic. The frequency-domain representation of this system is equivalent to (6.5). The stability analysis of LTI and LTV systems is a well known topic and will not be object of consideration in this work.

The advantage of the frequency domain approach is that the condition for the transfer functions (6.3) and (6.6) to be unstable can be easily checked in this domain. On the contrary, the identification of the time-domain systems (6.9) and (6.10) for a real amplifier or mixer can be a very difficult task.

6.4 THREE-PORT STABILITY THEORY

6.4.1 Linear Approach

The three-port stability of a network characterized by its scattering parameters can be verified with different techniques: using a set of three conditions as reported in [6.2] or with a single geometrically derived parameter, as presented in [6.1]. The three conditions to be satisfied ($K_3(\Gamma_k)>1$, $F_{ij}((\Gamma_k)>|J(\Gamma_k)|$ and $F_{ji}((\Gamma_k)>|J(\Gamma_k)|$) locate the terminations Γ_k (k:1,2,3) on the Smith Chart, which will guarantee the unconditional stability between ports i and j. F_{ij}, K_3 and J are functions of the load reflection coefficients Γ_k and of the three-port network scattering parameters (detailed expression of the functions can be found in the annex to [6.1]). The same result can be obtained with a single condition $\mu_3(\Gamma_k)>1$ for unconditional stability. Nevertheless, with $\mu_3(\Gamma_k)<1$ it is still possible to have a useful design, evaluating the Minimum Stable Distance (MSD) from the load reflection coefficient to the unstable region to ensure enough stability margin [6.3**Error! Reference source not found.**].

6.4.2 **Non-Linear Extension Under Large Signal Pumping**

In nonlinear three-port circuits such as active mixers, with capability to provide conversion gain, stability can become an issue. A exhaustive but complex and time consuming analysis procedure for such a circuit is presented in [6.20] An easier-to-implement procedure is proposed and discussed here: starting from the unconditional stability criteria for two ports and assuming a fixed load termination in a third port, the formulation presented in [6.1] can be extended considering linearized scattering parameters under large-signal pumping. As a previous step, the Rollet proviso [6.6] for intrinsic circuit stability must be verified to ensure meaningful results (absence of complex conjugate poles with positive real part, Right Half Poles –RHP- of the three-port network with open ended ports). If this condition is not fulfilled, the method is no longer valid, reason why some authors question the utility of the Rollet condition.

In the case of three ports under large-signal pumping, verification of Rollet's proviso is quite demanding: the circuit has to be linearized around a periodic (LO) regime and verification that with the three unloaded ports the circuit does not oscillate is not sufficient; considering LO injection, a parametric pole-zero identification is required.

In Figure 6.1, a simplified diagram of the up converter circuit under consideration is sketched. In case of down conversion, RF and IF ports should be inter-changed.

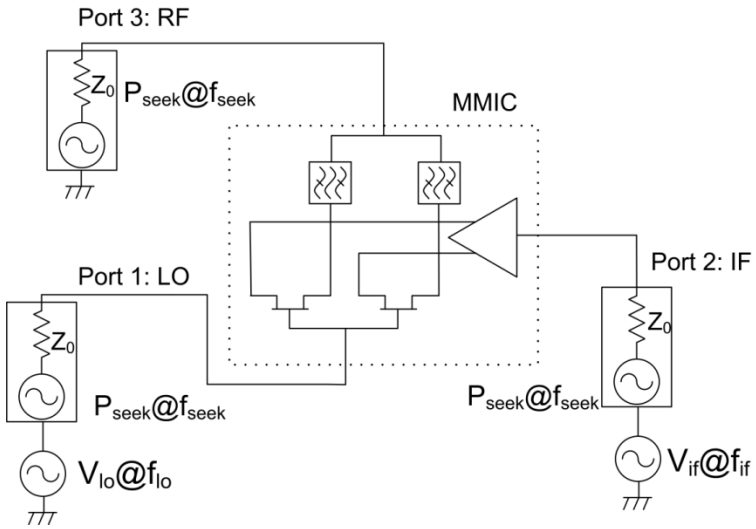

Figure 6.1 *: Test-bench for linearized S parameter simulation under large-signal pumping. Simplified block diagram of the mixer is also detailed*

A low power level (P_{seek}) is injected at the small-signal frequency variable f_{seek} in the linearized circuit to obtain the Scattering parameters at f_{seek}. The frequencies and powers of the local oscillator (LO) and intermediate frequency (IF) signals are f_{lo}, P_{LO} and f_{if}, P_{IF} respectively (up-conversion is considered). In case of a quasi-periodic regime under IF/RF pumping it would be possible to take into account a high level of IF/RF to perform a simultaneous analysis of gain compression and stability. The list of variables and parameters must include the biasing of the circuit (V_{bias}) as it affects the linearization point as well as the level of injected power.

A Harmonic Balance (HB) simulator is required to perform this analysis with at least one (LO) or two (LO and IF) large-signal sources and one small-signal source. Aliasing of frequencies in the harmonic balance frequency base may provide erroneous results, therefore it must be avoided.

Large-signal scattering parameters may already be implemented in the simulator or not. If not, it is possible to emulate their computation with virtual couplers, injecting the test signal alternatively from the 3 ports. If they are already included in the simulator, care has to be taken to load the 3 ports appropriately. The scattering parameter ports have fixed impedances Z_0 (normally 50 Ohm), which will also load the large-signal pumping source. These sources must be voltage type in series, or current type in parallel, with amplitude fixed in agreement with the generator/reference impedances and the available power expected from them (see eq. (6.11) for voltages):

$$v_{lo} = 2\sqrt{2.Z_0.P_{lo}} \qquad v_{if} = 2\sqrt{2.Z_0.P_{if}} \tag{6.11}$$

The linearized scattering matrix (6.12) is a function of f_{seek}, which acts as an independent variable, and depends on a set of parameters: f_{LO} ,P_{LO} , f_{IF} , P_{IF} and V_{bias} therefore S_{ij} (f_{LO} ,P_{LO} , f_{IF} , P_{IF} , V_{bias}).

$$\begin{aligned} S_{ij}(f_{seek}) &= \left[\frac{b_i(f_{seek})}{a_j(f_{seek})}\right]_{a_i(fseek)=0,Plo(flo),Pif(fif),Vbias} \\ b_i(f_{seek}) &= \frac{V_i(f_{seek}) - I_i(f_{seek})Z_0}{2\sqrt{Z_0}} \\ a_j(f_{seek}) &= \frac{V_j(f_{seek}) + I_j(f_{seek})Z_0}{2\sqrt{Z_0}} \end{aligned} \tag{6.12}$$

where a_j and b_i are incident and outgoing power waves, respectively at f_{seek} .

A sweep in f_{seek} may lead to the evaluation of μ_3 as a function of Γ_k, f_{seek}, f_{LO} ,P_{LO} , f_{IF} , P_{IF} and V_{bias}, where Γ_k are the reflection coefficient of load at port k (k:1-3).

The unconditional stability condition [6.1] becomes:

$$\mu_3(\Gamma_k, f_{seek} , f_{LO} ,P_{LO} , f_{IF} ,P_{IF} , V_{bias})>1 \qquad (6.13)$$

Being

$$\mu_3(\Gamma_k, f_{LO}, P_{LO}, f_{IF}, P_{IF}, V_{bias}) = \frac{N(\Gamma_k,...)}{D(\Gamma_k,...)}$$

Where:

$$N(\Gamma_k,...) = \left|1 - S_{kk}\Gamma_k\right|^2 - \left|S_{ii} - \Delta_{jj}\Gamma_k\right|^2$$

$$D(\Gamma_k,...) = \left|\begin{matrix}(S_{jj} - \Delta_{ii}\Gamma_k)(1 - S_{kk}{*}\Gamma_k{*}) \\ -(\Delta_{kk} - \Delta_3\Gamma_k)(Sii{*} - \Delta_{jj}{*}\Gamma_k{*})\end{matrix}\right| + \left|J(\Gamma_k,...)\right|$$

$$J(\Gamma_k, f_{LO}, P_{LO}, f_{IF}, P_{IF}, V_{bias}) = (S_{ij} + \Delta_{ji}\Gamma_k)(S_{ji} + \Delta_{ij}\Gamma_k)$$

Δ_3=DET[S_{ij}], Δ_{ij} Cofactor of the i,j element of [S_{ij}]. i,j,k= 1,2,3;2,3,1; …

μ_3<1 does not mean necessarily that a spurious oscillation will be present, but it is not the desirable situation, as it requires an additional study to determine the stability margins. Two of the three μ_3 factors (Γ_k k=1,2,3) should be considered, as one termination of the three-port network is fixed while the other two are variable.

Even if the circuit is simulated in large-signal conditions at several frequencies, power waves (a_i, b_i, i:1-3) ratios are evaluated only at the f_{seek} frequency, so this can be seen as a particular application of the Conversion Matrix approach [6.21] under a periodic regime (P_{IF}<<) or a quasi periodic regime.

6.4.3 **Conversion Matrix-Based Pole-Zero Identification**

The identification of poles and zeros obtained by the Conversion Matrix approach [6.15] has been used as a reference for comparing the results obtained with the proposed method. Harmonic Balance oscillation analysis and transient simulations have also been used to validate stability.

The circuit was analyzed in HB with LO pumping and RF/IF injection. The SISO transfer function (6.14) is defined injecting a current source I_n at the frequency f_{seek} (non rationally related to f_{lo}, f_{RF} or f_{if}) in a sensitive node *n* and evaluating the voltage on it ($V_n(f_{seek})$). As a current source, it acts as an open circuit at all other frequencies, including at the pumping frequency.

$$H_n(f_{seek}) = \left[\frac{V_n(f_{seek})}{I_n(f_{seek})} \right]_{Plo(flo)} \tag{6.14}$$

Therefore, the evaluation of this transfer function is a particular case of the Conversion Matrix approach. Thus, poles and zeros, fitted to the transfer function by least squares, are obtained and plotted. The existence of complex conjugate poles with positive real part ($\sigma>0$) denotes a potential oscillation condition.

The choice of the sensitive node requires some designer expertise because poles of the transfer function are supposed to be the same in any node, but pole-zero cancellation may happen in some nodes, masking unstable poles [6.20]. Terminals of active devices are usually the most suitable choice, and the repetition of the analysis from different nodes is advisable. In contrast with the μ factor technique, results are limited to the actual impedance terminations used in the analysis.

6.5 **RELATIONSHIP BETWEEN μ, NEGATIVE RESISTANCE, AND CONVERSION MATRIX POLE-ZERO IDENTIFICATION UNDER LARGE SIGNAL PUMPING**

To apply the μ factor, the Rollet's proviso is the basic requirement to be fulfilled. With this assumption, $\mu>1$ implies non fulfilment of oscillation start-up conditions. To establish the relationship with the no-RHP condition, let us consider a two-port network

containing closed feedback loops, which is defined by its linearized S parameters, loaded at the output with a passive impedance Z_L ($|\Gamma_L|<1$), and with two current sources injected at the input with a generator impedance Z_g, for example equal to the reference impedance Z_0 (Figure 6.2). On the one hand, the steady-state solution is periodic due to the presence of the large-signal current source $I(f_{lo})$. On the other hand, the small-signal current source $I_{in}(f_{seek})$ is used to perform the perturbation analysis of the periodic regime.

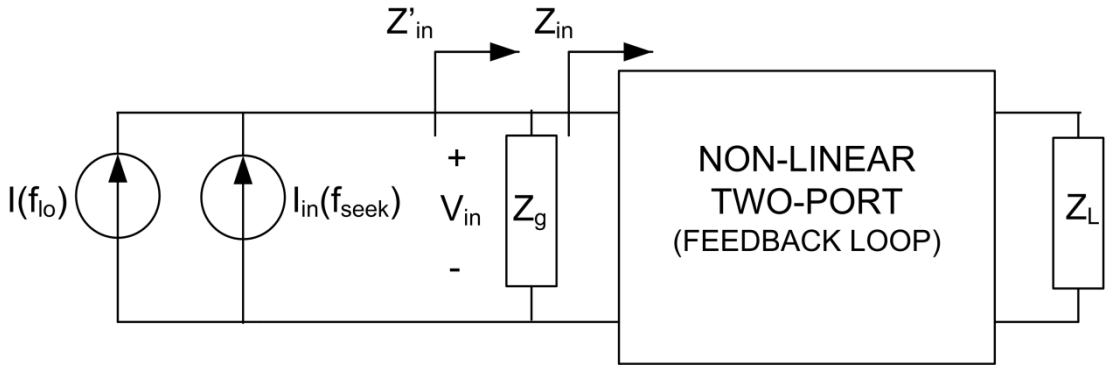

Figure 6.2*: Diagram of the two-port circuit used to apply μ factor from linearized S parameters and to obtain a transfer function Z'_{in} with poles and zeros, under large-signal pumping.*

The input impedance $Z_{in}(\Gamma_L)$ at f_{seek} is directly related to the corresponding input reflection coefficient Γ_{in} (15). In (6.15) $\Delta=S_{11}S_{22}-S_{12}S_{21}$ and Z_0 is a real and positive reference impedance. Z_{in} at f_{seek} and, therefore Z'_{in}, if Z_g is embedded in the two-port network, can also be considered as SISO transfer functions of the system, with P poles and Z zeros (6.16).

$$\Gamma_{in}=\frac{S_{11}-\Delta\Gamma_L}{1-S_{22}\Gamma_L}\ ;\ Z_{in}=Z_0\left(\frac{1+\Gamma_{in}}{1-\Gamma_{in}}\right) \tag{6.15}$$

$$Z'_{in}(s)=K\frac{\Pi_{i:1\ldots Z}(s-z_i)}{\Pi_{j:1\ldots P}(s-p_j)} \tag{6.16}$$

In the case that $s=j\omega_{seek}$ ($\omega_{seek}=2\pi f_{seek}$), the transfer function $Z'_{in}(\omega_{seek})$ matches a conventional frequency-dependent impedance expression. This transfer function is evaluated measuring the perturbation voltage at the input V_{in} when the small amplitude

sinusoidal current I_{in} at f_{seek} is injected, always under large-signal pumping $I(f_{LO})$. Instability condition of the periodic solution at a frequency f_0 ($\omega_0=2\pi f_0$) is generally associated with (6.7), which can be rewritten in this case as:

$$\begin{aligned} \mathrm{Re}(Y'_{in}(\omega_0)) &< 0 \\ \mathrm{Im}(Y'_{in}(\omega_0)) &= 0 \\ \left.\frac{\delta Y'_{in}}{\delta \omega_{seek}}\right|_{\omega_0} &> 0 \end{aligned} \tag{6.17}$$

where $Y'_{in}=1/Z'_{in}$. In this case, conditions are not referred to the stability of the DC solution, but to the stability of the periodic regime under $I(f_{LO})$. Rollet's proviso means that the unloaded non-linear two-port circuit does not oscillate i.e. if $Z_L=\infty$ and $\Gamma_L=1$ then $|\Gamma_{in}|<1$ or $\mathrm{Re}(Z_{in}(\Gamma_L=1))>0$. With this hypothesis, $\mu>1$ implies non fulfilment, at least, of the first oscillation start-up condition in (6.17) at a certain frequency f_0 ($\omega_0=2\pi f_0$).

In order to establish oscillating conditions with the presence of RHP, in line with [6.19], it can be assumed that, in absence of pole-zero cancellations, a pair of dominant complex conjugate poles $p=\sigma-j\omega_0$, $p^*=\sigma+j\omega_0$ provides a contribution to $Z'_{in}(s)$ of the form:

$$Z_p(s)=\frac{R}{(s-p)(s-p^*)} \tag{6.18}$$

where R is a constant residue. Eq. 18 can be re-written for the variable $s=j\omega_{seek}$ as:

$$Z_p(\omega_{seek})=\frac{R}{(\sigma^2-\omega_{seek}^2+\omega_0^2)-j2\sigma\omega_{seek}} \tag{6.19}$$

It can be verified that:

$$sign\left(\frac{\delta(ang(Z_p(\omega_{seek}))}{\delta\omega_{seek}}\right)=sign\left(2\sigma\frac{\left(\sigma^2+\omega_0^2+\omega_{seek}^2\right)}{\left(\sigma^2+\omega_0^2-\omega_{seek}^2\right)^2}\right) \tag{6.20}$$

Therefore, $\sigma>0$ implies $\delta(\text{ang}(Z'_{in}(\omega_{seek})))/\delta\omega_{seek} >0$ and vice versa. On the other hand, for any angle φ and any independent variable x:

$$\text{sign}\left(\frac{d\varphi}{dx}\right) = sign\left(\frac{d(\tan(\varphi))}{dx}\right) \tag{6.21}$$

and the relationship defined in eq. 6.22:

$$\tan(\text{ang}(Z'_{in}(\omega_{seek})) = \frac{-im(Y'_{in}(\omega_{seek}))}{real(Y'_{in}(\omega_{seek}))} \tag{6.22}$$

According to what reported in [6.19], supposing a slow variation of $real(Y'_{in}(\omega_{seek}))$ with ω_{seek}, the fulfillment of (6.17) would be equivalent to having a positive value of σ, corresponding to an unstable pair of complex conjugate poles. For a rigorous determination, pole-zero identification should be applied to $Z'_{in}(\omega_{seek})$ under a given pumping level $I(f_{LO})$.

This is valid for a Z_{in} or Z'_{in} obtained by the matrix conversion approach from a two-port large signal pumped at a given frequency f_{LO} (see fig. 6.2) non-rationally related to f_{seek}, and loaded with a passive Z_L. It can also be generalized to a three-port circuit.

Nevertheless, we should mention that negative resistance stability criteria may lead to incorrect predictions in some cases, as negative real part of resistance/admittance is only one of the three conditions of the oscillation start-up (6.17), but there are another two. However, an oscillation starting up is not the same as an oscillation being maintained over time. Moreover, depending on the complexity of the circuit and on the port where impedance is measured, instability may be hidden, as happens with the observation node to obtain a SISO.

As a simple example to check the relationship between the prediction of instability by μ factor and by pole-zero identification, a two-port non linear circuit with fixed poles and zeros has been used (Figure **6.3**)

A quadratic non-linearity constituted by a two-port-voltage-controlled current source provides the dependence on the pumping signal. A Colpitt resonator provides the feedback loop, and two lossy resonators connected to reference impedance terminations serve as input and output networks, fixing the potential oscillating frequency.

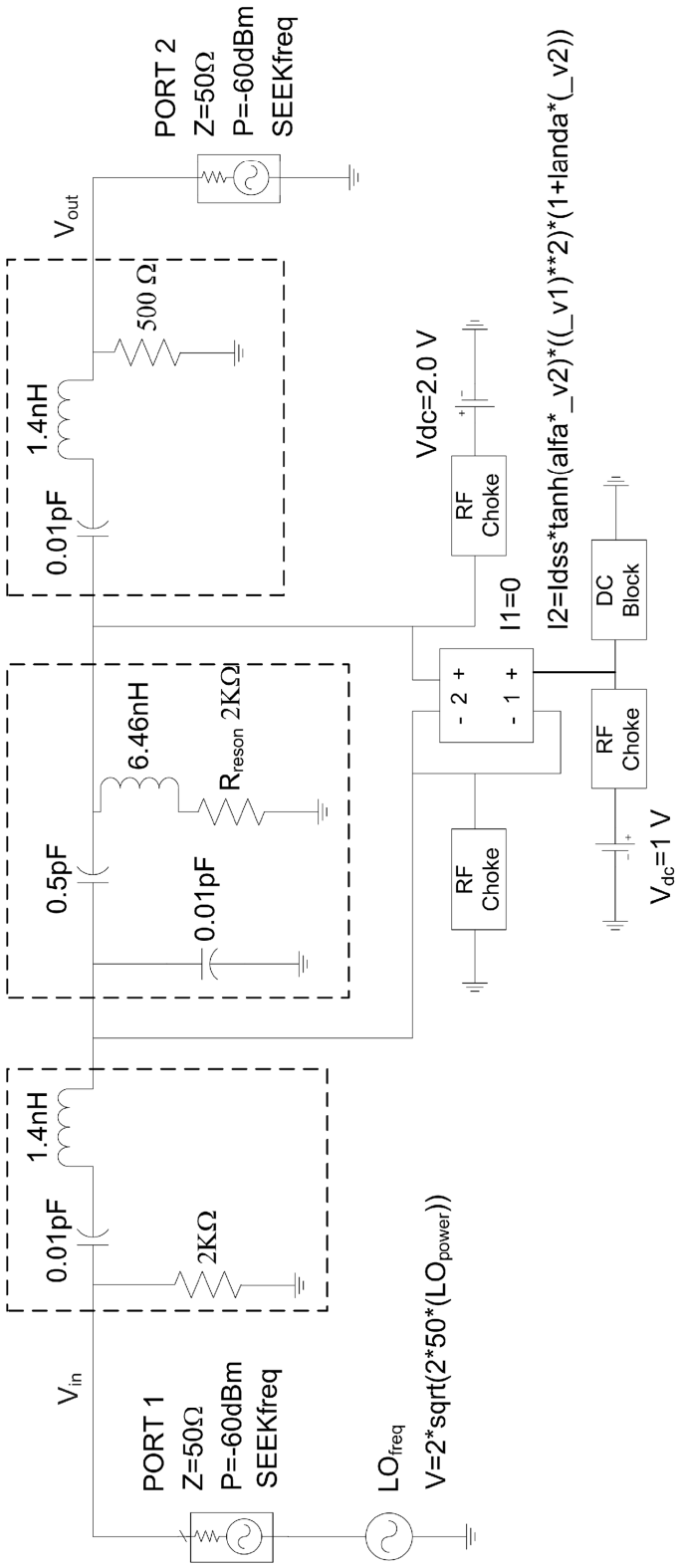

Figure 6.3*: Diagram of the two-port ideal circuit for linearized S parameter and μ factor calculation, and system pole and zero identification under large-signal pumping.*

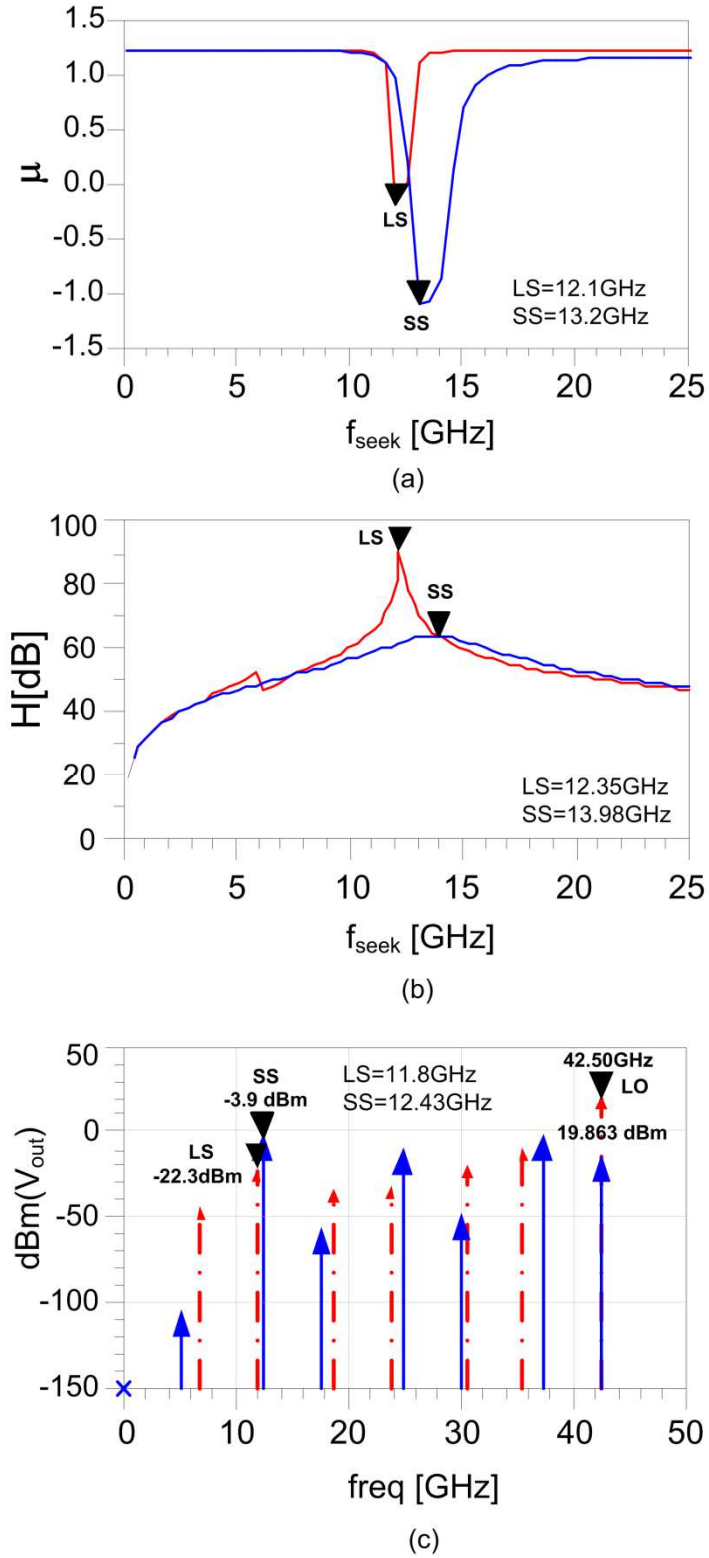

Figure 6.4*: Dependence of the instable frequency on the LO pumping level: (a) Shift in the μ<1 peak; (b) shift in the transfer function peak which corresponds to a shift in the unstable pole from 1.933 109 ± j13.687 109 Hz to 0.049 109 ±j12.294 109; (c) Outp ut spectra showing a shift backwards in the self-oscillation for the highest pumping level (+20 dBm).*

First of all, it was verified the fulfillment of the Rollet's proviso by checking for oscillation conditions after removing 50 Ohm terminations. Then the complete circuit is fed with -20 dBm and with +20 dBm input power for large-signal S parameters and pole-zero identification.

It has been verified (Figure 6.4) that with the large signal applied, there is a shift of the instable frequencies predicted by μ stability factor (fig. 6.4.a) and by the pole and zero identification method (fig. 6.4.b). This was also confirmed by large signal HB oscillation analysis (fig 6.4.c) with a small offset in the values. The peaks in transfer function $H_n(f_{seek})$ defined in eq. (14) (fig. 4b) are close to, but not exactly at the same values as possible instable poles. In this case $+1.933\ 10^9 \pm j13.687\ 10^9$ Hz and $+0.049\ 10^9 \pm j12.294\ 10^9$ Hz. This shows the validity of the dominant pole approach (18). In each case, the shift between potential frequency of oscillation and final oscillation is due to the change of signal level at the frequency f_{seek} from small to large signal as it growths until saturation [6.19].

6.6 APPLICATION TO A MM-WAVE MIXER

The method has been applied in the design of a GaAs mm-wave band MMIC doubly-balanced resistive up converter from L band (0.95-2.15 GHz) to Q band (40.5-42.5 GHz) developed for Multipoint Video Distribution System (MVDS) applications.

Resistive mixing provides the lowest intermodulation levels when the circuit is tuned to a sweet spot bias point [6.22]. A simplified block diagram of the mixer has been shown in Figure 6.1. The LO signal used to feed the mixer is phase shifted with an on-chip divider to obtain complementary signals. The mixer itself has no gain, but as the IF signal is split and amplified before reaching the mixer core, some gain was to be provided in the IF buffer. This circuit is also used to split the IF signal into two branches, one in common gate and the other in common source, providing two out-of-phase IF signals for the balanced operation of the mixer.

Once the preliminary design was carried out, Rollet's proviso was first checked for oscillation conditions with the 3 ports open and both with and without large-signal pumping.

Then the circuit was loaded with Z_0 terminations, as in normal operation. Oscillation test ports [6.17] and admittance probes [6.13] were applied in a wide frequency range to verify the absence of oscillation. Pole-zero identification techniques

were also applied [6.15]. Then the analysis for calculating the μ factor corresponding to the set up shown in Figure 6.1 was performed for typical frequency and power values, showing a potentially unstable behavior around 21 GHz in port 3 (Figure 6.5).

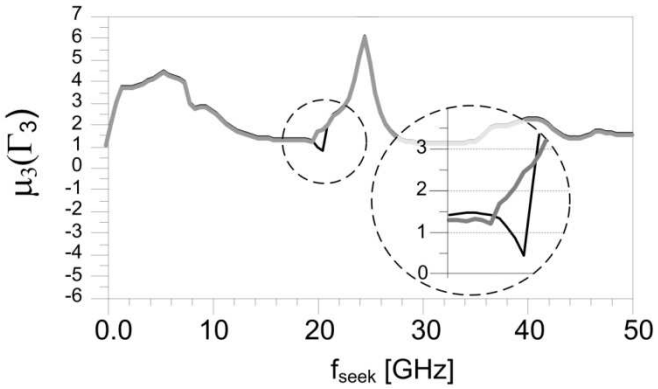

Figure 6.5*: Evaluation of μ_3 from RF port $\mu_3(\Gamma_3)$ versus f_{seek} for f_{LO} =42.5 GHz ,P_{LO} =10 dBm, f_{IF} =1 GHz, P_{IF}=-10 dBm, showing μ_3 <1 around 21 GHz and in the modified circuit μ_3 >1 for all the frequencies.*

Applying the admittance probe and the oscillation test port, a strong signal was found at ~21.8 GHz. The HB output spectrum is shown in Figure **6.6**.

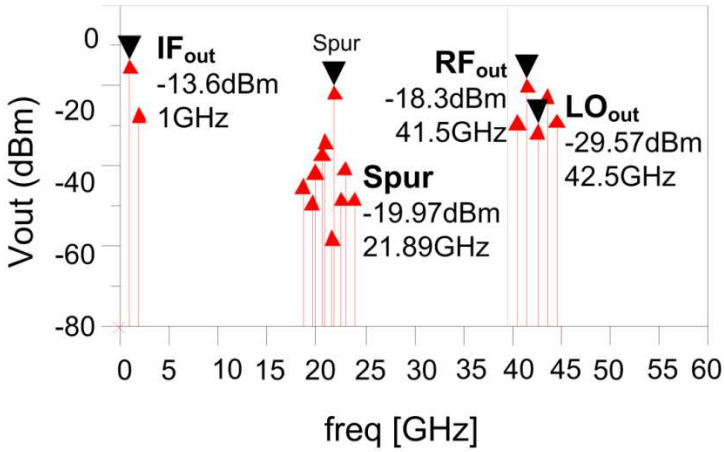

Figure 6.6*: Output spectrum with f_{LO} =42.5 GHz ,P_{LO} =10 dBm, f_{IF} =1 GHz, P_{IF}=-10 dBm, showing the spur oscillation at 21.8 GHz surrounded by lower intermodulation lines.*

The problem was found in the IF buffer which is designed at L band, but whose interconnections seem to be critical at higher frequencies. Therefore, an RLC network resonant at frequencies around 21 GHz was added. The resulting μ_3 is always higher than one (Figure 6.5). The transfer function (6.14) was applied to the circuit and poles and zeros were identified. The evolution of the poles, from the instable zone to the

stable one (left hand side) when the resistance of the RLC network is swept from high to low values is shown in figure 6.7.

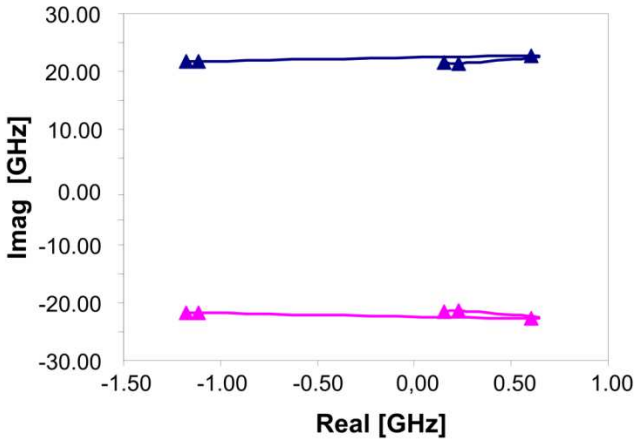

Figure 6.7*: Evolution of the unstable pole around 21 GHz from the right half side to the left half side when a series resistor in the RLC trap is swept from high to low values.*

The shift in the poles matches the shift from μ_3 <1 to μ_3>1. The HB output Spectrum of the circuit when μ_3 <1 (figure 6.7) confirms the presence of a spurious tone in that case.

The proposed method enables the evaluation of unconditional stability under different levels of LO power. In general, LO signal level is a relevant parameter to which the generation or extinction of spurious oscillations could be associated. In this case, high levels of LO power around 40 GHz may be difficult to generate due to inherent losses. For this reason, μ_3 from IF port stability factor ($\mu_3(\Gamma_2)$) has been simulated in a quasi-periodic regime for a fixed P_{IF} (-10dBm) sweeping f_{seek} and P_{LO} below the nominal value (Figure 6.8), showing stable conditions in the sweeping range.

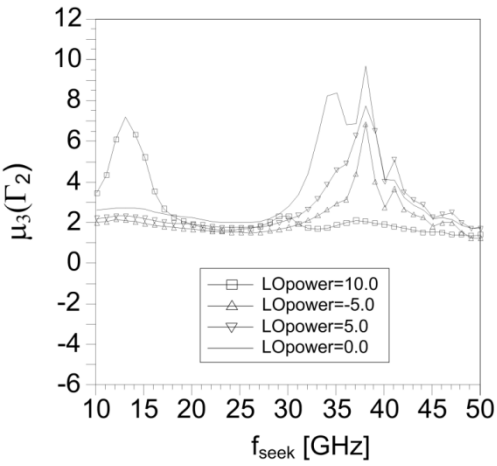

Figure 6.8*: Evaluation of μ_3 from IF port $\mu_3(\Gamma_2)$ versus f_{seek} for f_{LO} =42.5 GHz , f_{IF} =1 GHz, P_{if}.=-10 dBm, sweeping P_{LO} from -5 to 10 dBm (P_{LO} nominal is 10 dBm).*

If $\mu_3<1$, further stability analysis would be required. It should be remarked that unlike in a two-port circuit where a single μ_2 factor provides all the information, in a three-port circuit two μ_3 factors should be considered, as one termination of the three-port is fixed while sweeping the other two.

6.7 UP-CONVERTER MEASUREMENTS AND PERFORMANCE

The application of the method enabled stability issues to be addressed and the final design to be completed. The technology used was the commercial Pseudomorphic High Electron Mobility Transistor (HEMT) process by OMMIC with 0.2 µm gate length and f_t over 60 GHz.

A microphotograph of the fabricated circuit is shown in figure 6.9. This photograph can be compared with circuit topology schematic in figure 1. LO input is split into two branches with different phases to be applied to both transistor gates while IF input amplified and phase shifted is applied to the corresponding sources. RF signal is collected in phase from both drains.

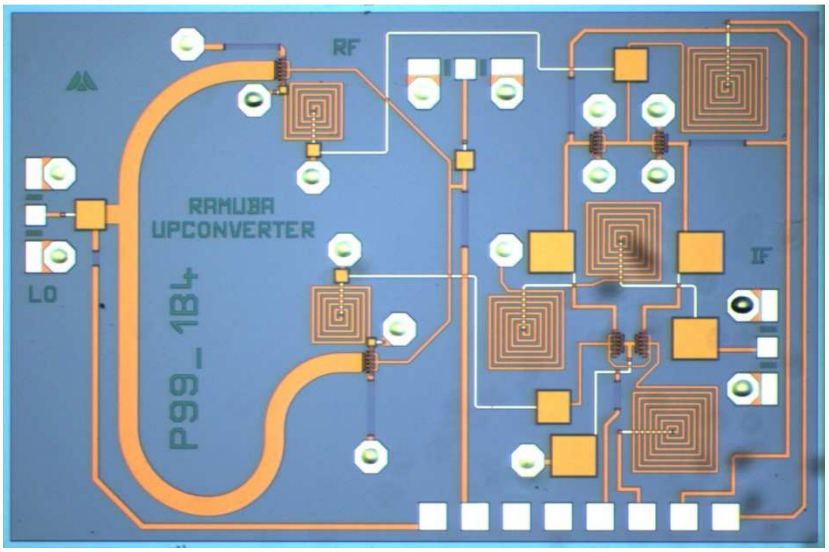

Figure 6.9: Photograph of the up-converter MMIC. Size is 2 x 3 mm^2. The corresponding circuit topology simplified schematic appears in fig. 1.

During measurements no spurious oscillation was observed for any bias point or power level around their nominal values. Measured and simulated gain conversion and LO isolation are plotted in Figure 6.10 and Figure 6.11. 2.5 EM simulations (Momentum®) were used to improve agreement between simulations and measurement. It should be mentioned that inter-modulation performance has been improved (~12 dB decrease in spectral re-growth) by slightly biasing mixer drains from 0 to 1 V [6.22]. The spectral re-growth plot is shown in Figure 6.12.

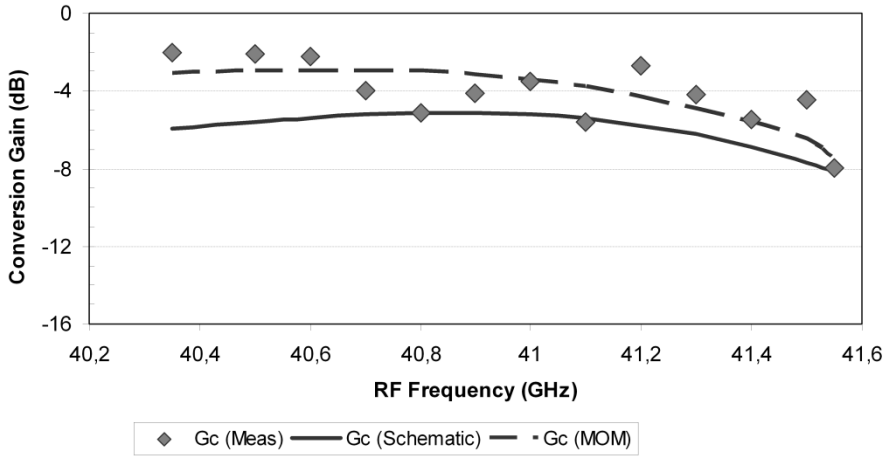

Figure 6.10*: Measured and simulated conversion gain (schematic circuit model and Method of Moments, MOM) LO power = 6 dBm.*

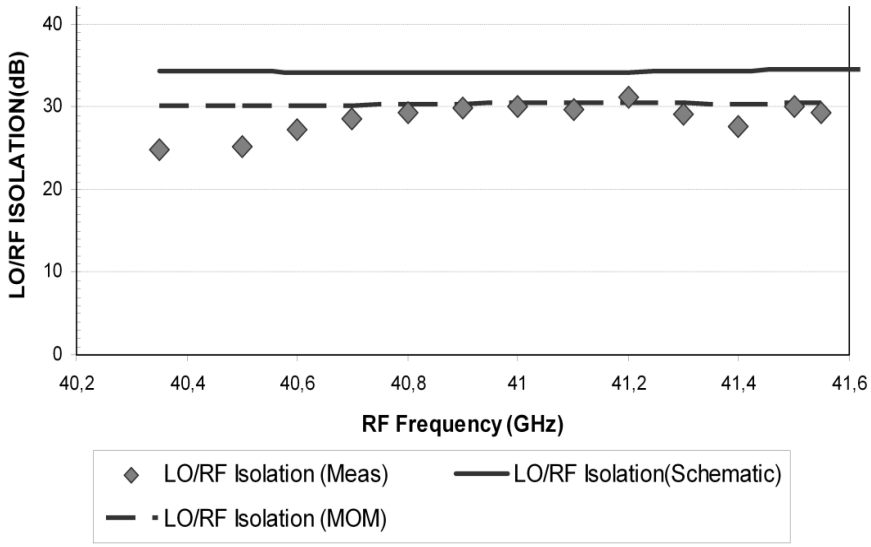

Figure 6.11*: Measured and simulated LO isolation (schematic circuit model and Method of Moments). LO power = 6 dBm.*

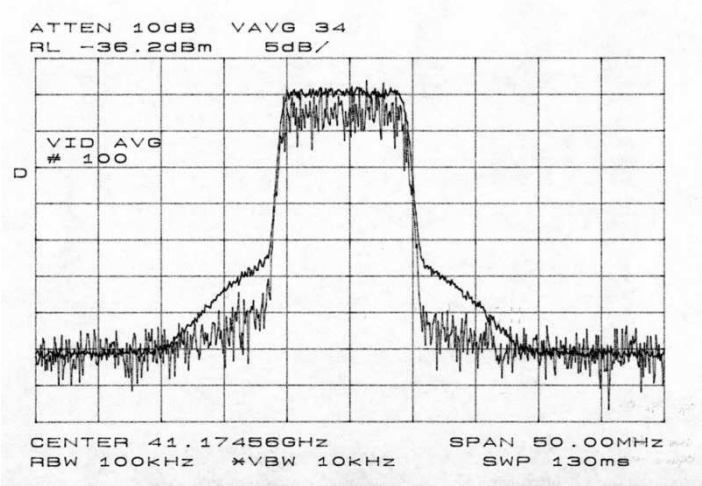

Figure 6.12*: Spectral re-growth for two values of drain mixer voltage: 0 V and 1 V Measurement conditions: 10 MHz bandwidth QPSK, f_{IF}:1.3 GHz, P_{IF}=-10 dBm, P_{LO}=6 dBm.*

6.8 CONCLUSIONS

The non-linear extension of the μ factor defined for linear 3-port circuits to those operating under large-signal regime has been described and compared with Matrix Conversion based pole-zero identification. μ factor is restricted to the fulfillment of Rollet´s proviso, but in most cases it may enable a huge saving in time, compared to in-depth non-linear stability techniques as with μ_3 >1 no spurious oscillations would be expected. If μ_3<1, an additional stability analysis with Conversion Matrix would be required. μ factor takes into account all possible passive loads while the transfer function obtained by Conversion Matrix is only valid for the given load impedances. Both methods have been applied in the design of a mm-wave band MMIC up-converter, successfully avoiding unwanted oscillations in the fabricated prototype.

6.9 REFERENCES

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7 . Conclusions

7.1 SUMMARY

The work presented in the previous chapters summarizes part of the activities carried out during many years of research and development spent at the University of Cantabria in the field of microwave circuit design.

This PhD thesis dissertation has dealt with the design, analysis and implementation of custom GaAs MMIC circuits covering different functionalities. Several circuits have been presented from the conception to the final implementation and characterization, the scope being providing a detailed guideline in support of future works in this field.

As a proof of the efficiency and validity of the processes which have been followed, it could be noticed how all the proposed circuits resulted in successful first-run implementations (second and final flight runs were required to fine tune performances) and how nowadays most of the circuits are successfully used in a commercial product and several on-going space mission.

Not only the main features of each circuit and the detailed design and characterization flows has been presented (with a constant focus on all the practical and physical implementation aspects), but also specific design methodologies (e.g. how to implement a gain control, how to realize a frequency divider…) and analysis techniques which could be applied transversally to various families of circuits have been proposed to ease and make more reliable the work of the microwave circuit designer.

Detailed conclusions of each chapter have been already presented, however it is worth recalling here those results which have been considered as mostly contributing to an advance in the field on MMIC circuit design and analysis. In particular:

1. A straightforward method to design compact linear-in-dB VGAs with good input/output matching and power handling capability has been presented and

demonstrated through its successful first-run implementation of a fully monolithic GaAs VGA (chapter 2) with very good performance[5]

2. A novel dual-modulus prescaler topology has been reported. The topology is in principle capable to overcome most of the speed limitations of conventional dual-modulus dividers and this has been demonstrated through two consecutive design steps (chapter 3 and 4)
3. A digital frequency divider model based on the "switched ring-oscillator" concept, suitable for dividers with even, odd, fixed and variable division ratios has been described and a simple procedure to design a dual modulus prescaler combining the topologies of two consecutive order dividers has been proposed (chapter 4).
4. Phase noise simulation of digital frequency dividers based on HB simulation has also been presented. The method, using a full non-linear and noise model of the individual transistors, can provide a test bench to develop accurate modeling of noise sources (chapter 4).
5. A dual out-of-phase auxiliary generator has been proposed as an HB tool for the analysis of balanced and differential circuits and Envelope-Transient has been used, for the first time to the authors knowledge, to analyze digital frequency division mechanisms and the change in the division ratio of a dual-modulus dividers (chapter 4).
6. The derivation of a parametric microwave package model has been described and the developed model has been validated for use through the implementation of a set of MMIC circuits for space application (chapter 5).
7. A detailed stability and thermal analysis of a multistage power amplifier has been provided in support of a successful implementation and reliable use of this type of circuits (chapter 5)
8. A simplified methodology to determine stability in non-linear three-port circuits based on a generalization of the three-port μ-stability factor applied to linearized S parameters under large-signal pumping has been derived

[5] *The performance and figure of merits have been referenced by authors as among the state-of-the art VGA at the time of publication (e.g. Masud, M.A. ; Zirath, H. ; Kelly, M. "A 45 dB variable gain low noise MMIC amplifier" , IEEE Transactions on Microwave Theory and Techniques, Volume:54 , Issue: 6 , June 2006)*

(chapter 6), and validated with the design and measurements of a implemented mm-wave MMIC mixer.

In addition to the above mentioned "foreground", the activities carried out in these years have allowed to mature an established MMIC design competence within the University of Cantabria which have been successfully used for the implementation of many other circuits and projects. Additionally, all the knowledge and experience has been transferred to the industry (in the form of design documentation) and supported the establishment of a custom integrated circuit design team within the Spanish company ACORDE (www.acorde.com) with a long record of successful designs. As a proof of the work which has already benefit from the achievements described in this dissertation and which has not been included for sake of "readability" of this document, a non-exhaustive list of publications which have directly exploited the techniques and experience matured in these years and applied to other fields is reported hereafter.

7.2 WAY FORWARD

My hope for this work is that it has advanced the practice of microwave circuit design and analysis. I tried to transmit as much as possible (and as much as I was allowed to do) my experience and knowledge to many other engineers working in this exciting field. I have attempted to innovate without losing sight of the practical side of engineering. The road has been difficult but I firmly believe that the effort has been worth the journey.

As additional recommendations for future work to be carried out based on the result of this Dissertation I believe that at least the following should be taken into account:

- The further demonstration of the dual-modulus divider design methodology and topology with CMOS technology and targeting the highest operational speed. Taking into account that the performance obtained with GaAs are today still unrivalled [6], there could be the possibility to push forward the

[6] *The achieved performances are still referenced in recent publications (e.g Nan,.et al "A 6-GHz dual-modulus prescaler using 180nm SiGe technology", 13th International Symposium on Integrated Circuits (ISIC), 2011, and K Wang "Low-power high-speed dual-modulus prescaler for Gb/s applications", IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2012)*

performance in terms of speed-power consumption figure of merit toward an improvement of the State of the art;

- The full implementation of the TT&C radio frequency chain could be upgraded and the power consumption further reduced with the use of modern CMOS technologies (greatly evolved since the time in which the original circuits presented in this thesis were conceived, and once demonstrated its suitability for space missions). To this respect work should be started toward the implementation of the following generation of transponder targeting micro satellite;
- The use of HB techniques for the characterization of phase noise in a frequency-conversion context should be further exploited and possibly combined with behavioral modeling to predict more accurately system performance;
- Proposed stability analysis technique under large signal pumping can be applied to power amplifiers evaluating in which power level ranges and topologies it allows to speed up conventional time consuming procedures. Moreover, the multiport concept, inherent in a mixer, could be extended to virtual ports at different frequencies and applied to power amplifiers.

7.3 PUBLICATIONS DIRECTLY RELATED WITH THIS WORK

7.3.1 Publications in International Journals

M. Detratti, J.P. Pascual, M.L. de la Fuente, J. Cabo, J.L.Garcia, " *A GaAs Monolithic Linear-in-dB Wide-Dynamic-Range Variable Gain Amplifier with Matching Compensation for 1.95 GHz Applications"*, Microwave and Optical Technology Letters, February 2005

C. Barquinero, M. Detratti, A. Herrera, J.L.Garcia, J. Cabo, *"Multimode GaAs chip-set for new S-band satellite TT&C transponders"* IEEE Transactions on Aerospace and Electronic Systems, Volume: 44 , Issue: 3. 2008 , Page(s): 1029- 1041

M. Detratti, J.P. Pascual, "*Variable-ratio digital frequency dividers: Analogue design methodology and phase noise analysis based on harmonic balance*"

International Journal of RF and Microwave Computer-Aided Engineering vol. 19 issue 5 September 2009. p. 529 – 539

M. Detratti , B. Aja, Ma. L. de la Fuente, S. Sancho and J. P. Pascual, *"Nonlinear circuit stability under large-signal pumping: Three-port μ stability factor versus conversion matrix system identification—application to a millimeter-wave band MMIC up-converter"*, International Journal of RF and Microwave Computer-Aided Engineering Volume 20, Issue 6, November 2010, Pages: 711–720

7.3.2 **Publications in International Congress**

M. Detratti, S. Sotero, C. Barquinero, J. Chuan, J. P. Pascual, M. L. de La Fuente, A Herrera, J. L. García, J. Cabo , J. M. Graña,*"Multifunction MMIC Modules for Space Applications based on a Commercial 0.2um pHEMT Technology"*, XVII Conference on Design of Circuits and Integrated Systems, Santander, Spain, November 2002.

M. Detratti, J.Chuan, J.P. Pascual, *J. Cabo, J.L. Garcia.,"E/D pHEMT Multy Frequency Generator MMIC for Aerospace Applications"*, 33thEuropean GaAs and Other Compound Semiconductors Application Symposium (GAAS2003) Munich, Germany, October 2003.

S. Sotero, J. Chuan, M. Detratti, C. Barquinero, A. Herrera, M. L. de la Fuente, J. P. Pascual, J.L. Garcia(, J. Cabo, E. J. López, *"GaAs pHEMT Multifunction MMIC Modules for Satellite Applications at S Band"*, ESA Workshop on Tracking, Telemetry and Command Systems for Space Applications, Darmstadt, Germany, September 2004.

M. Detratti, J. P. Pascual, M. L. de la Fuente, J. L. García, J.Cabo**,** *"An S-Band MMIC Linear-in-dB Wide-Dynamic-Range Variable Gain Amplifier with Matching Compensation"* 16th International Conference on Microelectronics (ICM2004), December 2004.

M. Detratti, J. Cabo, J.P. Pascual, A. Herrera, *"A 4.5 GHz 3-4 Dual-Modulus Frequency Divider IC in GaAs Technology"*, 32thEuropean Microwave Conference (EuMC2005), Paris, France, October 2005

7.3.3 **Publications in National Congress**

C. Barquinero, M. Detratti, S. Sotero, J. Chuan, A. Herrera, J. Cabo, *" Modulos MMIC Multifunción para Aplicaciones Espaciales"*, XVIII Simposium Nacional de la URSI, La Coruña, Septiembre 2003.

7.4 **OTHER PUBLICATIONS**

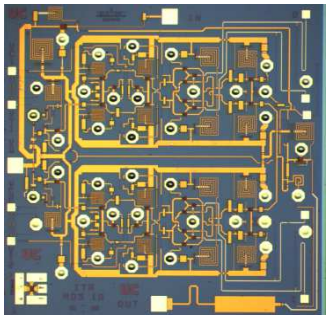
In this section, a non-exhaustive list of publications which are based on the MMIC design and analysis techniques which have been presented in this work are presented.

A. Georgiadis, M. Detratti, S *"A linear, low-power, wideband CMOS VCO for FM-UWB applications"*, Microwave and Optical Technology Letters, Vol. 50 , Issue 7, pp 1955-1958, July 2008.

M. Detratti, E. Lopez, E. Perez, R. Palacio, M Lobeira , *"Dual-band RF receiver chip-set for Galileo/GPS applications"*, IEEE International Position, Location and Navigation Symposium, 2008 IEEE/ION, pp 851-859, 2008

M. Detratti, E. Perez, J. Gerrits, M Lobeira, *"A 4.6mW 6.25–8.25 GHz RF transmitter IC for FM-UWB applications"*, IEEE International Conference on Ultra-Wideband, ICUWB 2009, pp 180-184, 2009

J. Gerrits, H. Bonakdar, , M. Detratti, E. Perez, M Lobeira,Y. Zhao, Y. Dong, G. Van Veenendaal, J. Long, J. Farserotu, E. Leroux, C. Hennemann, *"A 7.2 – 7.7 GHz FM-UWB transceiver prototype"*, IEEE International Conference on Ultra-Wideband, ICUWB 2009, pp 580-585, 2009



ANNEX I: ISBT Transponder Datasheet

Integrated S-Band Transponder (ISBT)

Multimode in-orbit reconfigurable Communications Transponder

Applications

- TCR and data transmission subsystems for Scientific and Earth Observation satellites (LEO & GEO).
- TCR subsystems for Navigation and Telecommunications satellites.
- Communications subsystems for manned and unmanned space vehicles.
- Intersatellite links for Data Relay, Rendezvous and Docking, etc.

Main features

- Compatible with ESA (ECSS-E50-05) and NASA (SNUG 450) standards.
- Compatible with most Satellite Platforms worldwide.
- In-orbit configurability by Telecommand:
  - Coherent / non-coherent
  - Rx/Tx Frequency
  - Rx/Tx Modulation formats
  - TC/TM Data Rates
  - Ranging mode
  - PN code seed (spread spectrum)
- Multimode Telecommand & Ranging Receiver
  - Modulation formats: PCM/BPSK/PM, PCM/SP-L/PM, BPSK (suppressed carrier), SS-BPSK, (U)SQPN, UQPSK (spread spectrum) TDRSS compatible
- Multimode Telemetry & Ranging Transmitter
  - Modulation formats: PCM/BPSK/PM, PCM/SP-L/PM, BPSK (supp. carrier), (O)QPSK, SRRC/OQPSK, GMSK, SQPN (spread spectrum TDRSS compatible)
- Multi-standard Ranging (ECSS E50-02, SNUG 450)
- Product options include:
  - Corona-free diplexer.
  - High stability reference

Production

- Typical lead time is 14 months.

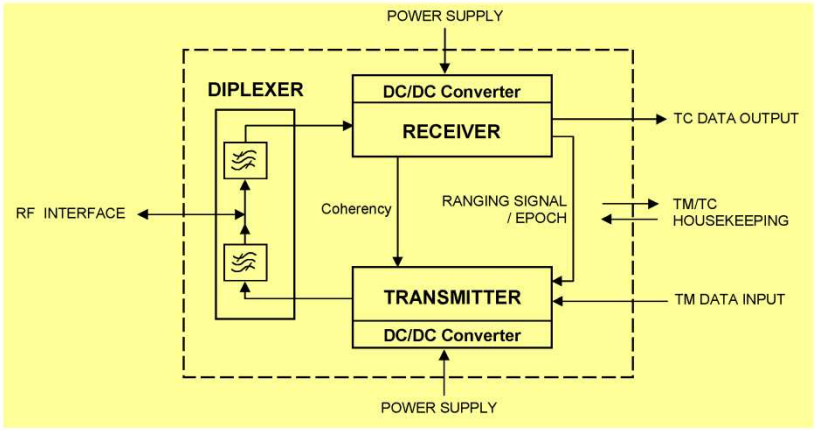
Technical description

- Three independent modules: Receiver, Transmitter and Diplexer assembled together as a single equipment.
- High performance RF sections based on highly integrated MMIC technology.
- IF sections highly integrated in analog ASIC's.
- TC demodulation, TM modulation and low frequency functions in general based on advanced DSP techniques and devices.
- Highly stable local oscillators.

Background

- Over 60 transponders sold for programs Galileo IOV, CryoSat 2, Swarm, SAOCOM, Aquarius/SAC-D, Sentinel 1, 2 & 3, Ingenio, EarthCare, AstroTerra (SPOT 6 & 7), COTS/Cygnus, OCO 2, Skynet 5D, Egypt-Sat, KompSat 3, Kazakhstan, Athena-Fidus, Sicral 2…
- 180 transponders sold world-wide from previous product generations: Telecom 2, SPOT 4 & 5, Helios 1 & 2, XMM-Newton, Integral, Hot Bird 2, 3, 4, 5, 6, 7A, 8, 9 & 10, WorldStar, SOHO, Cluster I & II, Eutelsat W1R, W3A & W2M, Hispasat 1A, 1B, 1C & 1D, Jason 1 & 2, ETS VIII, METOP A, B & C, ATV, MTSat 1R & 2, ROCSAT 2, SciSat, SMART 1, Syracuse 3A & 3B, HTV, GOCE, CryoSat, Pleiades-HR 1 & 2, Skynet 5A, 5B & 5C, ADM-Aeolus, THEOS, CALIPSO, COROT, SMOS, Megha-Tropiques, COMS 1, CASSIOPE, OCO, IBEX, COMSATBw 1 & 2, Ka-Sat, Quasi-Zenith...

ISBT Block Diagram



Typical performances

Receiver	*Transmitter*
♦ S-Band (2025-2120 MHz) ♦ Carrier Acquisition Threshold: -128 dBm ♦ Input dynamic range: -128 to –50 dBm ♦ Noise Figure: < 4.2 dB (including diplexer) ♦ Telecommand bit rates up to: - 4 kbps PCM/BPSK/PM - 64 kbps PCM/SP-L/PM - 300 kbps (U)SQPN, UQPSK (spread spectrum TDRSS Compatible) - 2 Mbps BPSK ♦ Telecommand subcarrier: 8 or 16 kHz (for BPSK/PM) ♦ Frequency stability: - Initial setting: ± 5 ppm - Global: ± 20 ppm - Option TCXO ± 1ppm temperature stability ♦ Receiver power consumption: 5 W typ	♦ S-Band (2200-2300 MHz) - Coherent mode ratio: $F_{TX} = \frac{240}{221} F_{RX}$ ♦ Frequency stability: as in receiver ♦ Phase noise: < 3°rms ♦ Telemetry bit rates up to: - 50 kbps PCM/BPSK/PM - 250 kbps PCM/SP-L/PM - 300 kbps SQPN (spread spectrum) - 8 Mbps suppressed carrier modes - High rate GMSK modulation ♦ RF Output Power: up to 37 dBm (higher with external module) ♦ Tx Power consumption: 25 W (P_{RF} = 37 dBm)
Ranging	***General***
♦ Ranging modes: - ESA / NASA two tone and ESA MPTS (typ 450kHz) alone or simultaneous with TM - Regenerative code ranging NASA SNUG 450	♦ Mass: 2.6 kg ♦ Dimensions: 228 x 170 x 194 mm^3 ♦ Primary Bus Voltage: 21 to 52 ♦ Serial interface for TM/TC housekeeping

This datasheet is not contractual and can be changed without any notice. *Updated June 2011 Ed. 2*

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Conclusiones

El trabajo que se ha presentado en los capítulos previos resume parte de las actividades llevadas a cabo durante muchos años de investigación y desarrollo en el campo de diseño de circuitos y sistemas de microondas, pasados en el Departamento de Ingeniería de Comunicaciones de la Universidad de Cantabria.

Esta disertación doctoral ha tratado del diseño, análisis e implementación de circuitos MMIC de AsGa que cubren diversas funcionalidades. Se han presentado diversos circuitos desde la fase de la concepción a su implementación final incluyendo la caracterización completa de las prestaciones, siendo el objeto proporcionar una guía detallada de apoyo a futuros trabajos en este campo. Como prueba de la eficiencia y validez de los procedimientos seguidos debe mencionarse que todos los circuitos propuestos resultaron en implementaciones exitosas a la primera implementación, si bien una segunda versión y una versión de vuelo fueron requeridas para optimizar el funcionamiento al máximo. En la actualidad la mayor parte de los circuitos se están empleando con éxito en productos comerciales y en varias misiones espaciales en curso.

Se han presentado tanto las principales características, así como los detalles del diseño y caracterización de cada circuito (con especial énfasis en aspectos prácticos y de la implementación física). También se han presentado metodologías de diseño específicas (implementación del control de ganancia en un amplificador, implementación de un divisor de frecuencia de razón fija o variable, etc.) y técnicas de análisis orientadas a hacer más fiable el trabajo del diseñador de microondas (estabilidad de los circuitos), que pueden ser aplicadas transversalmente a varias familias de circuitos.

Aunque se han presentado conclusiones detalladas en cada capítulo se considera conveniente repasar aquí las contribuciones más relevantes de cada uno de ellos en el campo del diseño y análisis de MMICs.

En particular:

1.- Se ha propuesto un método directo para diseñar amplificadores de ganancia variable (VGA) compactos y lineales en dB con buena adaptación de entrada y de salida y capacidad de manejo de potencia y ha sido validado con una implementación exitosa en la primera tirada de un circuito monolítico tipo VGA de AsGa con un funcionamiento muy satisfactorio (capítulo 2).

2.- Se ha desarrollado una nueva topología de pre-escalador de doble módulo. Dicha topología es, en principio, capaz de superar las limitaciones en velocidad de los divisores convencionales de doble módulo y se ha validado en dos pasos sucesivos de diseño (capítulos 3 y 4).

3.-Se ha descrito un modelo analógico de divisor digital de frecuencia basado en el concepto de oscilador de anillo conmutado, adecuado para divisores de razón par, impar, fija o variable. A partir del mismo se ha propuesto un procedimiento para diseñar un pre-escalador de doble módulo combinando la topología de dos divisores de órdenes consecutivos (capitulo 4)

4.-Se ha presentado un procedimiento de Simulación del ruido de fase añadido de divisores de frecuencia digitales basado en balance armónico y usando el modelo no lineal completo y el modelo de ruido de los transistores. Esta simulación proporciona también un banco de test para el modelado de fuentes de ruido (capítulo 4).

5.- Se ha propuesto un doble generador auxiliar en contrafase como una herramienta de simulación de balance armónico para circuitos equilibrados diferenciales y por primera vez, según nuestro conocimiento, se ha usado el transitorio de envolvente para analizar el mecanismo de división de frecuencia y el cambio en la razón de división de divisores de doble módulo (capítulo 4).

6.- Se ha descrito la derivación de un modelo paramétrico de empaquetados de microondas, que ha sido posteriormente validado para su uso en un conjunto de MMICs para aplicaciones de espacio (capítulo 5).

7.- Se ha desarrollado un análisis detallado de estabilidad y de comportamiento térmico para fundamentar la implementación satisfactoria y el uso fiable de este tipo de circuitos (capítulo 5)

8.-Se ha propuesto una metodología para determinar de forma sencilla la estabilidad de un circuito no lineal de tres puertos bajo régimen de bombeo en gran señal a partir de una generalización del factor de estabilidad μ de tres puertos aplicado a parámetros de Scattering en gran señal obtenidos bajo dicho régimen de bombeo. El método se ha validado por comparación con otros métodos analíticos y se ha verificado en el diseño y medida de un mezclador MMIC de bandas milimétricas libre de oscilaciones espurias (capítulo 6).

Todas las actividades mencionadas anteriormente han constituido un bagaje que ha contribuido a la madurez de la competencia de diseño de MMICs en la Universidad de Cantabria y que ha sido fructíferamente utilizada en la implementación de muchos otros circuitos y sistemas dentro de diversos proyectos. También este conocimiento se ha transferido a la industria en forma de documentación de diseño y de apoyo al establecimiento de un grupo de diseño de circuitos integrados a medida dentro de la empresa española spin-off ACORDE (www.acorde.com) con un largo historial de diseños exitosos. Prueba de las tareas que se han beneficiado de las contribuciones de esta tesis es la lista adicional de publicaciones que se incluye, en las que se ha explotado la experiencia y la técnica adquiridas durante estos años, pero que no se han incluido en el trabajo de tesis para mantener acotada su extensión y facilitar su lectura.

Perspectivas

La esperanza del autor respecto a este trabajo es que haya contribuido al avance del diseño y análisis de circuitos de microondas. Se ha intentado transmitir lo más posible la experiencia y conocimientos adquiridos a otros ingenieros trabajando en este campo tan estimulante. Se ha intentado innovar, pero sin perder de vista el lado práctico de la ingeniería. El camino fue difícil, pero el esfuerzo ha merecido la pena.

Como recomendaciones para la orientación de futuros trabajos basadas en los resultados de esta disertación, se cree que al menos los siguientes aspectos deberían ser tenidos en cuenta:

- Demostración de la metodología de diseño y de la topología propuestas para el divisor de doble módulo con tecnología CMOS y enfocado a conseguir la más alta velocidad de operación. Teniendo en cuenta que las prestaciones del divisor de doble módulo propuesto e siguen representando el estado del arte en tecnología de AsGa, existiría la posibilidad de dar un empujón a su funcionamiento en términos del compromiso velocidad-consumo de potencia hacia una mejora en el estado del arte.
- La implementación completa de la cadena de RF de TT&C puede ser mejorada y el consumo de potencia más reducido aun con el uso de modernas tecnologías CMOS (muy evolucionadas desde el momento en que se concibieron los trabajos de esta tesis y una vez demostrada su compatibilidad con las misiones espaciales). Respecto a esto se debería trabajar hacia la implementación de traspondedores para micro satélites.
- El uso de técnicas de balance armónico (HB) para la caracterización del ruido de fase en un contexto de conversión en frecuencia se podría explotar más aun, con la posibilidad de combinarse con el modelado comportamental para predecir con más precisión el funcionamiento de los sistemas.
- La técnica de estudio de la estabilidad propuesta podría ser aplicada a amplificadores de potencia evaluando en qué topologías y con qué niveles de potencia permite abreviar sustancialmente los procedimientos convencionales, más demandantes de tiempo. El concepto de la multipuerta, que es inherente al mezclador, se podría extender a puertas virtuales a diferentes frecuencias y aplicarse a amplificadores de potencia, que ya no serían solo bipuertas no lineales