Departamento de Tecnología Electrónica Ingeniería de Sistemas y Automática

Tesis Doctoral

Corrección de Factor de Potencia basada en la estimación digital de la corriente de línea

Aplicación en el Convertidor Boost en modo de conducción continua

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2013

Escuela Técnica Superior de Ingenieros Industriales y de Telecomunicación

Universidad de Cantabria

Digital power factor correction based on line-current estimation

CCM Boost converter appplication

PhD Thesis

For obtaining the PhD degree

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2013

Escuela Técnica Superior de Ingenieros Industriales y de Telecomunicación

Universidad de Cantabria

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The undersigned hereby certify that they have read and recommend to the Escuela Técnica Superior de Ingenieros Industriales y de Telecomunicación for acceptance a thesis entitled **"Digital power factor correction based on line-current estimation"** by **Víctor Manuel López Martín** in partial fulfillment of the requirements for the degree of **PhD Thesis**.

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A mis padres, Marisa y Pedro

A Inés

Agradecimientos/Acknowledgements

En este documento se muestra una parte importante del trabajo realizado desde Octubre del año 2008, en el que comencé mi proyecto fin de carrera, y que desembocaría posteriormente en esta Tesis. Durante este tiempo han sido muchas personas las que me han ayudado y que merecen un agradecimiento especial:

Paco Azcondo, tutor de esta Tesis, que me ha mostrado su apoyo, confianza y paciencia; y que me ha sabido ilustrar y enseñar la luz siempre que me han surgido dudas.

A Charo, Christian y Javi por ayudarme siempre que lo he necesitado.

Alejandro, mi grandísimo amigo y compañero. Hemos compartido una cantidad ingente de horas juntos en el Laboratorio, con las que he disfrutado y aprendido cómo nunca habría imaginado. Una parte de esta Tesis es gracias a tí, ya lo sabes.

Regan Zane, many thanks for your support during my time with you in Boulder and Logan. All your comments have helped me to improve my knowledge about Power Electronics.

Mi familia, con mis padres a la cabeza, por ayudarme a llegar aquí sin ninguna preocupación más allá que mi propio trabajo.

Inés, tu apoyo y comprensión infinita desde el primer día han sido una bocanada de oxígeno en la consecución de esta Tesis. Todo lo que pueda decir es poco.

Y a mis amigos, que han entendido mis ausencias por las horas invertidas en esta Tesis.

Santander, Cantabria, Spain — Víctor Manuel López Martín

2013

Abstract

Continuous conduction mode (CCM) power factor correction (PFC) without input current measurement is a step forward with respect to previously proposed PFC digital controllers. Inductor volt-second (vs_L) measurement in each switching period enables the digital estimation of the input current, used in the inner current loop. However, an accurate compensation of the small inaccuracies in the measured vs_L is required in the estimation, to match the actual current. Otherwise, these errors are accumulated every switching period over the half line cycle, leading to an appreciable current distortion.

A vs_L estimation method is proposed in this Thesis, measuring the input (v_g) and the output voltage (v_o). Discontinuous conduction mode (DCM) occurs near input line zero crossings, and is also detected by measuring the drain-to-source MOSFET voltage, v_{ds}. Parasitic elements also cause a small difference between the estimated voltage across the inductor, based on input and output voltage measurements, and the actual one, which must be taken into account to estimate the input current in the proposed sensorless PFC digital controller.

This Thesis analyzes deeply the current estimation inaccuracies caused by errors in the ON-time estimation, voltage measurements, and the parasitic elements. A new digital feedback control with high resolution is also proposed to cancel the difference between DCM operation time of the real input current T^{g}_{DCM}, and the estimated DCM time T^{reb}_{DCM}. Therefore, the current estimation is calibrated using digital signals during operation in DCM.

A fast feedforward coarse time error compensation is carried out with the measured delay of the drive signal, and then a fine compensation is achieved with the feedback loop that matches the estimated and real DCM times. With this contribution, an universal controller is proposed. The digital controller can be used in universal applications due to the ability of the DCM time feedback loop to autotune based on the operation conditions (power level, input voltage, output voltage...), which improves the operation range in comparison with previous solutions.

Furthermore, an additional improvement is presented in this controller in which the current

demanded by the Sensorless PFC rectifier is pure sinusoidal despite the non-sinusoidal input voltage of the grid. This contribution is really interesting in applications where the harmonics limits are stricter (like in aircraft systems) and must be fulfilled independently on the voltage waveshape. This modification is totally done into the digital controller without any need of extra analog components.

Experimental results are shown for a 1 kW boost PFC converter over a wide power and voltage range. The digital controller is implemented in a *field programmable gate array* (FPGA) with a very simple analog circuitry to adapt the signals needed by the controller. The behavior of the controller, applied in lighting systems is also shown.

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Nomenclature

Abbreviations

AC	Alternating Current
ADC	Analog-to-digital conversion/converter
ASIC	Application-specific integrated circuit
CCM	Continuous Conduction Mode
CPLD	Complex Programmable Logic Device
CRM	Critical Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
EPE_g	Equivalent Parasitic Element in series with the input voltage
EPE_o	Equivalent Parasitic Element in series with the output voltage
FFT	Fast Fourier Transforms
FPGA	Field Programable Gate Array
HIL	Hardware in the loop
IC	Integrated Circuit
LSB	Least Significant Bit
OCC	One-cycle control
PCC	Point of common coupling
PF	Power Factor

PFC	Power factor correction/corrector	
PMBus	Power Managment Bus	
PWM	Pulse Width Modulation	
RMS	Root mean square	
SMPS	Switched Mode Power Supplies	
$THDi$	Total Harmonic Distornic of the input current	[%]
$THDv$	Total Harmonic Distortion of the voltage	[%]
VRM	Voltage regulation module	
ZCD	Zero-crossing detector	
ZOH	Zero-order-hold	

Greek Symbols

Δi_g	Real input current ripple	[A]
Δi_{reb}	Estimated input current ripple	[A]
$\triangle t$	Integration time	[s]
Δt_{off-on}	OFF-to-ON delay	[s]
$\triangle t_{on}^{meas}$	Duty cycle modification measurement	[s]
Δt_{on-off}	ON-to-OFF delay	[s]
Δt_{on}	ON-time modification	[s]
$\triangle v_o$	Output voltage ripple	[V]
Γ	Constant used in the denominator of the low bandwith model	[V/s]

Latin Symbols

C	Capacitor value	[F]
d	Duty Cycle command	
D_{max}	Duty cycle saturation	
$DCMi_g$	Detection signal of the DCM in i_g	
$DCMi_{reb}$	Detection signal of the DCM in i_{reb}	
e	Error generated due to the A/D conversion	[bit]
e_{DCM}	DCM time error	[s]
f_{ADC}	ADC sample frequency	[Hz]
f_c	Crossover frequency of the PFC voltage loop	[Hz]
f_{clk}	Clock frequency	[Hz]

f_{sw}	Switching frequency	[Hz]
f_u	Utility voltage frequency	[Hz]
i_{avg}	Average value of the estimated input current each switching period	[A]
I_D	RMS value of the diode current	[A]
i_{error}	Current estimation error	[A]
$i_{error,sim}$	Simulated current estimation error	[A]
I_g	RMS value of the real input current	[A]
i_g	Real input current	[A]
i_{g1}	Fundamental component of the input current	[A]
i_g^+	Peak input current	[A]
$\langle i_g \rangle$	Average input current	[A]
I_{gh}	RMS value of the current h^{th} component	[A]
I_{reb}	RMS value of the estimated/rebuilt input current	[A]
i_{reb}	Rebuilt input current	[A], [bit]
$i_{reb}[j,k]$	Estimated current in the clock period k in the switching cycle j	[A]
i_{reb}^-	Valley value of the rebuilt current	[A]
i_{ref}	Current reference	[A]
i_L	Inductor current	[A]
j	j^{th} switching period	
k	k^{th} clock period	
L	Inductance	[H]
L_{est}	Estimated inductance	[H]
L_r	Parasitic series inductance in the current sensor	[H]
M	Voltage conversion ratio	
n_{clk}	Clock-cycles per switching-period	
n_u	Switching cycles per half-line period	
$Nbits$	Number of bits in the ADCs	
$on-off$	Control signal	
P_{cond}	Total conduction losses	[W]
P_D	Conduction losses in the power diode	[W]
P_g	Input power	[W]
P_L	Conduction losses in the inductor	[W]
P_{loss}	Total converter losses	[W]
P_Q	Conduction losses in the MOSFET	[W]
P_S	Conduction losses in the current sensor	[W]

P_{sw}	Total switching losses	[W]
q	LSB resolution defined by the designer	[V/bit]
q_g	LSB resolution of the input voltage	[V/bit]
q_i	LSB resolution of the current	[A/bit]
q_o	LSB resolution of the output voltage	[V/bit]
Q_{rr}	Reverse recovery charge	[C]
R	Load resistance	[Ω]
R_D	Diode ON-state resistor	[Ω]
R_e	Emulated Resistance	[Ω]
R_L	Parasitic resistance of the inductor	[Ω]
R_{on}	Power MOSFET ON-resistor	[Ω]
R_s	Sense resistor	[Ω]
R_e^*	Digital emulated resistance	[Ω]
T_{clk}	Clock period	[s]
t_{on}	Main switch ON-time	[s]
t_{on}^*	Estimated ON-time in the digital controller	[s]
T_s	Sampling period of the PFC voltage loop	[s]
T_{sw}	Switching period	[s]
T_u	Utility voltage period	[s]
T_{DCM}^g	DCM time of the real input current	[s]
T_{DCM}^{reb}	DCM time of the estimated input current	[s]
V_β	Voltage across the EPE_o	[V]
V_{bus}	DC bus voltage	[V]
V_D	Diode forward voltage at zero-current	[V]
v_{dig}	Variable control to compensate current estimation error	[bit]
v_{ds}	MOSFET drain-to-source voltage	[V]
v_{ds}^*	Digital drain-to-source voltage	[bit]
V_g	RMS value of the input voltage	[V]
v_g	Input voltage	[V]
v_{g1}	Fundamental component of the input voltage	[V]
v_g^*	Digital input voltage value	[bit]
v_g^s	Sampled input voltage	[V]
v_{gs}	MOSFET drive signal	[V]
v_L	Inductor voltage	[V]
v_L^*	Digitally estimated inductor voltage	[bit]

$v_{L,reb}$	Rebuilt inductor voltage	[V]
V_m	Carrier signal amplitude	[V]
v_m	Carrier signal	[V]
v_{max}	High-level voltage of the digital device	[V]
V_o	Average output voltage	[V]
v_o	Output voltage	[V]
v_o^*	Digital output voltage value	[bit]
v_o^s	Sampled ouput voltage	[V]
v_{par}	Voltage drop accross the parasitic elements	[V]
V_{ref}	Reference voltage level	[V]
v_{xg}	Instantaneous EPE voltage when this is in series with L	[V]
v_{xo}	Instantaneous EPE voltage when this is in series with v_o	[V]
vs_L	Volt-seconds in the inductance	[V · s]

Capítulo 0

Introducción

La red eléctrica transmite y distribuye la potencia a una frecuencia constante (50 Hz - 60 Hz) y a una tensión alterna (AC). Sin embargo, la mayoría de los aparatos eléctricos y electrónicos necesitan fuentes de alimentación de corriente continua (DC). Por tanto, se necesita una conversión de potencia de AC a DC como primera etapa para la conexión a la red eléctrica. Un rectificador es un convertidor electrónico diseñado y construido para la conversión de AC a DC, entregando potencia en DC a una o varias cargas, pero todas ellas conectadas a la misma línea de DC.

Rectificadores sin ningun tipo de control, como el rectificador de media onda o el de onda completa, seguidos por un gran condensador (que almacene la energía), han sido durante muchos años las soluciones empleadas para conseguir tensión en DC y alimentar la carga, sucesivas etapas DC-DC o un regulador lineal. Pero el valor del factor de potencia (PF) en este tipo de rectificadores es muy bajo, y con un contenido armónico en la corriente muy elevado. Este factor de potencia aumenta si se introducen fuentes de alimentación controladas (convertidores DC-DC conmutados que controlan la corriente demandada por la red) entre el rectificador y el condensador de salida, haciendo que el sistema sea un rectificador activo con corrección de factor de potencia.

Una corriente de línea con un alto contenido armónico tiene efectos perjudiciales para la red electrica, como:

- Valores eficaces mayores para el valor de potencia demandada, limitando los valores de potencia activa a entregar a la carga para una determinada sección de cable.
- Aumento de las corrientes por el neutro en sistemas trifásicos, provocando inestabilidades y distorsión en la tensión.

Mientras la mayoría de la energia eléctrica consumida viene por el uso de motores eléctricos,

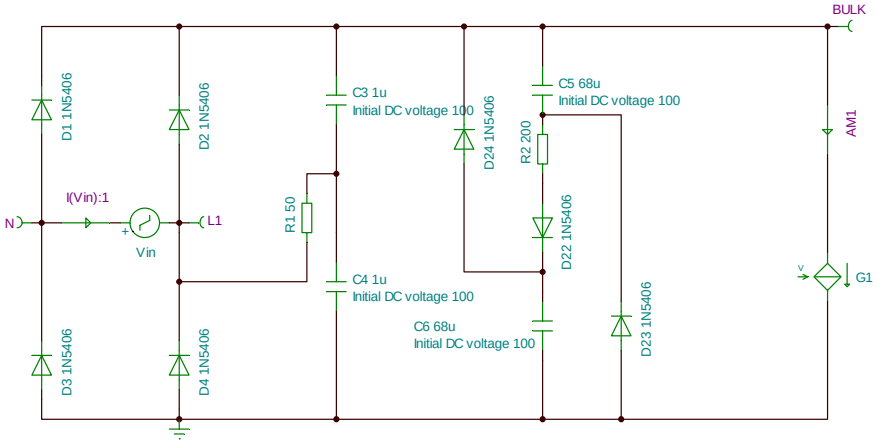


Figura 1: Circuito *Valley-fill*.

hornos, iluminación ..., la cantidad de energía que representan estos equipos electronicos ha aumentado de manera considerable, afectando a la red eléctrica por su característica no lineal.

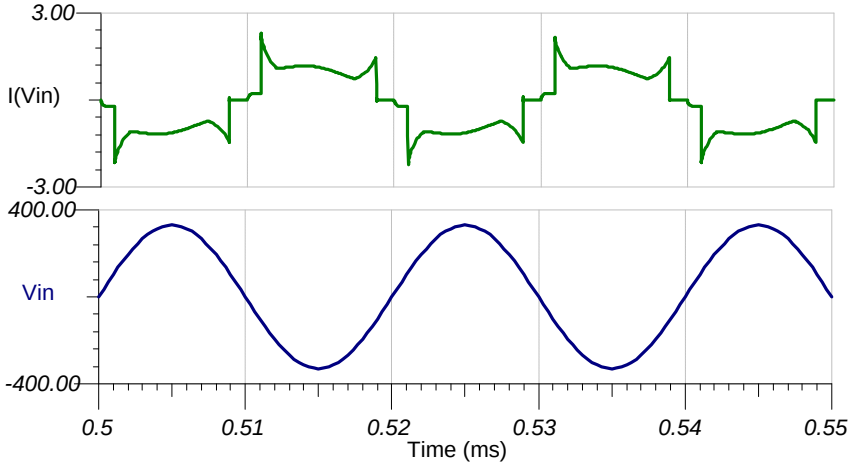
Para mantener una calidad en la energia eléctrica y mitigar estos efectos negativos, diferentes normativas internacionales como la EN 61000-3-2 [1] definen lo límites admisibles de armónicos de corriente inyectados a la red eléctrica para diferentes tipos de cargas.

El valor del factor de potencia es un dato que describe la "calidad" de una carga desde el punto de vista de la red eléctrica. Un factor de potencia alto indica un comportamiento resistivo desde el punto de vista de la red, con una corriente en fase y proporcional a la tensión de línea. Cargas con un factor de potenica bajo, poseen un contenido armónico en su corriente muy alto y/o un desfase entre la tensión de línea y la corriente.

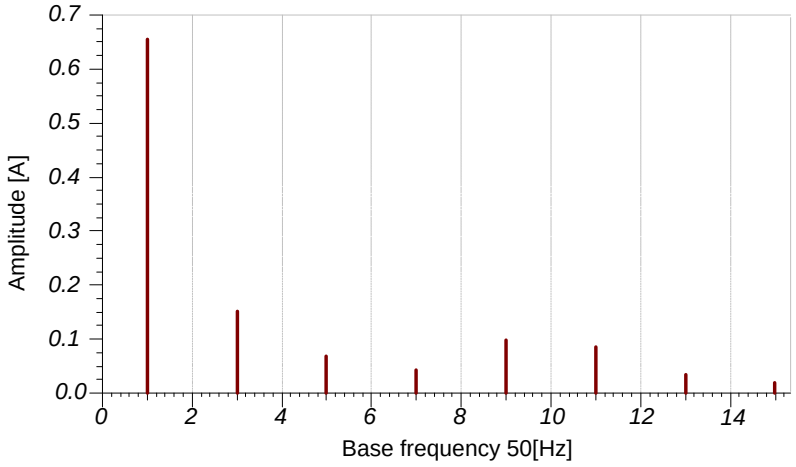
Soluciones pasivas utilizando filtros o circuitos *Valley-fill* [2, 3] consiguen buenos factores de potencia a cargas constantes y en condiciones de diseño. En la Fig. 1 se muestra el circuito *Valley-fill*, mientras que las formas de onda de tensión y de corriente se presentan en la Fig. 2a. En lo que se refiere a la corriente de entrada, su contenido armónico se muestra en la Fig. 2b.

Dentro de los rectificadores activos de corrección de factor de potencia (*PFC rectifiers*), el convertidor Boost y el Flyback son, probablemente, las soluciones más utilizadas. Para bajas potencias, el convertidor Flyback trabajando en modo de conducción discontinua (DCM - *Discontinuous conduction mode*) tiene un comportamiento resistivo de modo natural, sin necesidad de un control de corriente, si su frecuencia de conmutación (f_{sw}) y tiempo de ON (t_{on}) son constantes, tal y como se muestra en la Fig. 3, donde i_g^+, i_g, $\langle i_g \rangle$ son los valores de pico, instanténeo y medio en cada periodo de conmutación de la corriente de entrada, respectivamente. En comparación con el Buck-Boost (su alternativa sin aislamiento) el convertidor Flyback proporciona aislamiento a su salida y evita los problemas debido a la polaridad inversa de la tensión de salida del Buck-Boost.

El convertidor Boost también presenta esta propiedad de "emulador" natural de resistencia operando en el límite entre modo de conducción continua y discontinua (CRM - *Critical*



(a)



(b)

Figura 2: (a) Formas de onda del circuito *Valley-fill*. Arriba: Corriente de entrada. Abajo: Tensión de entrada. (b) Contenido armónico de la corriente de línea.

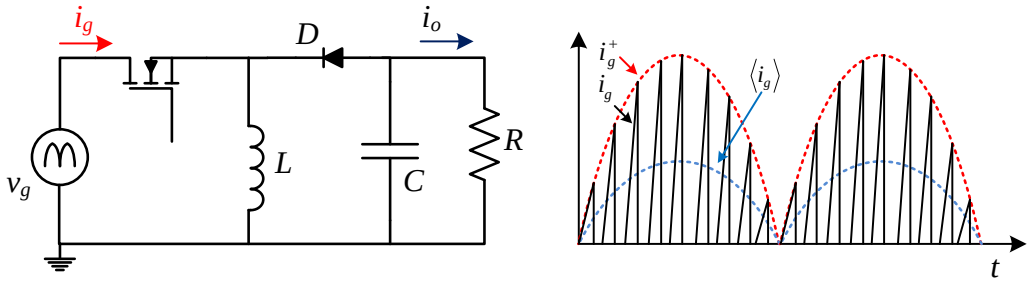


Figura 3: Convertidor Buck-boost trabajandor como resistencia en modo natural.

Conduction Mode) con tiempo de ON constante y a una frecuencia de conmutación variable, aunque este aspecto hace que el filtro EMI necesario en la entrada sea más complejo y costoso. Circuitos integrados como el L6560 [4] permiten una realización analógica de este control de una manera sencilla.

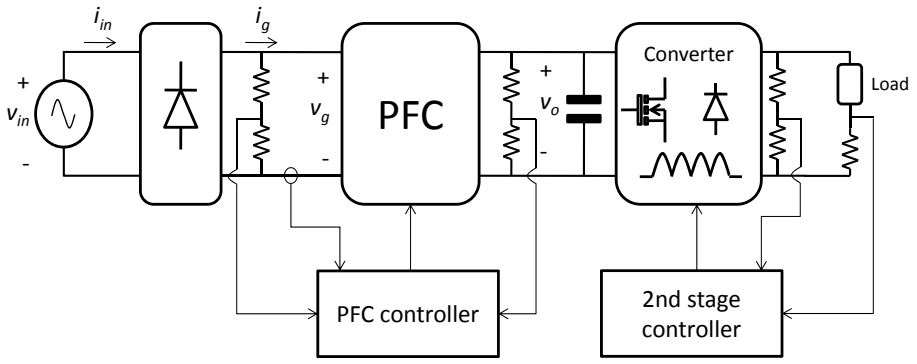
En aplicaciones de alta potencia (por encima de 250 W) se prefiere la operación en modo de conducción continua (CCM) o la operación de etapas en paralelo en DCM y en "*interleaving*". En CCM se emplean dos lazos de control: un lazo interno de ancho de banda amplio (alrededor de 1-5 kHz) que da forma a la corriente demandada de la red eléctrica; y un segundo lazo lento, de unidades de Hz de ancho de banda, que regula la tensión de salida empleando como variable de control la amplitud de la intensidad de entrada. En este caso, el convertidor Boost es el convertidor más empleado, debido a su alta eficiencia (la corriente que circula por sus dispositivos semiconductores es la menor comparada con otros convertidores), y su baja emisión de ruido comparado con los diferentes tipos de convertidores.

Para resolver este doble lazo de control se pueden encontrar en el mercado circuitos integrados con tecnología analógica, como el UC3854 [5], que es uno de los más usado para corrección de factor de porencia. Existen técnicas de control no lineales, como "*Nonlineal-carrier (NLC)*" o el control "*One-Cycle*". Un dispositivo analógico que realiza este tipo de control es el IR1150 [6]. Estos circuitos que se caracterizan por su simplicidad y mejora de la respuesta dinámica del lazo de corriente, comparada con la solución tradicional de doble lazo. Pero a pesar de esta disponibilidad de controladores de corrección de factor de potencia comerciales, las normativas y los programas de certificación de fuentes de alimentación cada vez más estrictos, y la busqueda de precios más competitivos ha hecho que diversos grupos de investigación empleen sus esfuerzos es este tema.

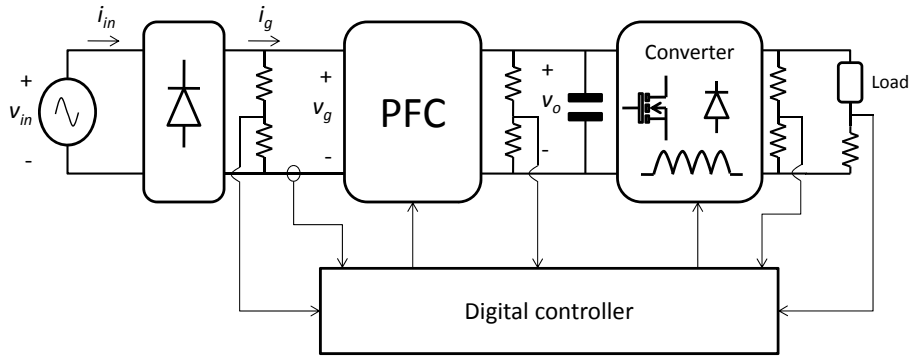
Una parte importante de estos esfuerzos están orientados hacia el desarrollo de técnicas de control digital. Aunque se han presentado gran cantidad de soluciones, sólo unas pocas han podido entrar en el mercado con éxito. En lo que se refiere a la corrección de factor de potencia, los requisitos de dinámica en los controladores no son especialmente elevados, haciendo que la corrección de factor de potencia sea un ambito en el que se han presentado numerosas técnicas digitales de control.

El control de convertidores de potencia mediante dispositivos digitales permite incluir funciones complejas para adaptarse a las diferentes situaciones de la tensión alimentación y de la carga. Algunas de las ventajas son generales para cualquier aplicación; como la programabilidad, reducción del número de componentes, menor sensibilidad al ruido o tolerancias de componentes, y más recientemente en aplicaciones de potencia, la compatibilidad con estándares como el PMBus [7–9] para la gestión de potencia.

En aplicaciones de corrección del factor de potencia (PFC) en las que no existe interacción con otras etapas, el control analógico prevalece, ya que obtiene, en principio, mejor compromiso entre prestaciones y coste. Pero incluso en este caso, es habitual encontrar que las etapas posteriores, alimentadas por el PFC, dispongan de un control realizado en un dispositivo digital donde sería susceptible de ser integrado un control digital del PFC, simplificando el



(a)



(b)

Figura 4: Esquemas de sistemas de alimentación: (a) Esquema tradicional con etapa PFC con control analógico y dispositivo digital controlando el convertidor posterior. (b) Integración digital completa del control de las dos etapas

diseño final (ver Fig. 4).

El uso de controles de digitales permite, por ejemplo, reducir la variación en el rendimiento debido al envejecimiento, temperatura u otro tipo de factores mediambientales, la posibilidad de diseñar controles adaptativos, o reducir el el tamaño en comparación con una materialización analógica.

Además, el uso de plataformas de desarrollo como microprocesadores, FPGAs, CPLDs, PICs..., permite añadir funciones adicionales de control sin un coste extra excesivo, ya que los cambios se realizan interiormente en el dispositivo digital sin necesidad de introducir elementos analógicos extra.

La regulación de la corriente de entrada al PFC operando en CCM para hacerla sinusoidal, proporcional a la tensión de entrada, se realiza generalmente a partir de un sensor de corriente. Las capacidades del PFC son sensibles a las prestaciones de este sensor que origina ruido y disipación de potencia. La traducción directa de los controladores lineales empleados en controladores analógicos, como el UC3854 [5], en controladores digitales requiere una solución como la que se muestra en la Fig. 5, donde R_s representa el valor de la resistencia de sensado. Se necesitan tres medidas, la tensiónes de entrada (v_g) y de salida (v_o), y la corriente de entrada (i_g).

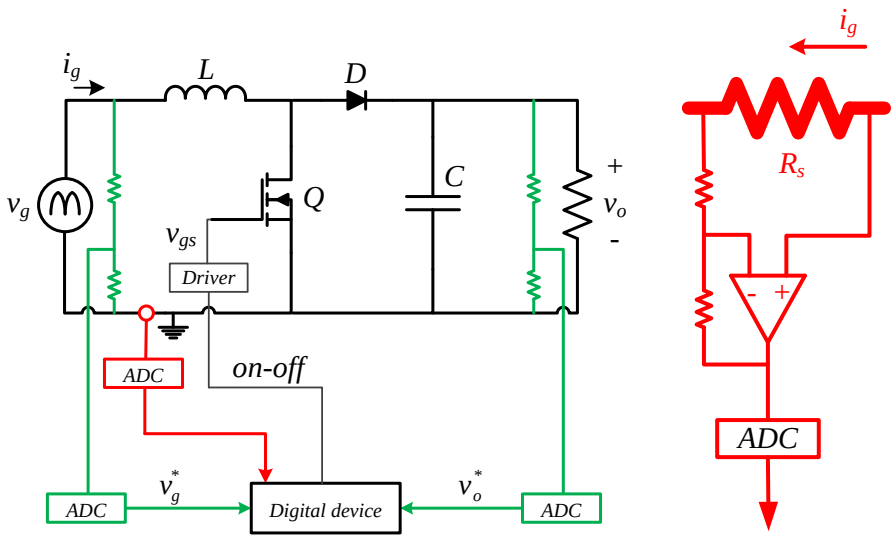


Figura 5: Esquema típico de rectificador PFC con control digital y circuito de sensado de corriente.

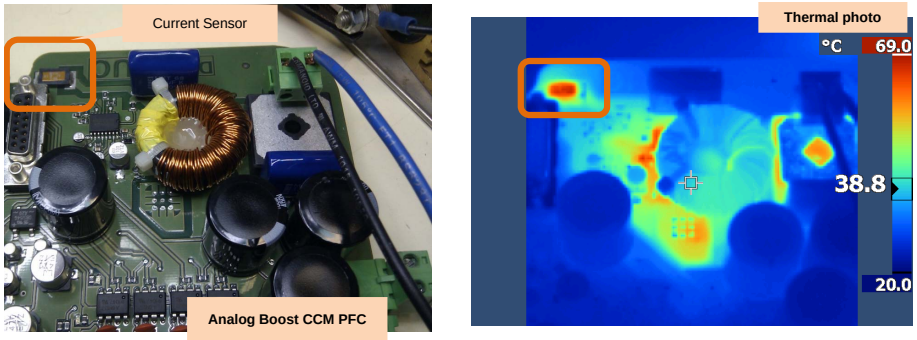


Figura 6: Izq: Imagen de un convertidor Boost PFC con control analógico, usando el controlador comercial UC3854 de Unitrode. Der: Foto térmica del convertidor trabajando a plena carga.

De estas tres variables, la medida de la corriente es la que presenta una mayor complejidad, necesitando un circuito de adaptación de señal como el que se presenta en la Fig. 5. Por ello, varios autores y grupos de investigación han prestado atención en este tema [10–14]. La resistencia de sensado (R_s) es la solución más empleada para la medida de la corriente, y la potencia disiparda por ella (que será mayor a medida que aumenta la corriente demandada) da lugar a un punto caliente en la placa de circuito impreso. La Fig. 6 muestra una placa de un Boost PFC analógico controlado con el UC3854, que trabajando a plena carga (1 kW) genera una zona de alta temperatura como el que se muestra en la foto térmica de dicha figura.

Las tensiónes de entrada y de salida (v_g y v_o), tienen una dinámica lenta (50-60 Hz y 100-120 Hz) y su conversión analógico-digital no requiere de unas prestaciones muy elevadas. Es necesario un circuito de adaptación de señal tras el sensor de corriente para que la señal sea adecuada como entrada al convertidor analógico-digital (ADC), y además, dicho convertidor tiene que poseer un ancho de banda mucho mayor que los ADCs empleados en las tensiones.

En el presente trabajo, se busca una solución digital de bajo coste, pero capaz de alcanzar las especificaciones de la norma EN-61000-3-2 clase C para unas condiciones de tensiones y frecuencias universales, y un amplio intervalo de carga. Para ello, se propone sustituir la medida de corriente de entrada en el PFC (i_g), por su estimación digital (i_{reb}), partiendo de los datos digitales de tensión de entrada y salida. La naturaleza de dinámica lenta de estas tensiones hace que se pueden obtener a través de convertidores analógico-digitales de prestaciones más bajas a las que se necesitan en la medida de corriente. Las señales de mando del convertidor se generan de forma que la corriente estimada resulte proporcional a la tensión de entrada (sinusoidal), utilizando una técnica de control no-lineal [15–18] aplicado a la corriente reconstruida. En resumen, en todos aquellos lazos de control en los que tradicionalmente se emplea la variable i_g, en este trabajo se sustituya la variable i_{reb}.

Para realizar estas funciones se emplea un dispositivo digital configurable concurrente, *field programable gate array* (FPGA), donde se ha implementado el control. Los resultados experimentales se presentan para un Boost PFC del 1kW.

En el capítulo 2 de este trabajo se realiza una breve revision de corrección de factor de potencia y normativas vigentes referentes que definen los límites de armónicos de corriente inyectados a la red eléctrica, seguido por una muestra del estado del arte del control digital en fuentes conmutadas de alimentación, y en especial de etapas correctoras de factor de potencia. Se hace un especial énfasis en la técnicas de sensado de corriente en fuentes conmutadas, y una breve revisión de los últimos trabajos de sensado de corriente en rectificadores activos con corrección de factor de potencia.

El concepto de estimación digital de la corriente empleado en este trabajo se analiza en el Capítulo 3, junto con el algoritmo de corrección de factor de potencia empleado, y los errores de estimación de corriente que afectan a este tipo propuesta sin medida de la corriente. Cada fuente de error es analizada por separado, obteniendo las expresiones que modelan ese error. El Capítulo 4 presenta el error de estimación de corriente debido a los elementos parásitos internos del convertidor de potencia. Este tipo de errores se presentan por separado porque no dependen de la resolución de la conversión analógico-digital de las variables, si no que es inherente al convertidor, y depende del punto de trabajo.

La implementación digital del control se muestra en el Capítulo 5, junto con la compensación digital de cada uno de las fuentes de error enunciadas. Se muestra la influencia de la resolución, y como se puede obtener una compensación de alta resolución sin necesidad de elementos analógicos extra. Dicha compensación de alta resolución se realiza proponiendo un nuevo lazo de realimentación. En el Capítulo 6 se realiza un modelado AC en pequeña señal del sistema a regular, para analizar la estabilidad del sistema. Por su parte, en el Apéndice A se muestra la relación que existe entre los valores eficaces de la corriente de entrada y la real en caso de que la estimación de corriente no sea correcta. Este aspecto es necesario para la obtención del modelo de la planta que corrige el error de estimación de corriente con alta resolución.

En el Capítulo 7 se propone un nuevo control digital de la corriente demandada de la red

eléctrica, para que ésta sea sinusoidal pura independientemente de la forma de onda de la tensión de la red eléctrica. Aplicaciones críticas como aviónica, presentan unos requerimientos de armónicos de corriente que, ante una tensión de red distorsionada, los controladores de PFC tradicionales no son capaces de cumplir. Este nuevo control busca eliminar este problema.

La validación experimental de la aportación presentada en esta Tesis se muestra en el Capítulo 8 para unas condiciones de trabajo universales de tensión y frecuencia de entrada (85 - 250 Vrms y 50 - 800 Hz), para las cuales el controlador digital no ha sido reprogramado. Por su parte, en el Capítulo 9 se muestra un ejemplo de aplicacion industrial del trabajo presentado en esta Tesis, donde se utiliza como etapa PFC para balastos de lámparas de alta intensidad de descarga. Además, se introduce una modificación en el lazo de control para evitar parpadeos en la lámpara debido a fluctuaciones de baja frecuencia en la red eléctrica.

Las conclusiones obtenidas tras la realización de esta Tesis, y las futuras líneas de trabajo se recogen en el Capítulo 10. Todas las publicaciones realizadas a partir de este trabajo se muestran en el Capítulo 11.

Chapter 1

Introduction

Utility systems transmit and distribute power at constant frequency (50-60 Hz) and AC voltage. Nonetheless, most of the electrical and electronics applications require DC power supplies. Therefore, an AC to DC power conversion is needed as front-end stage. A rectifier is a power electronics interface built for converting AC power to DC power, and may supply DC power to different electrical loads, all of them connected to the same DC bus.

Uncontrolled rectifiers, either half-wave or full-wave, followed by a large energy storage capacitor were traditionally used to perform the necessary AC rectification, and supply a DC output to a load, downstream DC-DC converter or linear regulator. The power factor (PF) of such rectifiers is low with a high harmonic content in the AC line current. Placing a controllable switched-mode converter between the rectifying elements and the large energy storage capacitor of the uncontrolled rectifier results in the configuration of a power factor corrector (PFC) rectifier.

High harmonic input current content has undesirable effects:

- Increased RMS line currents, limiting the power available to an AC load for a given AC service wire gauge
- Increased neutral currents in 3-phase systems. Possible AC system instability and line voltage distortion.

The global growth of the electronics has led to the great increment in the use of electronics devices or gadgets. Although the most of the energy is consumed by electrical motors, furnaces or lighting; the amount of energy consumed by these electronic equipment has increased considerably, affecting the power grid due to its non-linear characteristic.

To maintain the quality of the AC line and mitigate these negative effects, international standards such as EN 61000-3-2 [1] set the current harmonics magnitudes of many ubiquitous

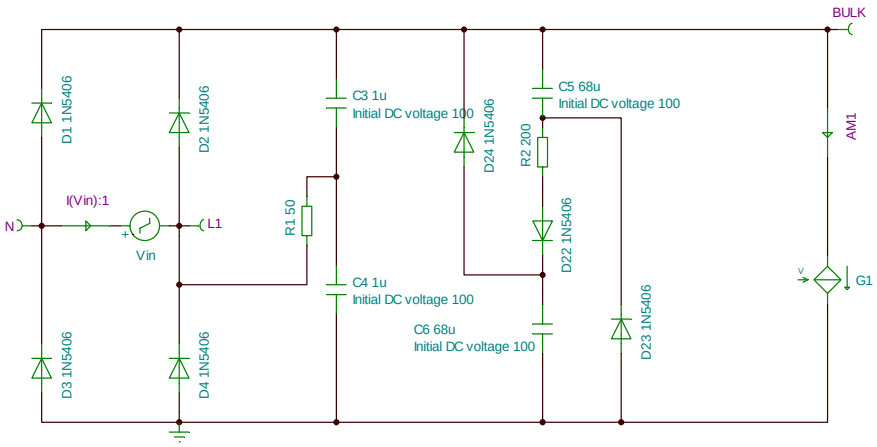


Figure 1.1: Valley-fill circuit.

electronic devices. Power factor describes the qualities of a load in a AC power system. Loads with a high power factor appear largely resistive to the AC utility mains as the demanded current is in-phase and proportional to the line voltage. Systems with a low power factor have phase-displaced line voltage and current, non-proportionality between line voltage and line current resulting from high harmonic current content of the line current, or both phase displacement and high harmonic current content combined.

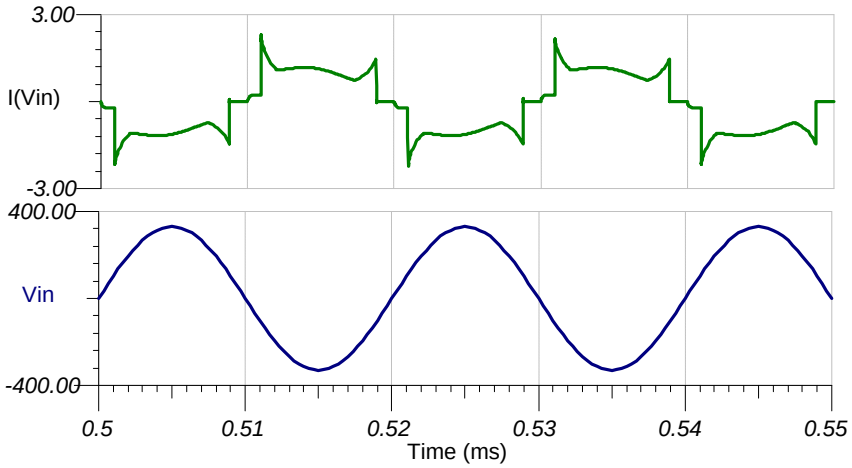
Passive approaches using filters or Valley-fill [2,3] topologies have a good behavior at constant load and around nominal conditions. Figure 1.1 shows the Valley-fill circuit scheme. The voltage and current waveforms are presented in Fig. 1.2a, in which the input current has an current harmonic content shown in Fig. 1.2b.

Among the active switch mode PFC rectifiers, Boost or Flyback topologies are more popular due to their good current shaping ability for the entire line period.

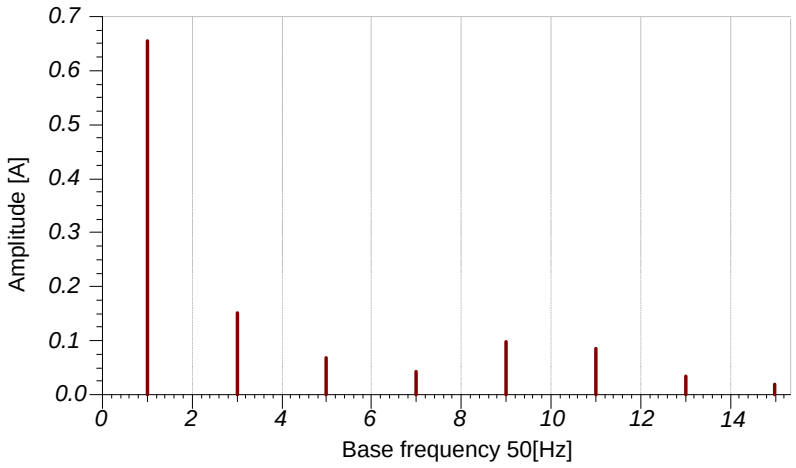
In general, boost PFC rectifiers have higher conversion efficiency than Buck-Boost PFC rectifiers, which makes boost topology the most popular structure for PFC rectifiers. For low power applications, Flyback converter working in the discontinuous conduction mode (DCM) presents averaged resistive emulator behavior at a constant switching frequency (f_{sw}) and ON-time (t_{on}) as is presented in Fig. 1.3, where i_g^+, i_g, $\langle i_g \rangle$ represent the peak, instantaneous and average value in each switching cycle of the input current, respectively. No current loop is needed. In comparison with the Buck-Boost converter, Flyback converter offers isolation and avoids problems due to the inverse polarity in the Buck-Boost output.

Boost converter shows resistive emulator behavior at the boundary between CCM and DCM (Critical Conduction Mode - CRM) with a constant ON-time and a variable switching frequency. This aspect makes necessary a EMI filter in the input, increasing the cost and complexity of the power supply. Integrated circuits (ICs) as the L6560 [4] enable an analog implementation of this control in an easy way.

For higher power applications (more than 250 W), the continuous conduction mode (CCM) is preferred, or several DCM stages in parallel and interleaved operation. In CCM two control



(a)



(b)

Figure 1.2: (a) Valley-fill waveforms. Upper trace: Input current. Lower trace: Input voltage. (b) Harmonics of the line current.

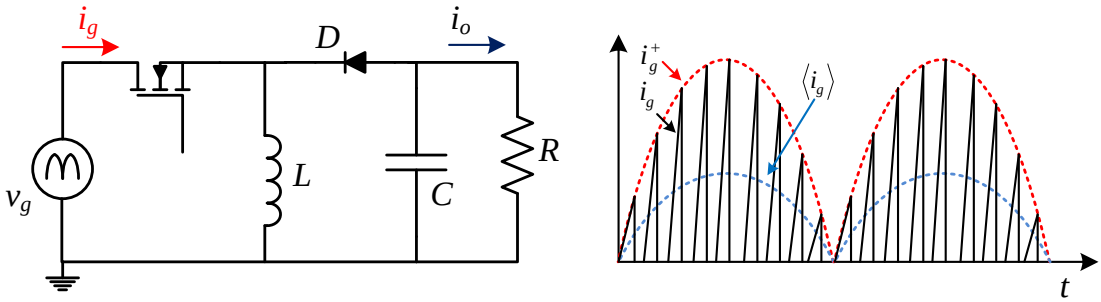


Figure 1.3: Buck-boost converter working as a PFC rectifier.

loops are typically needed: a high frequency inner loop (around 1-5 kHz) whose goal is to obtain a sinusoidal current shape using a sinusoidal reference (obtained with the input voltage waveform), and a second low bandwidth voltage loop (around 10 Hz) that regulates the output voltage using the input current amplitude as control variable. In this case, Boost converter is the most popular due to its efficiency (the current through the semiconductor devices is lower in comparison with other topologies), and low noise.

Several commercial analog integrated circuits (ICs) are available to solve this two loops, as the UC3854 [5], widely used in power factor correction. Nonlinear controllers as the "*Nonlinear-carrier*" (NLC)" control or the "*One-Cycle*" control are famous due to its simplicity and improve the bandwidth of the current loop in comparison with the traditional approach. An analog device for this type of control approaches is the IR1150 [6]. But while these (and more) commercial ICs are available, the stricter standards and certification program requirements as well as the pressure on achieving higher competitive cost, have motivate the research in this topic.

The digital control in power converters enables the implementation and design of complex control algorithms to adapt the behavior of the power supply according to the demanded power and input voltage. There is no doubt about the interest in using digital control for switched mode power supplies (SMPS). Due to that, an important part of the efforts are focused in digital control techniques. However, only few designs have enjoyed widespread market use and success. Talking about power factor correction, the relatively low dynamic requirements of the controller, along with the increasing use of PFCs as front-end stages, provides a promising outlook for the appropriate application of digital control techniques in PFC rectifiers.

Some of the advantages are valid for any application, for example programmability, with decreased number of components, less sensitivity to changes or noise, reduced design time and, more recently, additional power management capabilities, such as Power Management Bus, PMBus, compatibility or electromagnetic interference (EMI) reduction [7–9]. In PFC applications without interaction with other stage, the use of analog controllers is the most common solution due to its agreement between performance and cost. But it is usual to find second stages, supplied by the PFC stage, with a digital controller in with the PFC digital control can be implemented, simplifying the final design (see Fig. 1.4).

The benefits of a digital implementation of the controller prevent performance variation due to age, temperature and other type of environmental factors, the ability to easily implement adaptive control structures and possibly a reduction in the controller cost and die/package size when compared to an analog controller. A digital controller designed and implemented using a flexible digital device like a Complex Programmable Logic Device (CPLD), a Microprocessor or a Field Programmable Gate Array (FPGA), enables the inclusion of additional or auxiliary control features without an extra cost, because the extra features are programmed into the device without need of extra discrete analog components.

The control of the input current in a PFC converter has the goal of obtaining a sinusoidal

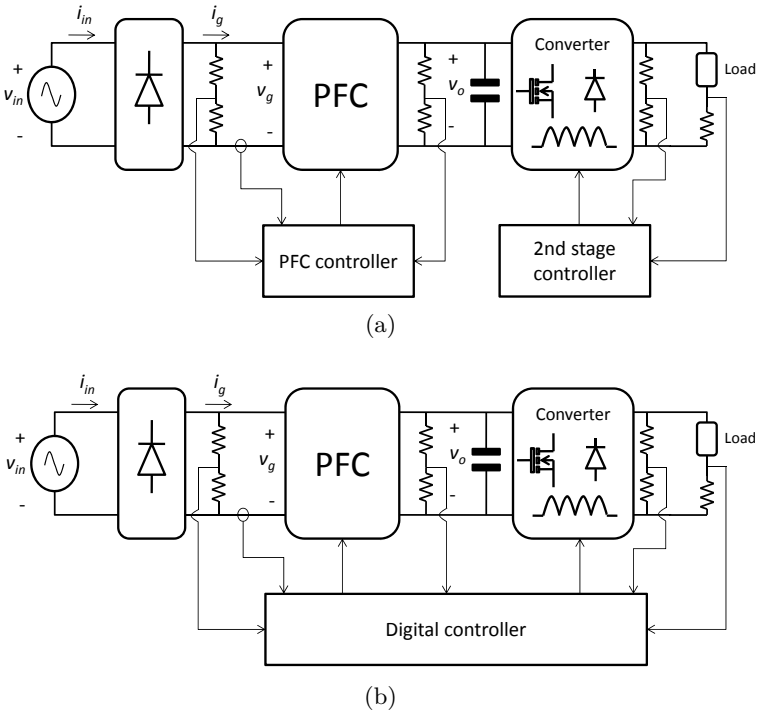


Figure 1.4: Switched mode power supply scheme. (a) Traditional approach with a PFC stage with analog control and a digital device for the second stage. (b) Complete digital implementation of the two stages control.

current (proportional to the input voltage), and is commonly done with a current sensor when working in the CCM. The PFC converter performances are sensitive to the sensor behavior, originating noise and power losses. A discretization of these traditional linear controllers used in analog ICs, and its implementation in a digital device requires a solution as the depicted in Fig. 1.5, where R_s represents the value of the resistor used as current sensor. Three measurements are needed, the input (v_g) and output (v_o) voltages, and the input current (i_g).[1]

Sensing the input current is more complex in comparison with the voltage sensing, because a circuitry to adapt the signal, as the presented in Fig. 1.5, in needed. Due to that, several authors and research groups have paid attention to this aspect [10–14], focused on obtaining cost effective solutions without losing performance to measure and digitize the current. A resistive sensor (R_s) is the most common practice, but it generates power losses (the higher is the current, the higher are the power losses) and a hot spot in the printed circuit board. Figure 1.6 shows a picture of a Boost PFC stage controlled by the UC3854 IC, that has a thermal picture as the presented in the right side of the figure.

The low dynamic behavior of the input and output voltage (v_g and v_o) whose frequencies are the same as the line frequencies (50 - 60 Hz and 100-120 Hz) and its analog-to-digital conversion do not need high performance requirements. However, the input current frequency

[1] Although v_g and i_g represent the rectified signals of v_{in} and i_{in}, both symbols are used to indifferently represent the input voltage and current, respectively.

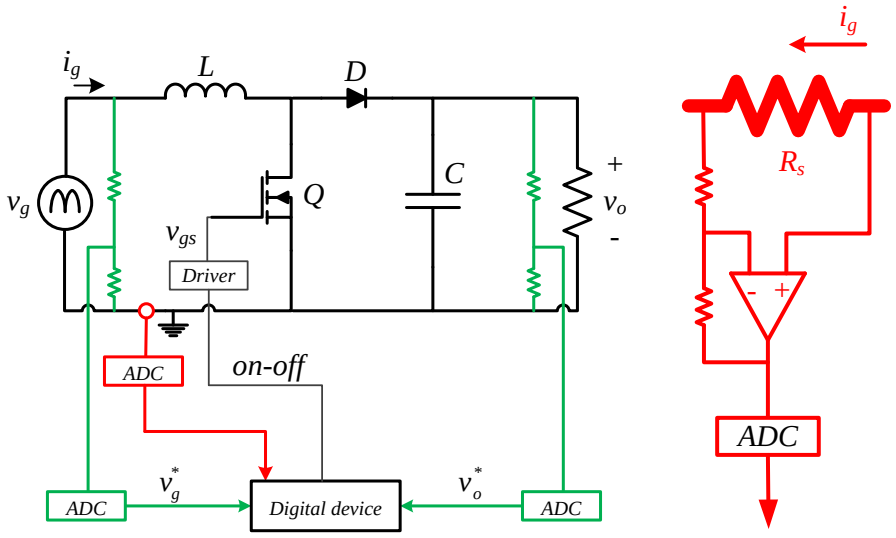


Figure 1.5: Typical scheme of a digitally controlled PFC converter with the current sensor circuit.

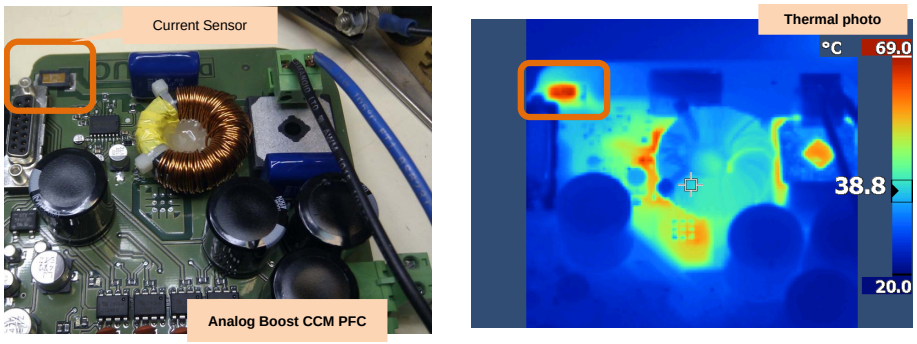


Figure 1.6: Left: Picture of a PFC Boost analog converter controlled by the UC3854 of Unitrode. Right: Thermal picture of the converter at nominal power.

is equal to the switching frequency, so high sampling frequency is needed in the current analog-to-digital conversion, increasing the cost in comparison with the voltage analog-to-digital conversion.

This dissertation introduces a digital PFC cost-effective controller able to fulfill the requirements defined by the EN-61000-3-2 standard for Class C equipment (the most restrictive) over a universal input voltage and frequencies values, for a wide power range. The current measurement is substituted by its digital estimation, from the input and output voltage data and the model of the converter, implemented in the digital device. The drive signal is generated to obtain a sinusoidal estimated current using a nonlinear technique [15–18] applied to the estimated input current. A Field Programmable Gate Array (FPGA) is used for the power stage emulation and the control algorithms implementation, and the experimental results are obtained in a 1 kW Boost PFC prototype.

Chapter 2 provides a review of harmonic current power factor standards related to single-phase PFC rectifiers, followed by a brief background of the digital control in Switched Mode Power Supplies (SMPS), specially for power factor correction stages. The different techniques for current sensing in SMPS are addressed, and a brief introduction of the last works about current sensing techniques in PFCs.

The digital rebuilding concept used in this work is shown in Chapter 3, together with the used PFC control technique and the current estimation error that affect this sensorless approach. Each cause of error is analyzed in detail and modeled. Chapter 4 presents the current estimation error due to the influence of the parasitic elements. This error is analyzed separately because it does not depend on the resolution of the analog-to-digital conversion, it is inherited to the converter and depends on the operating point.

The digital implementation of the control approach is shown in Chapter 5. The digital compensation of the different causes of error is presented in this Chapter, with the influence of the resolutions and how is possible to have a high resolution compensation without analog extra components. In Chapter 6 a small-signal AC model of the system is derived, so as to analyze its stability. Appendix A shows the relation between the RMS values of the real and estimated current when a current estimation error exists. This aspect is important to obtain the model of the plant that enables the estimation error compensation with high resolution.

Chapter 7 proposes a new current control for front-end stages, with the aim of demanding a pure sinusoidal current independently on the line voltage waveform. Critical applications like airborne systems have a very strict requirements in terms of current harmonics that, under distorted voltages can not be fulfilled by traditional PFC controllers. This new approach tries to solve this problem.

An experimental validation of the contributions presented in this Thesis is shown in Chapter 8 under universal input voltage range (85 - 250 V_{rms} and 50 - 800 Hz), in which the digital controllers does not need to be reprogrammed. In Chapter 9 it is shown an industry application of this controller in which the PFC rectifiers is used as front-end stage in electronic

ballast for HID lamps. Furthermore, an additional capability is introduced to avoid flickering in the lamp light, rejecting low frequency fluctuations in the grid voltage.

A summary of the contributions and conclusions of this work are presented in Chapter 10, the publications that include the contributions of this Thesis are enumerated in Chapter 11, which concludes this document.

Chapter 2

Background

This chapter provides a brief introduction to the existing controllers for boost power factor correction (PFC) rectifiers and describes the motivation for the research presented in this Thesis. First, basic principles of power factor correction and current harmonics are described; followed by an review of the benefits that digital control offers in switched mode power supplies (SMPS). After that, the basics of the Boost converter are presented, with the most popular analog, and recent digital, boost PFC controllers. Then, current sensing techniques in SMPS and the problems of current sensing are commented, with the different alternatives or solutions presented by many authors in order to avoid the current measurement. The motivations of this research on circuit simplicity and universal behavior are addressed at the end of this Chapter.

2.1 Power factor correction

Traditionally, Power Factor (PF) is defined as the ratio between the real power transmitted to the load and the apparent power taken from the source/utility, being a measurement of the energy conversion efficiency. The loads can be reactive and/or nonlinear. Reactive loads (or components of the load impedance) cause a phase shift between the input voltage and the input current. Universal AC-DC power supplies of electronic systems should be designed to accept any level of utility voltage used in the world. Due to that, it is common to find application notes of PFC controllers whose input voltage range is 85 to 265 V_{rms} [19], at different frequencies, such as 60 Hz (typical in USA), 50 Hz (typical in Europe), or even 360-800 Hz (airborne systems). The expression that defines the PF values is:

$$PF = \frac{Real\ power\ \ [W]}{Apparent\ power\ \ [VA]} \tag{2.1}$$

where the real power is the average power over a line cycle of the instantaneous product of current and voltage, and the apparent power is the product of the RMS value of the current and the RMS value of the voltage. The voltage v_g, and the current i_g, have a line period $T_u = {}^{2\pi}/_{\omega} = 1/f_u$ and can be expressed in terms of its Fourier series components:

$$v_g = V_0 + \sum_{h=1}^{\infty} V_h cos\left(h\omega t - \alpha_h\right) \tag{2.2}$$

$$i_g = I_0 + \sum_{h=1}^{\infty} I_h cos\left(h\omega t - \beta_h\right) \tag{2.3}$$

Voltage and current RMS values in terms of their Fourier components are given by:

$$V_g = \sqrt{V_0^2 + \sum_{h=1}^{\infty} \frac{V_h^2}{2}} \tag{2.4}$$

$$I_g = \sqrt{I_0^2 + \sum_{h=1}^{\infty} \frac{I_h^2}{2}} \tag{2.5}$$

Then, the real power can be written as:

$$P_g = \frac{1}{T_u} \int_0^{T_u} v_g i_g dt = V_0 I_0 + \sum_{h=1}^{\infty} \frac{V_h I_h}{2} cos\left(\beta_h - \alpha_h\right) \tag{2.6}$$

where the phase difference between the voltage and current waveforms at the h^{th} harmonic is represented by $\beta_h - \alpha_h$. The total harmonic distortion of the current ($THDi$) is a term commonly used to quantify the distortion caused by current harmonics, and is defined as the ratio between the RMS value of the current without the fundamental (I_{g1}), and the RMS fundamental magnitude (it is assumed that $I_{g0} = 0$), as is presented in Eq. (2.7).

$$THDi = \frac{\sqrt{\sum_{h=2}^{\infty} I_{gh}^2}}{I_{g1}} \tag{2.7}$$

The current harmonics limits, acceptable power factor and $THDi$ values are defined in all the Standards considering a pure sinusoidal voltage waveform ($V_h = 0 \; \forall \; h \neq 1$). Therefore, Eq. (2.1) can be rewritten considering Eqs. (2.4), (2.5) and (2.6) as:

$$PF = \left(\frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{h=1}^{\infty} \frac{I_h^2}{2}}} \right) cos\left(\beta_1 - \alpha_1\right) = \left(distortion\ factor\right)\left(displacement\ factor\right) \tag{2.8}$$

It can be seen how for sinusoidal input voltages, the power factor value can be rewritten as a product of two terms, one term due to distortion from current harmonics and other term due to the phase difference between the fundamental components of the current and the voltage waveforms. The power factor PF, is a number between zero and one that represents the

efficiency of the power transferred between the source and the load. The maximum ($PF = 1$) is achieved if the load has a resistor behavior. In this situation, the current waveform is a replica of the input voltage waveform with the same harmonics and in phase with the source voltage.

According to (2.7), distortion factor can be rewritten in terms of $THDi$:

$$PF = \frac{cos\left(\beta_1 - \alpha_1\right)}{\sqrt{1 - THDi^2}} \tag{2.9}$$

Usually, line rectifiers have a diode bridge connected to the input voltage, therefore the input current and voltage are in phase, and the degradation of the power factor value is caused by current harmonics; so the power factor becomes:

$$PF = \frac{1}{\sqrt{1 - THDi^2}} \tag{2.10}$$

Off-line AC–DC converters deliver important amounts of power, and power factor correction has of great interest for manufacturers and users. The line current, is in phase with the utility mains voltage, but is often non-sinusoidal with high peak values, placing high stress on circuit breakers, fuses, wall sockets, installation wires, and transformers [20]. For example, it is shown in Fig. 2.1 the line current (blue) in the Power Electronics Lab of the University of Cantabria in June 2012. In red, it is shown a sinusoidal signal with the same RMS value of the current. It can be seen the difference between the two waveforms (around 2.5 A peaks). With current distortion $PF < 1$, a larger RMS current value is required for a desired real power P_g, increasing power losses in the transmission line. Since power companies want to minimize the power loss in the transmission lines, they want customers to have a power factor as close to 1 as possible. For this reason, they will provide penalties or price incentives to encourage users to reduce the cost of energy transmission.

2.2 Standards about line current harmonics and power factor value

Nonlinear loads cause current harmonics, which interact with the utility power system causing harmonic input voltage distortion. As the number of units of electronic equipment powered from the AC line increases every year, the problem of line current harmonics grows up at the same time. Significance of this problem has led to development of standards that place limits on current harmonics assuming a sinusoidal utility voltage. Other standards specify a power factor that must be obtained under certain line and/or load conditions, effectively limiting the maximum amount of harmonic current permissible assuming that the input voltage and current are in phase [21].

The IEC 61000-3-2 Standard [1] is published by the International Electrotechnical Commission (IEC) and it limits the line harmonic content caused by a electrical or electronic

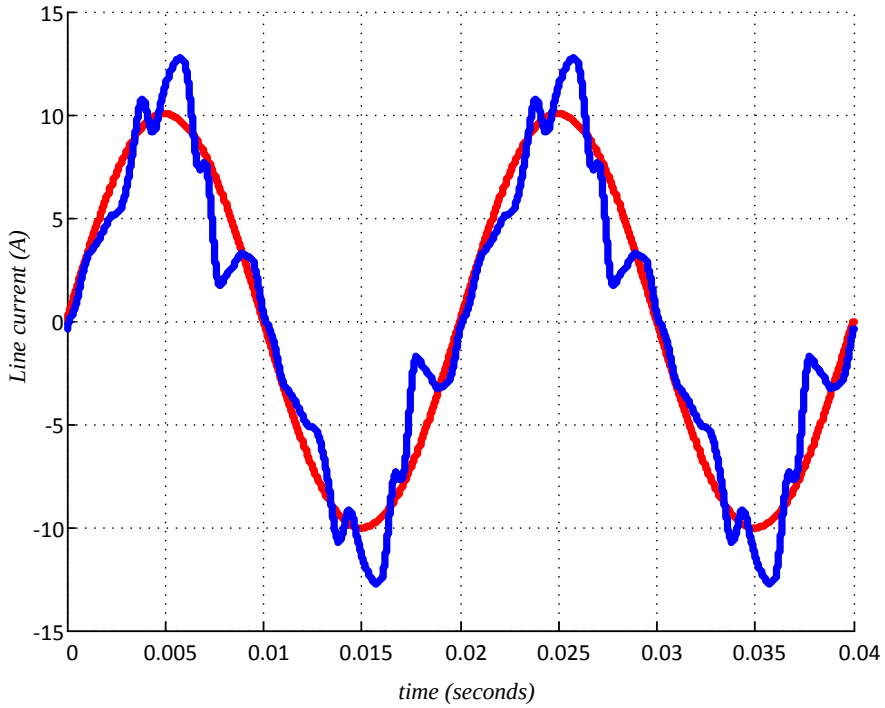


Figure 2.1: Line current (blue) in the Power Electronics Lab of the University of Cantabria at Santander (Spain) in June 2012. In red is plotted the sinusoidal waveform whose RMS values is equal to the line current.

load/equipment with a demanded current per phase up to 16 A. Four classes of load/equipment are addressed to define the allowed amount of current harmonic, as they are shown in Table 2.1. Class B equipment includes portable and arc welding equipment. Class C includes all lighting equipment and Class D equipment like personal computers, monitors and TVs with an input power of less than 600 W. Class A equipment is all the equipment not considered to be any other class.

Current limits are defined at a nominal (pure sinusoidal) utility voltage of 230 V_{rms}, with the PFC stage operating a full load. For Class A and B, the limits are referred to an absolute value of amperes (A), whereas Class C and D limits are defined as a percentage of the current fundamental harmonics and units of mA/W, respectively (see Table 2.1). Class C current limit are the most restrictive.

IEC 61000-3-2 Std is theoretically only applicable in Europe but it has been adopted buy the most of the major electronics manufacturer companies to market universal power supplies. It is common to find products that can operate over a universal voltage range (85-265 V_{rms}) with frequencies of 50 and 60 Hz.

The IEEE Standard 519 [22], published by the Institute of Electrical and Electronics Engineers (IEEE), specifies the limits on particular harmonics as well as on the THD of the current waveform, $THDi$ (Table 2.2). Harmonic limits are given in percentage of the fundamental component of the line current (I_L) depending on the short-circuit current (I_{sc}) at the point of common coupling (PCC).

h^{th}harmonic	Class A (A RMS)	Class B (A RMS	Class C (% 1^{st} harm.)	Class D (mA/W)
3	2.3	3.45	$30\times PF$	3.4
5	1.14	1.71	10	1.9
7	0.77	1.155	7	1.0
9	0.40	0.60	5	0.5
11	0.33	0.495	3	0.35
$\geq$13	0.21	0.315	3	$3.85/h$
2	1.08	1.62	2	-
4	0.43	0.645	-	-
6	0.30	0.45	-	-
$8 \leq h \leq 40$	$1.84/h$	$2.76/h$	-	-

Table 2.1: IEC 61000-3-2 harmonic current limits

I_{sc}/I_L	$h^{th} < 11$	$11 < h^{th} < 17$	$17 < h^{th} < 23$	$23 < h^{th} < 35$	$35 < h^{th}$	$THDi$
<20	4.0 %	2.0 %	1.5 %	0.6 %	0.3 %	5.0 %
20-50	7.0 %	3.5 %	2.5 %	1.0 %	0.5 %	8.0 %
50-100	10.0 %	4.5 %	4.0 %	1.5 %	0.7 %	12.0 %
100-1000	12.0 %	5.5 %	5.0 %	2.0 %	1.0 %	15.0 %
>1000	15.0 %	7.0 %	6.0 %	2.5 %	1.4 %	20.0 %

Table 2.2: IEEE Std 519 Maximum odd harmonic current limits for general distribution systems, 120 V to 69 kV.

In Japan, the Japanese Industrial Standards (JIS) Committee defines current limits equivalent to the IEC 61000-3-2 limits scaling them with the ratio of the fundamental utility voltages in Europa and in Japan ($230/100 = 2.3$).

Other agencies may find it necessary to impose additional harmonic restrictions for critical applications. The U.S. military was one of the first organizations to adopt a current harmonic regulation with a 3% limit [23,24]. Boeing and Airbus, the aircraft companies, adopted their own proprietary power quality standards for airborne equipment. These standards specify power quality requirements for a range of AC line frequencies, from 360 Hz to 800 Hz.

2.3 Digital control of Switched Mode Power Supplies

If a power converter designer would have to define the main challenges or goals of a Switched Mode Power Supply (SMPS), the answer could be [25]:

- To convert the energy between the input and the output, in some applications with a bidirectional flow, so as to guarantee the highest efficiency.
- To satisfy the expected operations to offer a high grade of precision, flexibility, communication capability and reliability to the end user.
- To decrease the overall costs.

This expected behavior must be achieved despite of the disturbances, tolerances, non-linearities, and a control is needed to drive the converter according to the value of the measured inputs and the expected outputs.

Traditionally, control systems was based on analog systems. But analog controllers permit only a limited set of standard functions. Analog controllers are usually constrained to linear functions, with a large number of passive components. This reduce the reliability, the efficiency and increase the complexity and space of the system, with a reduced computational capability. But from the designer point of view, the digital controller design can be less intuitive than the traditional analog design.

In the last 20 years, the capabilities of the digital devices (DSPs, CPLDs, FPGAs, Microcontrollers...) have increased in an exponential way, and the cost of these digital devices has decreased a lot. Due to that, digital control systems have become more attractive as they allow the implementation of complex control strategies and functions that are not realizable in the analog domain (communication and system level integration, controller autotuning, efficiency monitoring and optimization, and complex nonlinear control for improved dynamic performance) [25–27].

Microcontrollers and Digital Signal Processors (DSPs) embed input/output capability (analog and digital), making the connection with the power converter simpler; including 16 or 32-bit core, RAM and FLASH memory, analog-to-digital converters, PWM modules, pulse counters... Communication channels like SPI, CAN bus (very popular in automotive applications), USB, Ethernet, Zig-Bee, WiFi appears in some commercial boards that enable the connection to computers and other devices.

FPGAs can contain digital circuits with sophisticated system features, more logic flexibility and much higher complexity. The speed, size, and number of input and output pins far exceeds that of a microcontroller or DSP [25, 28].

But not only the digital devices have improved their capabilities. The simulation and design of digital controllers have decreased with the evolution of the software employed by the designer. Nowadays, there are several tools like MATLAB/Simulink or LabView of National Instruments offers an automatic code generations in high level languages. The design and simulation is developed with block diagrams that are translated into the "C" or "VHDL" languages and implemented in the digital device or embedded platform. Hardware-in-the-loop (HIL) simulation is another approach used to simulate (in real time) the behavior of the controller with the power converter, decreasing the simulation time [29].

Digital control, juxtaposed to analog control of switched mode power supplies, present several advantages and challenges [26, 30]:

- **Integration and reduction of discrete components:** The ongoing advances in power semiconductor technologies industry makes an integration of high-performance digital controllers with power semiconductors very attractive.

- **Reduced sensitivity to parameter tolerances:** The properties of the discrete components change with temperature and with the increasing age of these components. When used in analog controllers, specifically for control loop compensation, the resulting compensator can change significantly over time or with a considerable temperature change. As a digital controller's, control law is not implemented with discrete components, so these effects due to temperature and aging, or environment variations, are completely avoided.
- **Efficiency optimization:** with digital control it is possible to make on-the-fly adjustments to the operating parameters of a switching converter in order to optimize the efficiency, or in applications with several converters working in parallel and controlled by the same digital device.
- **Adaptive control:** Adaptive control refers to changing the implemented control law depending on present or past controller inputs. While it is not impossible to implement adaptive control with an analog controller, it is considerably simpler to accomplish with digital controllers. Also, the incremental cost of including adaptive control is relatively low once a digital controller is implemented. Adaptive control is attractive due to it's use particularly in realizing higher bandwidth regulation and converter efficiency improvements due to adaptive control actions. Control approaches, among others, like predictive current mode control, improve the dynamic response of the inductor current of the power converters, and are impractical with analog controllers.
- **Digital autotuning:** "Autotuning" represents the idea of a plug-and-play controller or system that automatically identify the system (power converter). This approach has a great interest in the industry.
- **Power System Management:** It is based in the idea of "Flexibility". A digital power management system is used to address communications and/or control outside one or more power supplies, including functions as power system configuration, control and monitoring and fault detection. It has a basic architecture consisting of power supplies communicated with a centralized power system host via digital communications bus. The Power Management Bus (PMBus) is a protocol adopted by several manufacturers [9], derived of the Inter-IC (I2C) bus, but focused to provide a greater functionality for power control applications [31].
- **Controller cost:** With the ever increasing density of digital logic prevalent in the computer processor industry, it is conceivable that a digital controller might eventually become more inexpensive than available analog controllers. This is particularly true for full-featured digital controllers as adding features in digital design does not greatly increase the cost of a controller whereas additional features in analog controllers often greatly increases their cost.

A good industry application example of comparison between analog a digital controllers is presented in [32]. The product used in the case study is the Ericsson PMH8918 Point of Load

(POL) regulator (an 18 A non-isolated synchronous buck regulator with a programmable output voltage and a nominal 12 V input voltage). It is shown how replacing some of the analog components with digital circuitry provides performance benefits without penalties of cost or design complexity, and how is possible to add an additional functionality of digital power management with a simple cost effective communication interface. The next are, literally the conclusions presented in the technical paper; and represents a real example of how a digital control can offer a good alternative to the standard analog control in a commercial power converter:

- *"The general electrical performance of the digitally controlled regulators is equal to or better than the analog version".*
- *"At the same current level, the efficiency of the digital designs is higher than that of the analog version. Efficiency improvements excess of 1% are possible".*
- *"The digital designs have a definite advantage in terms of packaging density. This can be used to make POLs smaller or to increase the power available within the standardized package size".*
- *"The digital designs exhibit drastically improved current and power densities when compared to the analog POL regulator, ranging from 289 % to 330 %".*
- *"The digital designs substantially reduce the parts count, a 58 % reduction for the 20 A POL design and 29 % for the 40 A version".*
- *"Due to low parts count and increased integration, digital designs are expected to offer outstanding value to the user when compared to analog POLs".*

But digital controllers have some limitations that should be considered. The resolution and range are limited by the number of bits used in the digital control, and the PWM resolution and the upper limit of the switching frequency are defined by the device clock frequency. Digital controllers suffer from latency issues that are not present in traditional analog controllers. The first latency issue is caused due to the sample rate of the analog ADCs used to sense controller inputs. These ADCs typically convert at a fixed rate that directly affects the response of the controller to a disturbance. If a disturbance occurs right after the previous sample point, the digital controller will not respond to the disturbance until the next sample instance. Additionally, the time it takes to process the digital inputs and generate a proper control output requires a finite amount of time depending on the type of hardware used to implement the controller and the controller clock rate/frequency. For ASIC and FPGA implementations processing of the appropriate control output can be computed in parallel requiring a minimum of one clock cycle after the controller inputs are valid. Microprocessor implementations often take far longer or require a high performance microprocessor to compute the control law as common microprocessors compute serially, thus requiring a number of clock cycles to produce an output. Limit cycling [33, 34] is

another common problem associated with digitally controlled switching converters due to the quantization effects of the ADCs and the PWM

It is well-known how Digital control in Switched Mode in Power Supplies is a topic which represents a great percentage of the articles presented nowadays in conferences and magazines of reference of the IEEE Power Electronics, Industrial Electronics or Industry Applications Societies. Among others, recent developments of digital control for DC/DC switching converters (digital power factor correction controllers are addressed in more detail in next section 2.4.3) are:

- Autotuning controllers in predictive current-mode control [35], based on the online frequency [36, 37] or impulse response [38], with the goal of keeping the loop stability behavior in the DC/DC converter tuning the LSB of the digital controller [39], or using a multiple-input-multiple-output (MIMO) controller to adjust continuously the PID compensator considering DCM-to-CCM mode transitions [40, 41].

- Predictive control: [42–44].

- Feedforward control: [45]

- Improvement of the dynamic behavior with digital Time-Optimal Controllers [46–48] under load transients, or lineal/nonlinear controllers [49] implemented in low-cost FPGAs which does not need the value of the buck converter output inductor, or with new adaptive slope control techniques (nonlinear) [50].

- Online system identification [51–54].

- Efficiency optimization and operation over a wide range of input voltages with pulse-width modulation/pulse-frequency modulation (PWM/PFM) controllers and input voltage feedforward [55], reducing the turn-on switching losses on DCM mode [56], with reconfigurable structure DC-DC converters [57], or with scalable solutions [58].

- Increasing the resolution of the digital controller [59, 60].

- Smart power management systems, that can be configured depending on the operating conditions of the different DC-DC converters operating in parallel [61], or improving the current sharing in multiphase converters with nonidealities [62].

These trends and references are only a small representative of the actual research in digital control in switched-mode power supplies around the world. Digital control is revolutionizing the industrial world, introducing complex control techniques which are impossible to be implemented with analog systems. Nowadays, a high percentage of power converters, except those with low power, include one or more microcontrollers, DSP or ASICs (CPLD or FPGA), or a combination of them. And furthermore, digital control is gaining new applications and in a future it will be used wherever power or energy must be controlled.

2.4 PFC converters

Several topologies used as PFC stage are Switched Mode Power Supplies connected to the utility. Basically, any converter topology like SEPIC, Ćuk or Buck-Boost converters are capable of producing input-to-output conversion ratios from 1 to infinity can be employed in the PFC applications. The Boost converter operating in continuous conduction mode is the most popular PFC topology, offering several advantages over the buck, flyback or SEPIC configurations. If isolation is not required and it is acceptable that the DC output voltage be higher than the peak AC input voltage, the boost converter is the mainstream type topology for rectification purposes. The characteristics of the different solutions are [63]:

- ***BOOST CONVERTER:***
  - Lowest transistor RMS current, highest efficiency (95 % is typical in a 1 kW application).
  - Isolated topologies are possible, with higher transistor stress.
  - No limiting of inrush current. When the output voltage is lower than the instantaneous input voltage, is not possible to control the inductor current. When the output capacitor is initially discharged, a high inrush current occurs, although auxiliary circuitry can be employed to manage this problem.
  - Output voltage must be greater than the peak input voltage.
- ***BUCK-BOOST, SEPIC, and ĆUK CONVERTERS:***
  - Higher transistor RMS current, lower efficiency (the switches process all the power of the converter).
  - Isolated topologies are possible, without increased transistor stress.
  - Inrush current limiting is possible.
  - Output voltage can be greater than or less than peak input voltage.

A variety of integrated circuits (ICs) are commercially available to simplify the goal of power factor correction. They integrate the various blocks that would have been separate ICs previously onto a single control chip, and require the design and implementation of an array of external passive components for the correct operation. Operating in the CCM, a well-known commercial IC is the UC3854 [5] of Texas Instruments.

The disadvantage of operating in the CCM is the increased stress on the boost power diode. During OFF-time, the load current flows through the diode, and the the converter turns ON, the diode must to recover quickly. Due to the reverse recovery time, t_{rr}, during in which the device experiences reverse current through, and reverse voltage across it, generating power losses on the diode. Furthermore, the reverse diode current increase the turn-ON losses on the MOSFET. Faster, SiC or Schottky diodes are used to manage this problem.

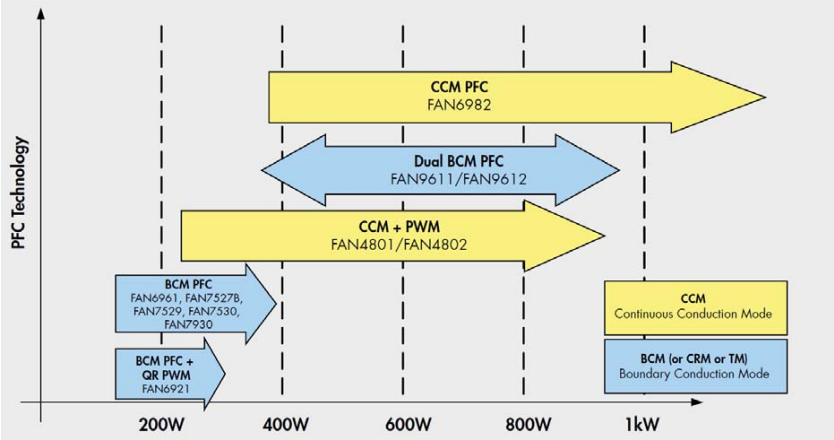


Figure 2.2: Fairchild PFC technology portfolio.

Figure 2.2 shows the PFC technology portfolio offered by Fairchild semiconductor, with the commercial ICs available and the power range recommended for each technology. Boundary conduction mode BCM (or Critical Conduction Mode - CrCM) is used in low power solution (300 W or lower), adding QR (Quasi-resonant) PWM modules when the power is around 200 W. Dual BCM PFC technology controls two parallel-connected boost power trains 180º out of phase. With this interleaving, it is possible to extend the maximum practical power level of the control BCM technique from about 300 W to greater than 800 W, offering inherited zero-current switching of the boost diodes. On the other hand, the number of discrete components is higher. As it has been addressed before, CCM PFC for high power applications above 300 W is the most commonly used since the inductor current has a small ripple and higher power factor can be achieved; but a high-speed diode with a small reverse recovery current is crucial to achieve high efficiency and low EMI.

In [19] a detailed comparative analysis of the different PFC approaches evaluated for a 300 W application with the ON Semiconductor PFC commercial ICs, with the following observations for the CrCM (BCM) and CCM control modes:

- ***CrCM (Critical conduction mode):***

  - Pros: Good Efficiency for power levels below 300 W.
  - Cons: Switching frequency variation, bigger PFC choke, a differential mode choke is needed to reduce the input current ripple and EMI. This differential mode choke introduces more losses, affecting the overall efficiency.

- ***CCM (Continuous conduction mode):***

  - Pros: Fixed frequency, lower EMI filter, and a smaller ripple on the input and output stage which create little stress for the input filter and output capacitor. Therefore this control mode is more suitable for high power applications.

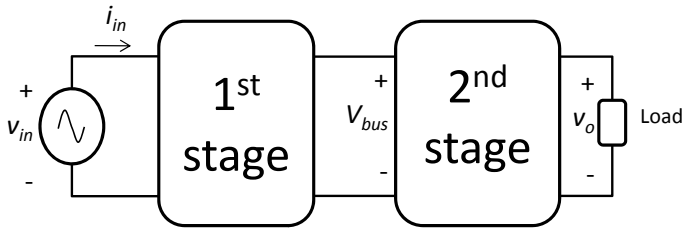


Figure 2.3: Typical power supply block diagram.

- Cons: This mode exhibits higher switching losses due to the Q_{rr} of the boost diode. In this control mode, the boost diode therefore becomes a critical component of the PFC stage.

2.4.1 Boost converter. Fundamentals

PFC rectifiers are typically only part of a electronics power supply. A typical complete power supply, shown in Fig. 2.3 uses a first stage whose goal is to supply a second stage and fulfill all the requirements in the point of view of the utility mains, like harmonics current limits defined by the standards (see Section 2.2), so a PFC stage is commonly placed in this 1st stage. This PFC converter processes the utility mains AC power into a regulated DC output voltage V_{bus}, that is often in the 380 - 400 V range. A second stage, commonly a DC-DC switched mode power supply is used to process the voltage a current available at the output of the boost PFC stage. The characteristics of the Boost converter have been addressed before, and in practice, in the 90 % of the applications, a Boost PFC converter with a 2nd DC-DC stage (with isolation is needed) is the classic adopted approach. This converter processes up or down the voltage to the application or load supplied.

As in all of the switched mode power converters, the current and the voltage are modulated adjusting the duty cycle d of a constant frequency ($f_{sw} = 1/T_{sw}$) drive signal ($on - off$) applied to a MOSFET, as is shown in Fig. 2.4. During the interval dT_{sw}, the MOSFET (Q) is ON and the diode (D) is OFF. The rest of the time of the switching period $(1-d)T_{sw}$, the MOSFET is OFF, the diode is ON, supplying energy to the output RC filter if operating in the CCM. Then, the given inductor voltage and capacitor current for the interval dT_{sw} are:

$$v_L = v_g \tag{2.11}$$

$$i_c = -\frac{v_o}{R} \tag{2.12}$$

During the rest of the switching period $(1-d)T_{sw}$,

$$v_L = v_g - v_o \tag{2.13}$$

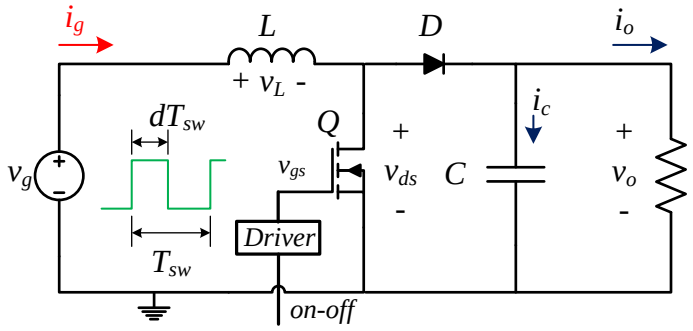


Figure 2.4: DC-DC boost converter.

$$i_c = i_L - \frac{v_o}{R} \tag{2.14}$$

These equations define the inductor and capacitor dynamics, knowing that $v_L = L\frac{di_L}{dt}$, and $i_c = C\frac{dv_o}{dt}$, respectively. The average behavior of the inductor variables (2.11) and (2.13) can be combined as:

$$\langle v_L \rangle = L\frac{d\langle i_L \rangle}{dt} = v_g d + (v_g - v_o)(1-d) = v_g + v_o(1-d) \tag{2.15}$$

and (2.12) and (2.14) as follows:

$$\langle i_c \rangle = C\frac{dv_o}{dt} = -\frac{v_o}{R}d + \left(\langle i_L \rangle - \frac{v_o}{R}\right)(1-d) = \langle i_L \rangle (1-d) - \frac{v_o}{R} \tag{2.16}$$

where $\langle x \rangle$ represents the average value of variable x over the switching period T_{sw}. The low frequency nature of the v_g and v_o voltages, leads to approximate $\langle v_g \rangle \approx v_g$ and $\langle v_o \rangle \approx v_o$. These expression define the state equations of the Boost converter operating in the CCM, which means that the inductor current (i_L) stays positive over the switching period. The Boost converter waveforms in the CCM operation are presented in Fig. 2.5a.

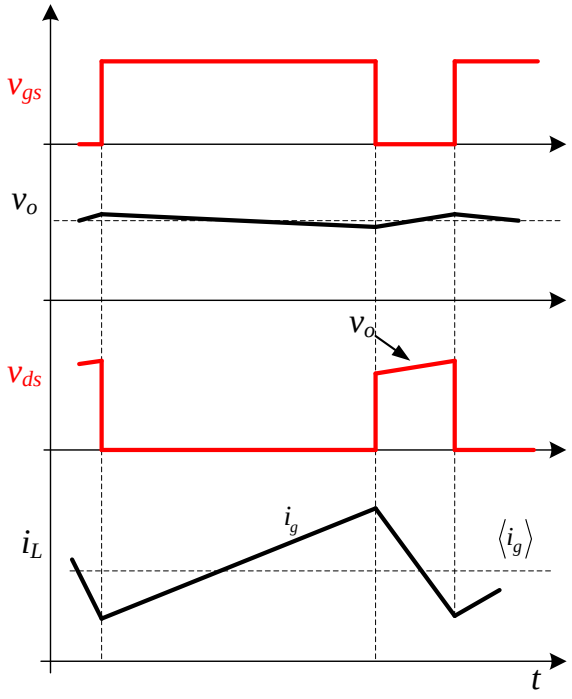
In steady state operation, in the output capacitor and the inductance, it is derived that (2.15) and (2.16) are equal to zero, giving the DC voltage conversion ratio (defined as M),

$$M = \frac{v_o}{v_g} = \frac{1}{1-d} \tag{2.17}$$

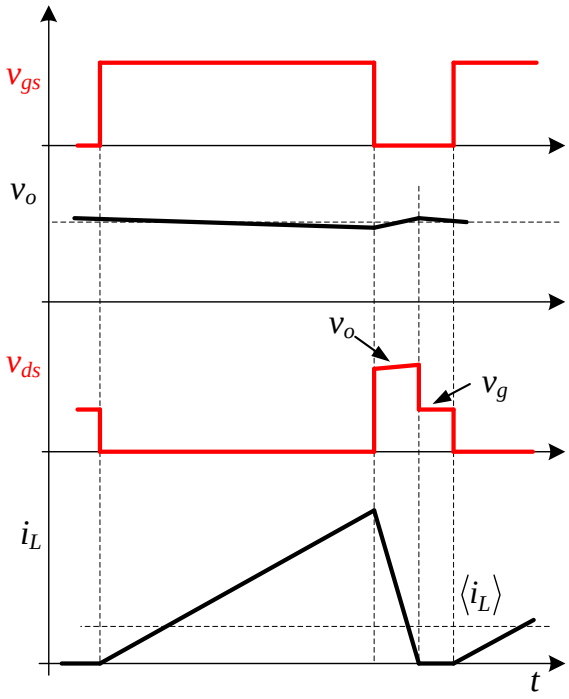
and the average inductor current,

$$\langle i_L \rangle = \frac{v_g}{(1-d)^2 R} \tag{2.18}$$

On the other hand, if i_L ramps down to zero before the end of the switching period, it is said that the converter operates in the Discontinuous Conduction Mode (DCM), and the waveforms are represented in 2.5b. In [20, 63] a deep analysis of the Boost converter is presented. The time interval (in DCM) of the switching period when the diode is conducting is defined as $d_2 T_{sw}$, and as K a parameter that measures the tendency of a converter to



(a) CCM operation waveforms.



(b) DCM operation waveforms.

Figure 2.5: Boost converter waveforms in CCM (a) and DCM (b). MOSFET gate signal (v_{gs}), inductor current (i_L), MOSFET drain-to-source voltage (v_{ds}) and output voltage (v_o).

CCM: $M(d)$	DCM: $M(d,K)$	DCM: $d_2(d,K)$	$K_{crit}(d)$
$\frac{1}{1-d}$	$\frac{1+\sqrt{1+4d^2/K}}{2}$	$\frac{K}{d}M(d,K)$	$d(1-d)^2$

Table 2.3: CCM-DCM mode boundaries for the Boost converter.

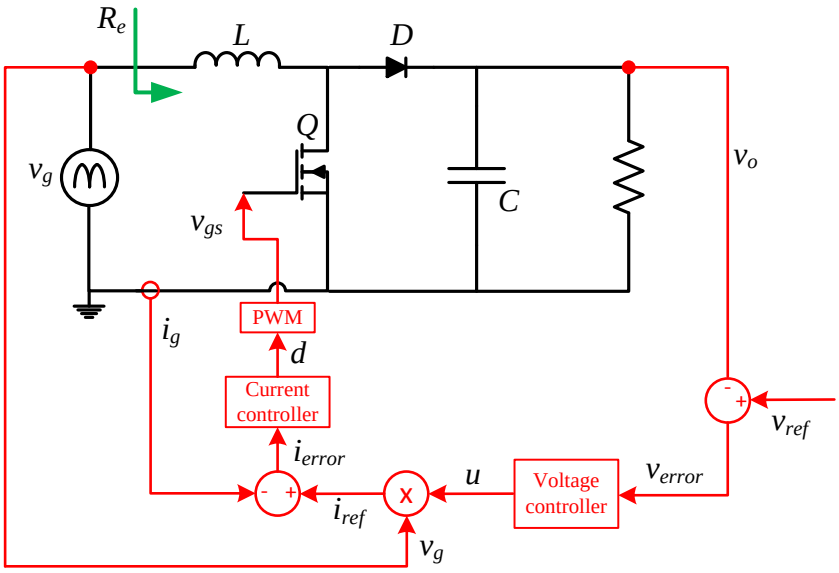


Figure 2.6: Block diagram of the average current mode control in a Boost converter.

operate in the DCM, equal to $K = \frac{2L}{RT_{sw}}$. K_{crit} is the critical value of K that defines the boundary between DCM and CCM.

Table 2.3 shows the values of M, d_2 and K_{crit} for the Boost converter as functions of d and K. The CCM is assured if $K_{crit} > K$.

2.4.2 Analog Control in PFC converters

Different analog PFC control approaches have been developed, but among them, maybe the most prevalent on boost PFC stages is the average current mode (ACM) controller. This approach is represented in Fig. 2.6. It has, a current loop and voltage loop [63]. Operation of the ACM PFC rectifier is straightforward. In order to obtain low harmonic distortion of the input current (i_g), the emulated input resistance (R_e) has to be constant over the line cycle.

An inner current loop (with high bandwidth around 1-10 kHz) is used to regulate the average value of the current as a reference (i_{ref}) which is proportional to the rectified input voltage (v_g). A power command signal (u) is adjusted by a outer voltage loop (with low bandwidth around 10 Hz) given by an output voltage controller to regulate the output voltage of the power supply (v_o). The outer voltage loop requires a low bandwidth in order to avoid a distortion in the input current waveform. A considerable voltage ripple on the output at the double of the line frequency exists. This ripple is due to the inherent instantaneous power imbalance between the AC input and DC output. As the output is supplying a constant (or

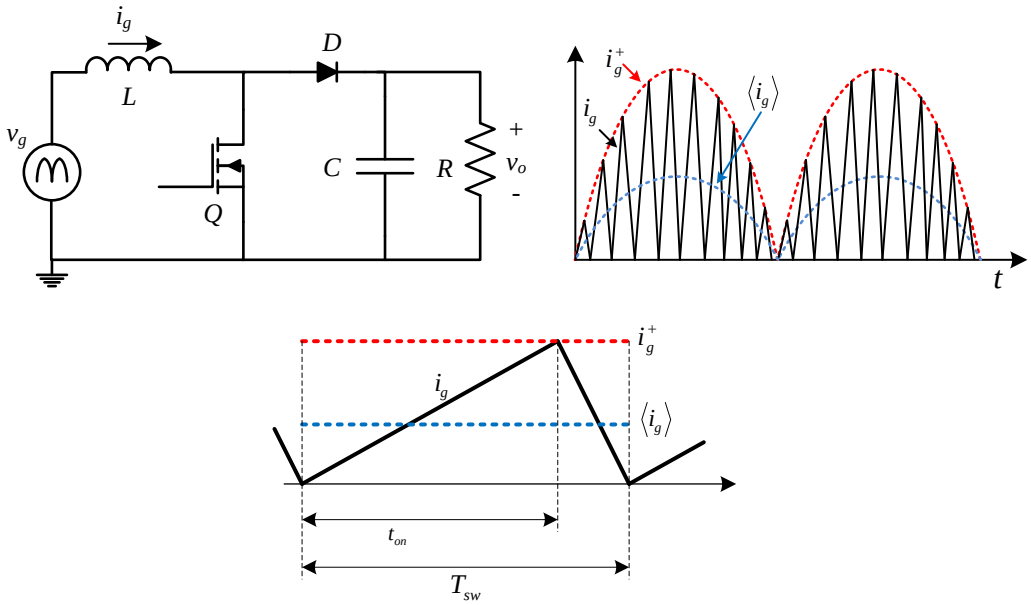


Figure 2.7: Waveforms of critical conduction mode control in the boost converter.

near constant load) in normal operation the output voltage drops when the power processing of the PFC stage is lower than the output power draw. Likewise, the output capacitor is charged and the output voltage increases when the instantaneous input power is greater than the output power draw. Due to the low bandwidth of the voltage loop, u is constant over the line cycle, and i_{ref} value is proportional to the input voltage.

This control tracks the average input current i_g, in each switching period, so a filtering action of the instantaneous input current measurement is implemented. Average current mode approach in PFC controller allows the converter to operate in CCM or in DCM.

Three variables have to be sensed in this controller to achieve power factor correction: the rectified input voltage (v_g) is used to shape of the current waveform, the rectified input current (i_g) is sensed to be regulated by the inner current loop, and the output voltage (v_o) is sensed to assure the desired output voltage.

Another control approach, widely used in Boost PFC stages for low power applications ($<$ 200 W), is the critical conduction mode (CrCM) controllers, also called transition mode (TM) controller, operates the boost PFC rectifier at the boundary between the CCM and the DCM. The current waveform are shown in Fig. 2.7 [63]. The controller keeps a fixed transistor turn-on interval ($t_{on} = T_{on}$) over half of the line period and ends the transistor OFF-time when the inductor current reaches zero. Therefore, the switching period (T_{sw}) varies over the line cycle. Critical conduction mode controller makes the average inductor current $\langle i_g \rangle$ follow the input voltage and exhibits loss-free-resistor (R_e) as Eq. (2.19) without reference current multiplication. Critical conduction mode boost PFC controllers are classified as the voltage follower type.

$$R_e = \frac{v_g}{\langle i_g \rangle} = \frac{2L}{T_{on}} \tag{2.19}$$

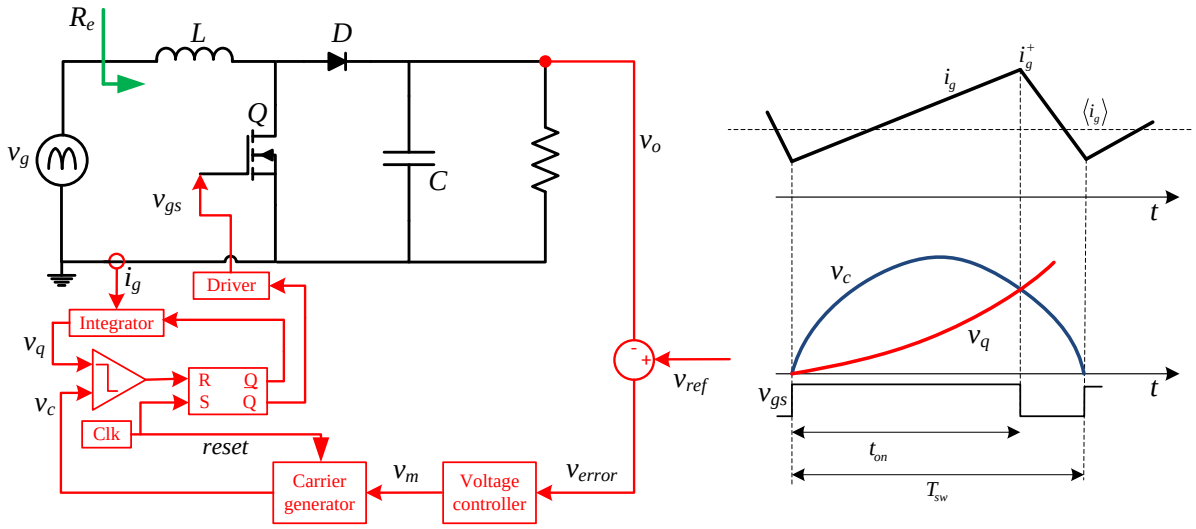


Figure 2.8: Left: Block diagram of nonlinear carrier control (boost example). Right: Waveforms of nonlinear carrier control (boost example) [15].

Nonlinear carrier control (NLC) is the third approach of the mainly analog controllers approaches used for PFC Boost controllers. NLC controller applies the ideal quasi-steady state conversion characteristic in CCM and shapes the input current without need of input voltage sensing. This approach is presented in [15] and [64] for Boost and Up-Down converters, respectively. NLC controllers forms a simple current loop by using a periodic reset integrator and a Set-Reset flip-flop with a nonlinear carrier waveform generator, as illustrated in Fig. 2.8. When the amount of charge flowed through the inductor (v_q) reaches the nonlinear carrier waveform (v_c), the gate signal resets, as Eq. (2.20) (corresponding waveforms are shown in Fig. 2.8). In comparison with the average current mode (ACM) control, this approach requires no amplifier in the current-shaping loop, no sensing of the input voltage, and no multiplier/divider in the voltage feedback loop.

$$v_q\left(t_{on}\right) = \int_0^{t_{on}} i_L\left(\tau\right) d\tau = \frac{V_o T_{sw}}{R_e}\left(\frac{t_{on}}{T_{sw}}\right)^2\left(1 - \frac{t_{on}}{T_{sw}}\right) \tag{2.20}$$

Besides the analog PFC controllers mentioned above, including multiplication approaches, follower approaches, and charge approaches, recently, with the development of the digital circuits, digital PFC controllers are getting more and more attention. Although some works about analog controllers have been presented recently, for example in [65–67] for PFC rectifiers with high output voltage ripple to decrease the output capacitor value. A new nonlinear controller called “The Voltage-Controller Compensation Ramp” (VCCR) is presented in [68].

A digital version of this NLC control is the PFC control approach used in this thesis, with modifications in comparison with the original one presented in [15]. It is presented with more details in Section 3.2.

2.4.3 Digital control in PFC converters

In Section 2.3, it has been addressed the interest of the digital controllers in comparison with the standard analog controllers. With analog control it is required to implement as many components as needed for desired controller performances; while with a digital controller only is necessary to modify control law/equations. Advanced control techniques has been presented in the recent years, developed with a digital control:

- Autotuning controllers to set the desired controller crossover frequency and phase margin in the controller adjusting the compensator gain [69] or the PID parameters [36], to improve the transient response [70].

- Predictive control of the current: [35, 44, 71–73].

- Feedforward control to increase the crossover frequency of the current loop [74–76].

- Dynamic improvements with a Lyapunov-based digital control [77], with the utilization of the circle criterion [78], modifying the output voltage ripple [79], simply varying the gain of the voltage feedback loop considering the load variations [80], replacing the energy storage capacitor (in 2-stage single-phase rectifiers) by a non-symmetric capacitive divider with independent voltage controls [81], or using "dead-zone" digital controllers [82]

- Operation improvements over wide load ranges [83–87], or universal input voltage range [88].

- Control of interleaved or dual PFC converters: [89–93].

- Control of Bridgeless PFC Boost converters: [86, 94]

In [95] a digital implementation of a "nonlinear carrier" (NLC) control is presented in comparison with two different linear PFC controllers. Simulation and Experimental Results show a better behavior of the nonlinear controller in steady state (lower $THDi$ and 3th current harmonic). On the other hand, linear controllers have a better dynamic response under voltage and load steps down, with a similar behavior of the three controllers under load steps up.

An interesting tendency is to avoid some measurement in the PFC stage. For example, in [44, 96–98] the input voltage is not measured, or in [99], where the output voltage is the avoided measurement. This aspect is presented in more detail in Section 2.6.

The concept of Harmonic Resistance in a Boost PFC converter with digital control is presented in [100]. Important aspects to take into account in digital controllers are the resources of the digital device or its clock frequency, that can limit the switching frequency. Due to that, some works present algorithms with low requirements for the digital device [101, 102].

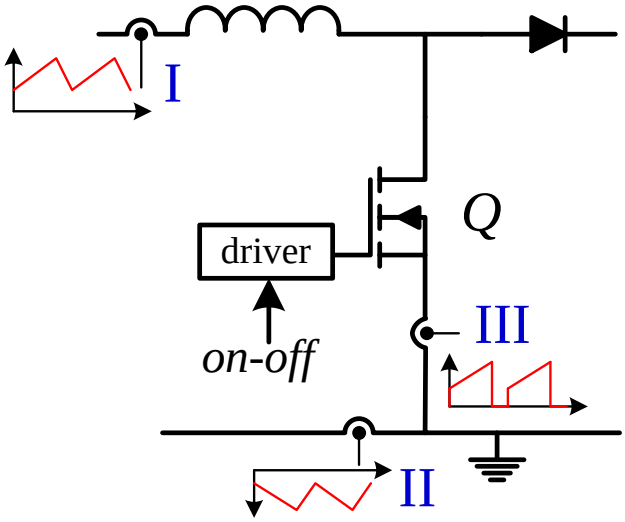


Figure 2.9: Current sensing options in a power converter.

2.5 Current Sensing in Switched Mode Power Supplies

An important aspect in the control of switched mode power supplies of considerable power is the measurement of the variables needed to control the system. Typical values of the voltage of digital devices are 3.3 V, 5 V, o 12 V, while the variables under control can reach values of cents of volts (converter input or output voltages), or tens of amps. In these cases that, the sample circuits must be designed carefully, because the measurement information is transmitted in a environment with considerable EMI.

Although it is common to associate the SMPS design with only a voltage regulation, there are applications in which a current mode behavior is needed, so it is necessary to sense the current. Several authors have highlighted the difficulty of current sensing in comparison with voltage sensing in SMPS [103–105]. A a review of the different current sensing techniques in switched mode power supplies is presented in [103, 105–108].

In current sensing, a trade-off between bandwidth, cost, losses, size and accuracy is made. The chosen current sensing technique depends on the converter application. One reason for the industry not to change on mass to digital controllers is because there are many practical problems perfectly solved with analog designs, and the high and interesting capabilities of the digital control have a higher cost. But this is not the only reason; another obstacle for the use or implementation of digital control in commercial power converters is the more complicated current sensing required.

Figure 2.9 shows the three different options to insert a current sensor in a switching converter to measure the input current. In option I, the inductor current is directly measured. A voltage changing in common mode appears, so some isolation is needed at this point. Solution II is the most popular in PFC converters, because is related to ground, allowing the use of a simple current resistor. But at point II, short circuit currents do not pass through the current resistor, and so on, they are not detected [107]. The use of the current measurement,

with the option II, needs amplification large enough in a digital control to be an input of the analog-to-digital conversion stage and a filter to attenuate the influence of the switching noise and the parasitic inductance effect (Subsection 2.5.1). In position III, a current transformer is typically placed. With a current transformer, the output signal is isolated and can be used directly by a analog-to-digital converter. According to Fig. 2.9, the current at this point is equal to the input current during ON-time of the MOSFET, being this value used in the control. The drawback of using the current transformer is the limitation on the minimum/maximum duty cycle of the switch for the transformer to be magnetized/demagnetized, respectively, without reaching saturation.

To be placed in the different positions presented in Fig. 2.9, different current sensing techniques can be addressed [107] :

2.5.1 Current sensor

It is the most common approach in applications such as power factor correction and overcurrent protection, due to its simplicity and cost. A dedicated sense resistor R_s, in series withe the inductor, functions as a current-to-voltage converter. The voltage across the sensor is proportional to the current flow. In can be used to sense both AC and DC currents.

The drawback of this sensing technique are the power losses incurred by resistor R_s, which can be calculated via Ohm's law (i^2R) and increases with the square of the current. Due to that, this aspect restricts the use of resistive sensor in high current applications.

For digital control applications, the voltage drop across the sense resistor also need a costly amplification so as to obtain a signal large enough for the ADC. It does not provide measurement isolation from transient voltage potentials on the load, and a noise filter is required to reduce the noise in the signal output, which affect the overall system bandwidth.

The current sensing resistor must be selected considering [103]:

- Low values to minimize the power losses ($R_s < 1\Omega$).
- Low parasitic series inductance (L_r) due to the high di/dt that occurs in SMPS.
- Tight tolerance on initial value and low temperature coefficient for accuracy.
- High peak power rating to manage short high current pulses.
- High temperature rating for reliability.

Several manufacturers offer different types is current sense resistor, depending on the application, frequency of the current, magnitude of the measurement ...

The first criteria in determining the sense resistor's value is, often, the voltage threshold of the following components (circuitry) which operates with the current sample. For example, this voltage threshold can be defined by the voltage range in nominal conditions, or by the

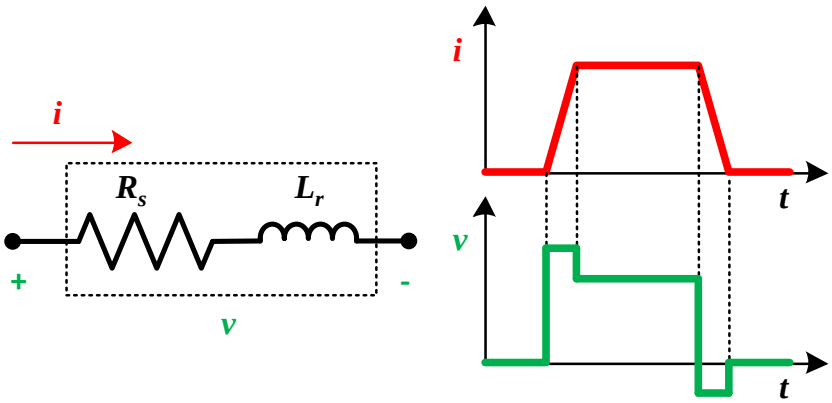


Figure 2.10: Resistor inductance combined with high di/dt can cause voltage spikes in the current measurement.

overcurrent protection. In more specific applications, the value is defined together with the amplification stage to minimize the voltage drop across the resistor. For example, in the commercial UC3854 integrated circuit [5], the peak voltage of 1 V across the resistor is recommended to have good noise margin but which is small enough to have a low power dissipation.

Another important aspect to take into account is the nature of the current waveform. The sensor circuit must be able to measure the steady state current, but capable of manage (or even measure) also current peaks due to the transients.

In [103] several points are addressed to consider in the election of a resistive sensor and design of the sensing circuitry, but include the parasitic series inductance (L_r) with the resistor R_s.

As it is shown in Fig. 2.10, when the resistor is exposed to a high current slew rate, a peak or step appears in the voltage drop. This may cause an error or a prematurely overcurrent detection. Due to that, several manufacturers have developed techniques to obtain "non-inductive" current resistors, but it should be remembered that this is a subjective term and, the higher the current, the less inductance it takes to create problems.

2.5.2 R_{on} sensing

MOSFETs have a resistive behavior when the are in ON-state and biased in the ohmnic region. The value of the ON-state resistance R_{on}, is given by Eq. (2.21), where μ is the mobility, C_{ox} is the oxide capacitance per unit area, v_{gs} is the gate to source voltage and v_{th} is the threshold voltage, and w and l the MOSFET length and width, respectively. Therefore, the switch current is determined by measuring the drain-to-source voltage, v_{ds} during ON-state (Fig. 2.11a).

$$R_{on} = \frac{l}{w\mu\frac{C_{ox}}{l}\left(v_{gs} - v_{th}\right)} \tag{2.21}$$

The main drawback of this technique is its low accuracy. The value of R_{on} is inherently non-

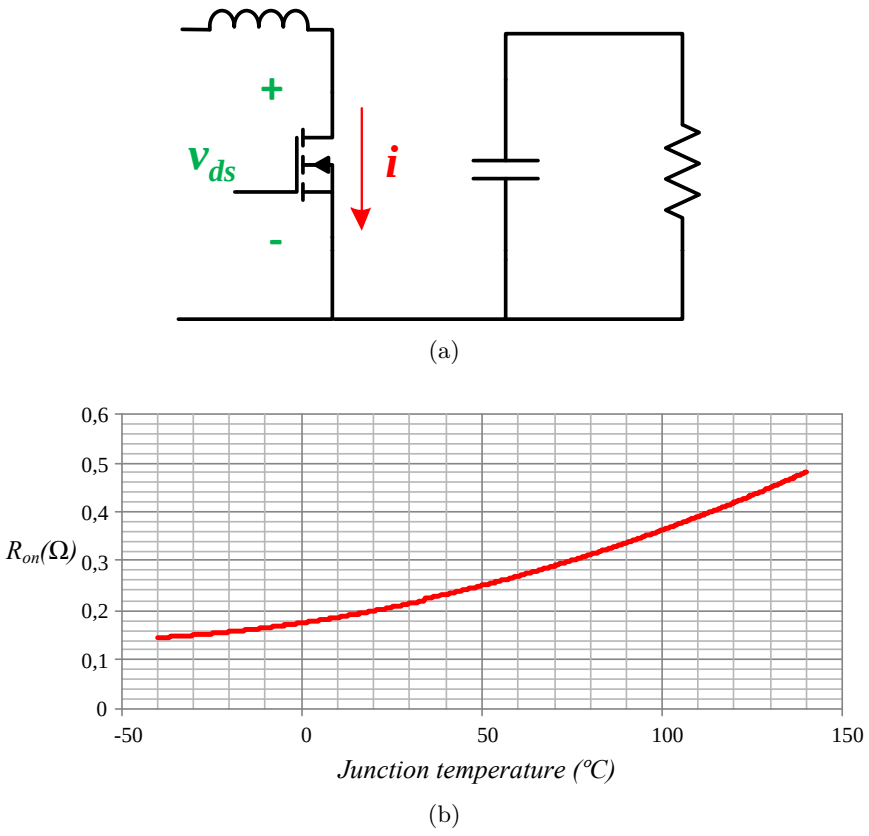


Figure 2.11: (a) MOSFET R_{on} Current Sensing scheme and (b) Normalized drain-to-source ON-resistance R_{on}, vs Junction Temperature for the IRF840 Power MOSFET of Fairchild.

linear due to the variation of μ, $C_{ox}$and v_T with the temperature [106], causing a exponential dependency of the R_{on} value with the temperature (around 35 % of variation from 27 ºC to 100 ºC) as is shown in Fig. 2.11b. MOSFETs ON-state resistor is not optimized to be used as current sensor, so parasitic elements of the power MOSFET have an undesired influence working at higher frequencies. Despite this low linear behavior and accuracy, this method enjoys commercial use for over current protection, for example in portable electronics devices like cell phones or laptops. Furthermore, the use of this technique needs a calibration, as is presented in [109], representing an extra cost.

In the case of a Boost PFC converter, this technique can not be applied because the drain-to-source is a pulsated voltage at the switching frequency with a low value during ON-state with a value of $I \times R_{on}$, and a high value of hundred of voltages (around 400 V_{dc} in the boost converter used in this thesis).

If more accuracy is needed in the current-mode converter, matched Sense-FET devices built in parallel with the power MOSFET can be used. These devices are not strongly dependent on parameters such as frequency, temperature, switching frequency or external components, based con current mirror techniques [110].

2.5.3 Filter-sense the Inductor

This approach is used in [111, 112], and is based in filtering the inductor voltage in switched mode power supplies using the inherent parasitic resistor R_L. The voltage across the inductor is given by Eq. (2.22), and the second term $L\frac{di_L}{dt}$, can be eliminated if the inductance value is known and a filter crossover frequency is suited accordingly.

$$v_L = R_L i_L + L\frac{di_L}{dt} \tag{2.22}$$

The required filtering is defined using a simple RC filter (first order), as in presented in Fig. 2.12. In the Laplace domain, the sensor output voltage v_{sensor}, is represented by

$$v_{sensor}(s) = (R_L + sL)\, I_L(s) \times \frac{1}{1 + sR_F C_F} = \frac{1 + \frac{s}{\frac{R_L}{L}}}{1 + \frac{s}{\frac{1}{R_F C_F}}} R_L I_L(s), \tag{2.23}$$

being R_F and C_F the resistor and capacitor value of the RC filter, respectively. The inductor voltage has AC and DC components. In the steady-state operation, the average value of the AC component is zero, and the DC component corresponds with the voltage drop in the internal resistor R_L.

Forcing $\frac{R_L}{L} = \frac{1}{R_F C_F}$ the zero and pole of (2.23) are canceled one each other, so sensor output voltage corresponds with the desired $R_L i_L$. Therefore, to use this technique, the value of L and R_L must be known. In this case, R_L varies with the temperature and L with the current value, being this method viable only for a custom designs these values are well-known. A trade off is needed between accuracy and bandwidth [113]; so if the bandwidth is too low,

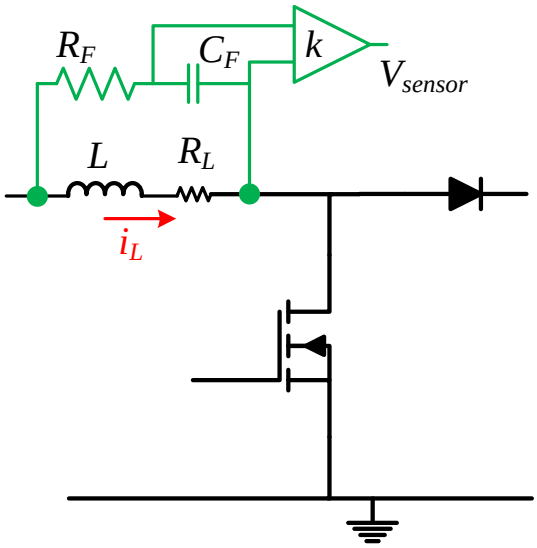


Figure 2.12: Sensing the inductor current by measuring the inductor voltage with a RC filter in a boost converter.

the accuracy is too low and the current data will not be useful for the current loop. This technique can be applied in applications where only the average value of the current is needed, like in the average current-mode control.

2.5.4 Current transformer sensor

Current transformer sensors provide two benefits in comparison with the previous techniques based on Ohm's law. The first one is the isolation between the control circuit and the power stage, and the second advantage is the lower power losses, but the cost is higher. The transformer allows a much higher signal level in the measurement data improving the signal-to-noise ratio in the control circuit.

Four different types of current transformers [108] are used: AC current transformers (ACCTs), unidirectional current transformers (UCTs), DC current transformers (DCCTs) and flyback-type current transformers (FBCTs). AC and Unidirectional CTs are the most commonly used, being used the DCCTs for high-current applications and FBCTs for high frequency pulsated currents.

Current transformers used in switched mode power supplies have typically a single turn in the primary side. A scheme of the current transformer equivalent circuit is shown in Fig. 2.13, with a turns ratio N, being i_p the current that must be measured, i_s the secondary side current and L_m the magnetizing inductance. The current i_s, through the load resistor R_s generates a magnetic flux, and is can be written as [107]:

$$i_s = \frac{i_p}{N} - \frac{1}{L_m}\int v_s dt \tag{2.24}$$

The transformer must be excited by the action of the magnetizing current. This current is given by the primary side and is subtracted by the secondary. A high magnetizing inductance

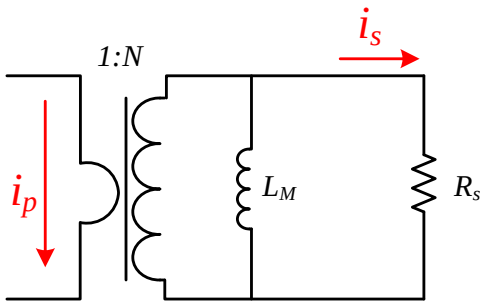


Figure 2.13: Current transformer equivalent circuit

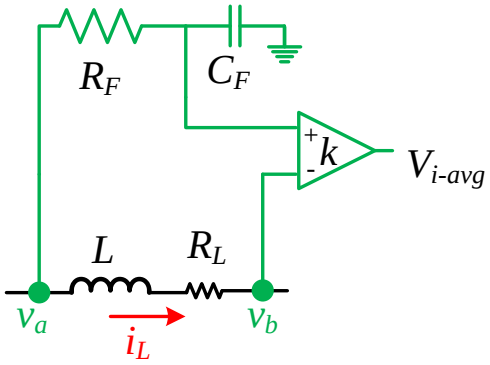


Figure 2.14: Averaging the inductor voltage to sense the current.

is needed (to obtain a low magnetizing current) [103]. Another additional requirements are flux density, low core loss with the typical goals of small size and cost.

Working at high frequencies, the integral term of Eq. (2.24) is small, being the secondary current proportional to i_s. This variable can be converted, with a resistor, in a voltage that does not need any amplification circuit and can be directly sampled by an analog-to-digital converter.

2.5.5 Current-average technique

The basic scheme of this technique is shown in Fig. 2.14. This technique is similar to the presented in Section 2.5.3, and filter the pulsated voltage in the junction of the power switches in the converter (v_a in the example of Fig. 2.14). The output voltage of the sensor is defined by expression (2.25), approximated and $V_{i-avg} \approx kR_L i_L$ at frequencies lower than the switching frequency ($R_F C_F \gg$ switching frequency). The advantages and the drawbacks of this technique are the same as the filter-sense inductor technique:

$$V_{i-avg} = k\left(v_a \frac{1}{1+C_F R_F s} - v_b\right) = k\left(\frac{v_b + (R_L + Ls)\, i_L}{1+C_F R_F s} - v_b\right) \approx kR_L i_L \qquad (2.25)$$

2.5.6 Hall-effect sensor

Hall-effect sensor is one of the most popular magnetic sensors. They are small, isolation and low power consumption, but with a high cost [107]. A current through a conductor, creates a magnetic field, and is a second conductor is placed into this magnetic field, at one edge of the conductor the density of conductive carrier is higher. With that, it results in a voltage potential proportional to the current that must be measured. Additional circuitry is needed in the Hall-effect sensor, and different configurations as open-loop Hall-effect sensing, closed-loop Hall-effect sensing, and combinations of open- and closed-loop Hall-effect sensing with a CT technique can be founded [106, 108]. This aspect increases the cost of this type of sensor, being no popular in PFC rectifiers.

2.5.7 Case study: Losses in a PFC stage with resistor current sensor

It has been addressed before, in a PFC Boost converter, a current resistor R_s is the most common solution adopted to measure the input current. Fig. 2.15 shows the boost converter scheme considering all the losses in the converter, highlighted in red the components that cause these losses, which can be divided in two types:

- Conduction losses originated by the current flowing through each element:

  - Losses in the inductor: $P_L = I_g^2 R_L$, I_g being the RMS value of the input current and R_L the inductor equivalent series resistance.
  - Losses in the current sensor: $P_S = I_g^2 R_s$.
  - Losses in the MOSFET: $P_Q = I_Q^2 R_{on}$, I_Q being the RMS value of the transistor current defined by (2.26), and R_{on} the MOSFET ON-state resistor [63].

$$I_Q = I_g \sqrt{1 - \frac{8}{3\pi} \frac{\sqrt{2} V_g}{V_o}} \tag{2.26}$$

  - Losses in the diode: $P_D = I_D^2 R_D + V_D I_D$, I_D being the RMS value of the diode current defined by (2.27), R_D the diode ON-state resistor and V_D the forward voltage at zero current [63].

$$I_D = \frac{V_o}{R} \sqrt{\frac{16}{3\pi} \frac{\sqrt{2} V_g}{V_o}} \tag{2.27}$$

    Hence, the total conduction losses are defined by :

$$P_{cond} = P_L + P_S + P_Q + P_D \tag{2.28}$$

- Switching losses generated in the ON-OFF transitions [63]: the energy dissipated due to the switching losses each switching period is given by the sum of the dissipated energy

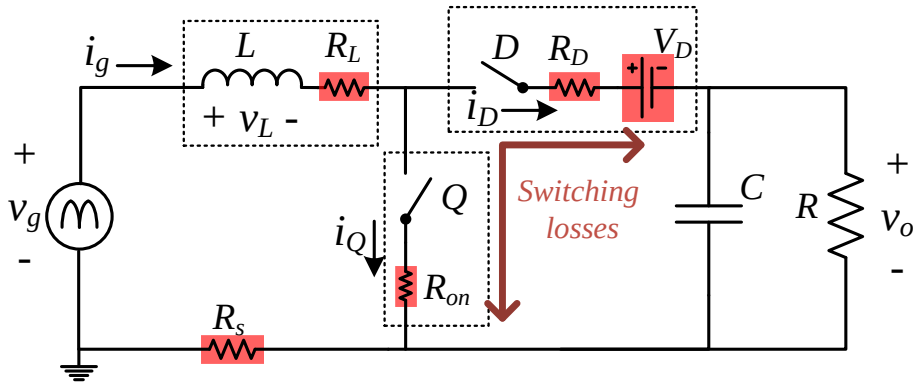


Figure 2.15: Boost PFC converter scheme considering losses.

each turn-OFF transition (e_{off}), and the energy dissipated each turn-ON transition during the rise time ($e_{on,rise}$) and due to the reverse recovery ($e_{on,rr}$). The expression that define these values are given by (2.29), (2.30), and (2.31).

$$e_{off} = \frac{1}{2}\left(i_g + \Delta i_g\right) V_o \left(t_{d,off} + t_f\right) \tag{2.29}$$

$$e_{on,rise} = \frac{1}{2}\left(i_g - \Delta i_g\right) V_o t_{rise} \tag{2.30}$$

$$e_{on.rr} = \left(\left(i_g - \Delta i_g\right) t_{rr} + Q_{rr}\right) V_o \tag{2.31}$$

where $t_{d,off}$, t_f, and t_{rise} are the turn-OFF delay time, the fall time and the rise time of the MOSFET, respectively. t_{rr} is the reverse recovery time of the diode, and Q_{rr} its reverse recovery charge. According to that, and neglecting the losses due to the parasitic capacitors, the total power dissipated each switching period p_{sw}, and the average power P_{sw}, are given by (2.32).

$$p_{sw} = \left(e_{off} + e_{on,rise} + e_{on.rr}\right) f_{sw};\ P_{sw} = \frac{1}{T_u}\int_0^{T_u} p_{sw} dt \tag{2.32}$$

Then, the total power dissipated in the Boost converter, is the addition of the conduction and the switching losses $P_{loss} = P_{sw} + P_{cond}$, and the theoretical efficiency of the converter:

$$\eta = \frac{P_o}{P_g} = \frac{P_g - P_{loss}}{P_g} = 1 - \frac{P_{loss}}{P_g} \tag{2.33}$$

Paying attention in Fig. (2.15), it can be seen how the current sensor is the only element of the converter that can be avoided in order to improve the efficiency. The switching frequency affects the value of the switching losses, but rest of the losses are inherent to the Boost operation. To evaluate the influence of the current sensor real values are going to be plug in the expressions presented before. Considering:

- $V_g = 230\ V_{rms}$, $V_o = 400$ Vdc, $L = 1$ mH, $f_{sw} = 75$-140 kHz, $R = 160\ \Omega$,

	P_S	P_{cond}	P_{sw}	η	P_S/P_{cond}	P_S/P_{loss}	η_{ssless}
75 kHz	3.98 W	13.56 W	13.65 W	97.3 %	29.34 %	14.62 %	97.7 %
100 kHz	4.02 W	13.66 W	18.54 W	96.9 %	29.45 %	12.49 %	97.3 %
140 kHz	4.08 W	13.82 W	26.44 W	96.1 %	29.57 %	10.15 %	96.5 %

Table 2.4: Theoretical power losses for different switching frequencies. Efficiencies with (η) and without (η_{ssles}) current sensor. And ratio between the current sensor losses (P_S), the conduction losses (P_{cond}) and total losses (P_{loss}).

- MOSFET IRFP27N60K: $t_{d,off} = 43$ ns, $t_f = 38$ ns, $t_{rise} = 60$ ns, $R_{on} = 180$ mΩ,
- Diode RHRP860 : $Q_{rr} = 56$ nC, $t_{rr} = 35$ ns, $V_D = 0.6$ V, $R_D = 200$ mΩ,
- Inductance : R_L= 250 mΩ,
- Current sensor : R_s= 200 mΩ.

The theoretical results are shown in Table 2.4 for different switching frequencies. The power losses in the current sensor (P_S) and the total conduction losses (P_{cond}) are almost constant, being the switching losses (P_{sw}) higher as the switching frequency increases. They are presented the percentage that represent P_S in the total conduction losses P_S/P_{cond}, and the total losses P_S/P_{loss}. The efficiency using current sensor (η) and the theoretical efficiency without it (η_{ssless}) are shown too.

It can be seen that without current sensor, the total efficiency increases around 0.5 %, representing the current sensor the 29 % of the conduction losses, and the 10-14 % of the total losses.

2.6 Digital power factor correction controllers with current sensor

Analog Average Current Mode (ACM), presented in Fig. 2.6, is one of the most prevalent analog solutions for CCM PFC rectifiers, being [114, 115] some examples of a digital implementation of the ACM relying on multiple current samples every switching period. Several current controllers implemented in a digital device can be found in the literature, but not only related with the quality of the input current, adding features or performances.

The capabilities of the digital devices are well suited for the implementation of nonlinear controllers. Digital signal processing enables the reduction of sensed variables and the design of more specific algorithms to improve the dynamic response and noise immunity. Illustrative examples can be found in [70,82] where samples are avoided in the switch transition to prevent the effect of the switching noise in the control circuit or in [44] where the controller requires the sampling of two variables: the output voltage and the average input current; being estimated the input voltage. Therefore, two ADC ICs are used in that approach. Leveraging the digital control capabilities, the average value of the sensed current is obtained in the MOSFET

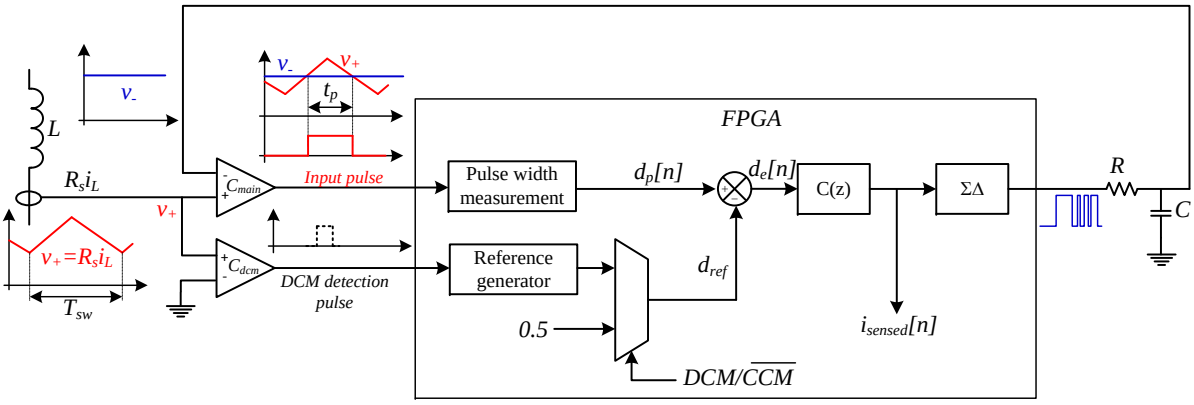


Figure 2.16: Average current sensor scheme.

terminal without low-pass filters in the loop, and synchronizing sampling and modulation, so that the current is always sampled in the middle of the ON-time. The current control is done in this case with a dead-beat controller. A modification is introduced in [96], where both measurements, the input current and the output voltage, are measured in the MOSFET terminals. The output voltage is measured with a small time delay after the turn-OFF time and synchronized at the line voltage peak, rejecting the low-frequency output voltage ripple.

In [98] the current controller is a digital nonlinear carrier (DNLC) PFC controller, based on a simple control law that allows CCM operation without input voltage sensing or estimation, becoming an US Patent in 2012 [116]. The current is sampled to in the middle of the ON-time or OFF-time too, and uses a single comparator for the output voltage sensing [117]. Improvements in the voltage dynamics are presented too in [118] where the output voltage sensor is substituted by a voltage estimation algorithm, with inherent cancellation of feedback voltage ripple. The diode current is used in [119] to compute the duty cycle without input voltage sensing.

The use of a feedforward control to improve the response in the current loop is introduced in [74], and digitally autotuning controllers perturbing the PFC current and voltage loops [120].

A sampling algorithm for digitally controlled Boost PFC Converters is presented in [121]. This algorithm, called "alternating-edge-sampling" (AES) present switching noise immunity, straightforwardness, accurate measurement of the average input current, and the need for only few processor cycles.

One of the most recent works about low cost current sensors for PFC converters is [10], where no ADC IC is used. The analog-to-digital conversions are done by the concepts presented in [122–124]. The architecture of the current proposed current sensor is shown in Fig. 2.16.

The instantaneous voltage of the current is represented by $v_+ = R_s i_L$, and it is compared with two signals. One of these, is the signal v_- which is compared by the comparator C_{main} whose output is called *Input pulse*. The signal v_- represents the analog value of the digital current data $i_{sensed}[n]$ (output data of the sensor) that in steady state represents the average value of $v_- \approx R_s \langle i_L \rangle$. In the comparator C_{dcm}, the signal v_+ is compared with 0 V. The

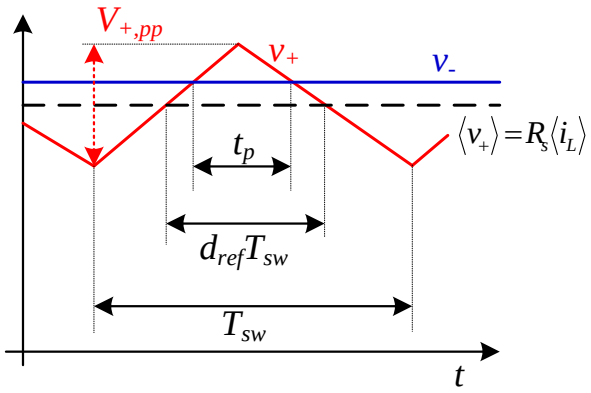


Figure 2.17: Operating waveforms of the average current sensor.

signal *Input pulse* has a pulse duration t_p, and then a duty cycle $d_p = {}^{t_P}/_{T_{sw}}$, which is measured in the digital device $d_p[n]$. With the feedback operation and the controller $C(z)$, it is forced $d_p[n]$ to equal d_{ref}. The signal d_{ref} is a reference chosen depending on the converter operation mode (for instance, if the converter operates in CCM then $d_{ref} = 0.5$).

The waveforms of the average current sensor presented in [10] are shown in Fig. 2.17. The goal of the controllers is to match the signal v_- with the real average value of the current sample $\langle v_+ \rangle = R_s \langle i_L \rangle$. With that, it is obtained:

$$d_p = \frac{t_p}{T_{sw}} = d_{ref} + \frac{\langle v_+ \rangle - v_-}{V_{+,pp}} \tag{2.34}$$

being $V_{+,pp}$ the current sample ripple amplitude. The block represented by "Pulse-Width Measurement" in Fig. 2.16 turns the output pulse duty cycle d_p into the digital signal $d_p[n]$. The error signal $d_e[n]$, generated by the subtraction of d_{ref} from $d_p[n]$, is the input of the loop compensator $C(z)$. The output of the compensator $i_{sensed}[n]$ is turned back by a digital-to-analog converter formed by a $\Sigma\Delta$ modulator and a RC low pass filter. The signal generated by the $\Sigma\Delta$ modulator is a bitstream whose average values is equal to the $i_{sensed}[n]$ input signal.

The same approach is used to obtain the input and output voltage data. The scheme of the voltage sensor is presented in Fig. 2.18. The voltage sample, represented by signal v_s is compared with the signal v_c by the comparator C_g. The signal v_c is, in this case, the result of a digital-to-analog conversion of $v^*[n]$, which represents the digital data of v_c. The output signal of C_g, called $Up/Down$ is a logic "1" if $v_c < v_s$, and a logic "0" if $v_c > v_s$ and is the input of the FPGA. The Up/Down counter block counts up 1 LSB if $Up/Down$ = "1" and counts down 1 LSB if $Up/Down$ = "0". In steady state the output value of this block represents the digital data of the input voltage, being the output of the voltage sensor. The signal $v^*[n]$ is turned back to the analog domain by the digital-to-analog converter formed by the $\Sigma\Delta$ modulator and the RC low pass filter. As in the current sensor, the signal generated by the $\Sigma\Delta$ modulator is a bitstream whose average value is equal to the $v^*[n]$.

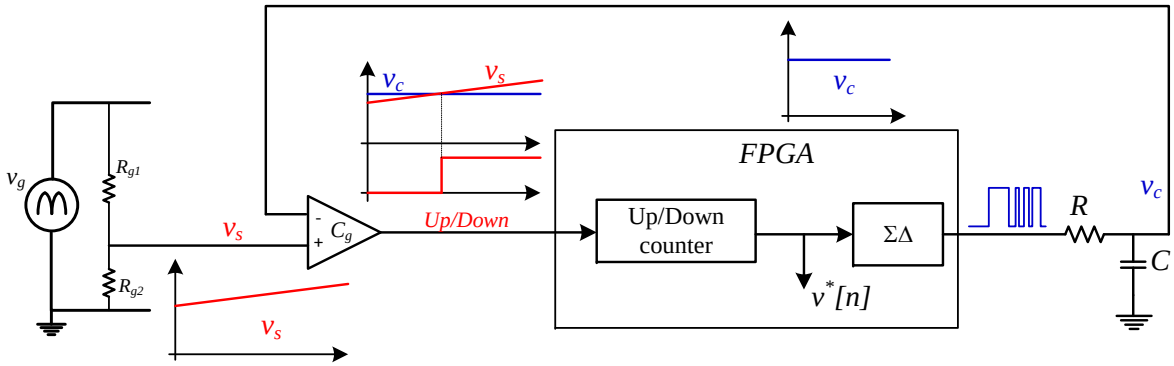


Figure 2.18: Voltage sensor approach used to obtain the digital data of the input and output voltages. Scheme for the input voltage.

So, with this proposal, in [10] the analog-to-digital conversion of the three variables (input voltage, input current and output voltage) is carried out without any discrete ADC chip, being an inexpensive solution. The main drawback of this approach is that the current sensor has a bandwidth limited by the compensator $C(z)$, that in turns limits the bandwidth of the current loop.

Another one recent solution of a PFC CCM rectifier controller without any type of ADC chip is presented in [11], based in [123, 125]. The line voltage zero crossings are detected by a isolated transformer and a zero crossing detector. The inductor current in sensed with a Hall sensor and the output voltage by a voltage divider, followed both by the sampling circuits presented in [11] to obtain the digital data of each variable. The sampling circuits are based on comparisons between the signals to be sample and sawtoothed waves, and digital counters which count the duty cycle of these comparisons. The sinusoidal current command is generated by the zero crossing detector and a sinusoid look-up table.

2.7 Digital power factor correction controllers without current sensor

In parallel with the idea of avoiding the input voltage measurement, or the instantaneous current values, or substitute the commercial ADC chips by low cost solutions based on comparisons and digital counters, several works have been done with the aim of presenting PFC controllers in with the input current (or inductor current) is not measured. It decreases the cost of the overall circuit cost, where the ADC IC is one of the most expensive elements, but furthermore (and maybe more interesting) simplifies the complexity of the control circuit and the design of the system.

In [126] the inductor current sensor is avoided, and it is replaced by a slower load current measurement. One of the first works about PFC rectifiers without any current sensor is [127]. In this work, the duty cycle command is a function of the input voltage value v_g and a function $\mathrm{d}|\sin\theta|/\mathrm{d}\theta$, where θ represents the phase angle in radians of v_g. In continuous conduction mode

(CCM) Boost PFC Controllers, the most recent works proposing current sensorless solutions are [12, 128–132].

In [128], only the AC line voltage is detected and used to generate the switching signal for the MOSFET. So, not only the DC output voltage sensor but also the AC current sensor can be removed in the control system, respectively. A Kalman filter approach to estimate the input current is presented in [129]. Several works presented by Hung-Chi Chen avoid the current loop using the Single-Loop Current Sensorless Control (SLCSC) for single-phase boost-type PFC rectifier. This controller is firstly presented in [130] as the Duty Phase Control (DPC) and presented as SLCSC in [12], where the duty cycle command is computed taking into consideration the parasitic elements. Its model and small-signal Analysis is presented in [131]. This controller type is programmed in the digital device measuring the values of the parasitic elements and considering them constant in the controller, and shows a good behavior under sinusoidal input voltages. A modification of the controller is presented in [132], where the input voltage is measured and the SLCSC is extended to work under distorted input voltages.

The idea of achieving power factor correction with a pre-calculated duty cycle for a line period in nominal conditions, and start applying these preprogrammed values at the half-line zero crossings is applied in [133–137]. In [133] no input voltage changes are considered and shows the control under voltage changes due to the load. A predictive duty-cycle is presented in [134], with an implementation in a DSP, where the duty cycle command of the next AC line period is computed measuring the input and output voltages, presenting limitations if the load changes. This controller is improved in [135] and implemented in an FPGA, reducing the cited limitations. However, to do that, the input current is measured.

With this strategy, the current measurement and the current loop are avoided too in [136]. In [137], the control method is based on the experimental acquisitions of the duty-cycle command for different load conditions using a current sensor. These experimental acquisitions are programmed in the digital device and used to control the converter without the need of current sensor.

2.8 Thesis Approach

In this Thesis, the input current measurement is substituted by an digital estimation in a digital device (in this case an FPGA) using as information the input and output voltage data, and the drain-to-source voltage. The variable volt-seconds (vs_L) across the inductor is estimated in each switching period, and the small error (current estimation error) accumulated per switching period over the half line cycle causes current distortion.

All the sensorless controllers mentioned in Section 2.7, high power factor value and low THD of the input current are achieved in the voltage and power ranges presented for each reference in Fig. 2.19 (according to the experimental results presented in each work). Furthermore, the influence of the parasitic elements and the effects of the nonidealities are not analyzed in

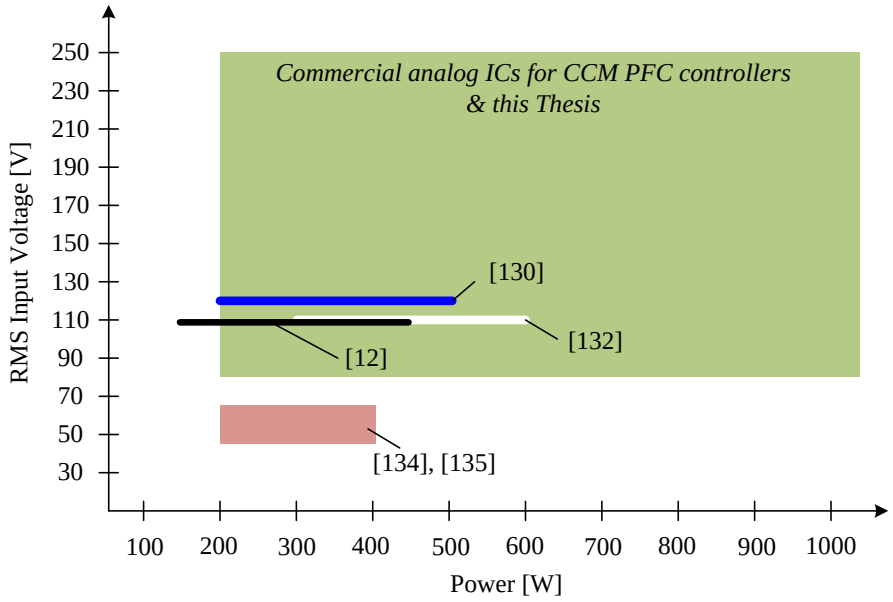


Figure 2.19: Input voltage and power range of the recent works in sensorless PFC controllers. The green area represents the goal of this Thesis.

detail. The green area represents the goal of this Thesis, that corresponds with the typical range of the commercial ICs [138] for CCM PFC controllers (universal input voltage range and wide output power range).

The objectives of this work are to:

- Study and model the influence of the different sources of current estimation error: drive signal delays, parasitic elements, and errors in the voltage acquisition data.
- Present a fast and coarse feedforward control to compensate automatically the effect of the switching delays, measuring them every switching period.
- Propose a fine low frequency feedback control, with high resolution, to compensate automatically the current estimation error.
- Present a modification in the nonlinear-carrier (NLC) control to obtain a pure sinusoidal current under a distorted input voltage.

With these goals achieved, an universal digital controller for Boost CCM power factor correction stages based on rebuilding concept is done. The term "universal" is used because with the fine resolution low frequency feedback loop, the digital controller compensates the estimation error which are sensitive to the input voltage specifications and power conversion rate. Therefore, the digital controller extends the operation range in comparison with the previous solutions presented in sensorless Boost CCM PFC controllers. The behavior under different input voltage frequencies is presented too, showing how a low THDi is achieved despite the distortion in the input voltage.

Chapter 3

Current estimation. Current control algorithm and errors

In this Chapter, it is presented the concept of current rebuilding/estimation of the inductor current and the current estimation error caused by the different sinks of error like delays, tolerances of the analog components and non-linearities. Firstly, the current rebuilding concept is presented as theoretical concept, an Simulink® blocks are used to define, mathematically, the different current estimation errors. All the errors are modeled, obtaining the expressions that define the current estimation error value in each case.

3.1 Current rebuilding. Theoretical concept.

Current rebuilding approach is first time presented in [139], as an observer which provides the operating benefits in the current mode control without current sensing, denominated as Sensorless Current Mode (SCM). This control uses state information from the converter and reconstruct and inductor current from voltage information. In this work, the rebuilding technique is applied in low voltage DC-DC power converters used in computer power supplies. The measurements of the voltage forward drop across the active switch when it is ON, and the input voltage are needed; and for the DC output, a fixed reference value is used, replacing the measurement of the real output voltage. The inductance voltage is function if these variables, and with its integration a proportional value of the inductor current is obtained.

The approach of this work is based on this idea, but applied to boost PFC controllers. This PFC topology is connected to the utility mains (120 - 230 V_{rms}) and the output voltage is higher (around 400 V_{dc}), so the measurement of the active switch voltage is complicated because is a pulsated voltage with low value around 1 V (ON-state), but during OFF-state it is equal to the output voltage.

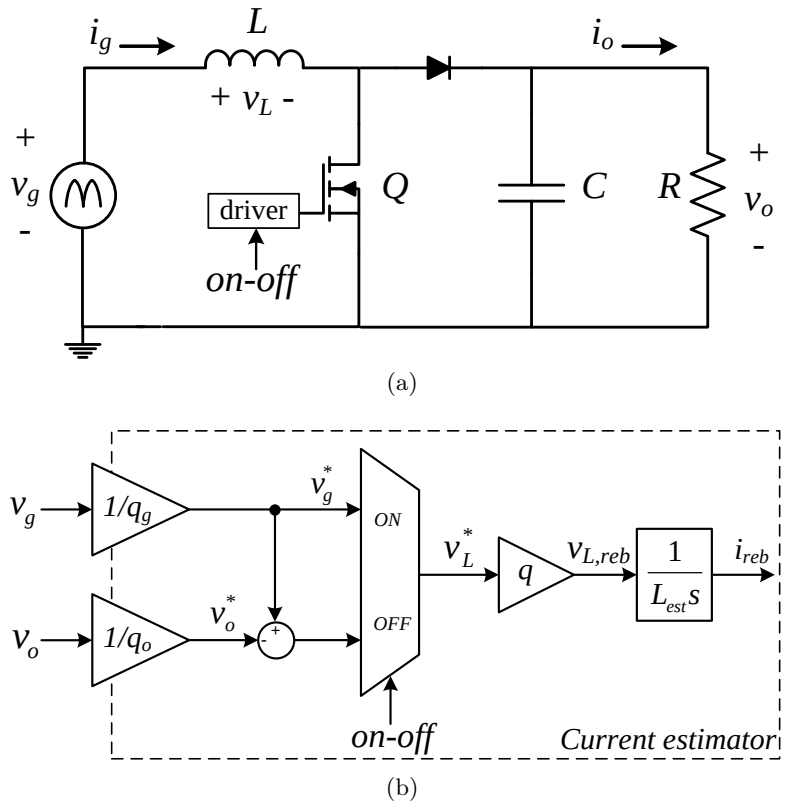


Figure 3.1: (a) Boost converter basic scheme and (b) basic simulation model of the sensorless Boost PFC converter current estimator.

Figure 3.1 shows a boost converter (Fig. 3.1a) and the first approach of the current estimator simulation model (Fig. 3.1b), which represents the behavioral model of the boost converter shown above. In the power converter, input and output voltages (v_g and v_o) are applied across the inductor terminals, and define the value of the real input current i_g, so they have to be measured and quantized to estimate the current in the digital circuit. Digital input and output voltage data, v_g^* and v_o^* respectively, have a LSB (low significant bit) resolution (expressed in Volts per bit) represented by q_g and q_o, respectively, and given by (3.1):

$$q_g = \frac{v_g}{v_g^*}\left(\frac{V}{bit}\right);\ q_o = \frac{v_o}{v_o^*}\left(\frac{V}{bit}\right) \tag{3.1}$$

The inductor voltage (v_L) is defined by the power converter state (ON- or OFF-state), being emulated in the current estimator by the signal $on-off$ which drives the power switch (Q) giving a digital estimated inductor voltage v_L^*, expressed in bits, and a rebuilt inductor voltage $v_{L,reb}$, expressed in volts. Ideally, The ON- and OFF-times are known within the controller because the driving signal is generated there. The value of q represents the LSB resolution defined by the designer. Ideally, $q = q_g = q_o$, but a real analog-to-digital conversion causes a small difference between them:

$$q_g = q(1-\varepsilon_g), \quad q_o = q(1-\varepsilon_o) \tag{3.2}$$

From (3.2), ε_g and ε_o are the percentage error of the input and output analog-to-digital conversions, respectively.

In the Laplace domain, the inductance represents an integrator with a gain equal to the inverse of the inductance value. Theoretically, the inductance L, is known; but temperature, switching frequency, inductor current and the core material cause a difference between the estimated inductance (L_{est}) and the real one. The estimated value is used in the current estimation algorithm. The integrator output corresponds to the digitally estimated current i_{reb}, expressed in the same units than i_g (i.e. amps).

Expressions (3.3) and (3.4) define the instant values for the real and estimated current, respectively. Assuming an ideal converter without parasitic elements, $v_L = v_g$ during ON-state and $v_L = v_g - v_o$ during OFF-state. Parasitic elements have an important influence in the sensorless controller, as it is shown in Chapter 4, but expressions are now presented without them to simplify the comprehension. Under ideal conditions, with $q_g = q_o = q$, and $on - off$ signal defining the same converter stage than v_L over the time (i.e. no drive signal delays), $i_{reb} = i_g$ and no current error is caused.

$$i_g = \begin{cases} \frac{v_g}{sL} & if \quad ON - state \\ \frac{v_g - v_o}{sL} & if \quad OFF - state \end{cases} \tag{3.3}$$

$$i_{reb} = \begin{cases} \frac{v_g}{sL}\frac{q}{q_g} \times \frac{L}{L_{est}} & if \quad on - off = 1 \\ \left(\frac{v_g}{sL}\frac{q}{q_g} - \frac{v_o}{sL}\frac{q}{q_o}\right) \times \frac{L}{L_{est}} & if \quad on - off = 0 \end{cases} \tag{3.4}$$

Once the input current is rebuilt i_{reb}, any current loop can be used: average current, peak-current, hysteretic control, etc. The input current control loop shapes the rebuilt current i_{reb}, while the output voltage control loop generates the current reference i_{ref}, for the utility period as is depicted in the block diagram presented in Fig. 3.2.

In this proposal, nonlinear-carrier (NLC) controller is used [15, 17], presented in detail in Section 3.2, which has the advantage of using constant switching frequency that can be easily implemented in digital hardware, because it is based on additions and comparisons.

The simulation block presented in Fig. 3.1 has been done in MATLAB®/Simulink® and PLECS® (Piecewise Linear Electrical Simulation), making possible to model and simulate electrical systems along with their controls. In this work, only the switching converter has been modeled with PLECS®, the simulation control algorithm has been develop completely in Simulink®. Recent works of Hardware in the Loop (HIL) or different simulation tools has been presented [29,140]. In the most of the commercial simulation programs, switches are modeled as nonlinear elements that need small time integration steps for simulation; and is not easy to simulate at the same time the digital control and the power converter. In this case, switches are considered ideal (ON- or OFF-state) [141]. In addition, in MATLAB®/Simulink® and PLECS®, it is possible to determinate loop gains directly with a perturbation injection in

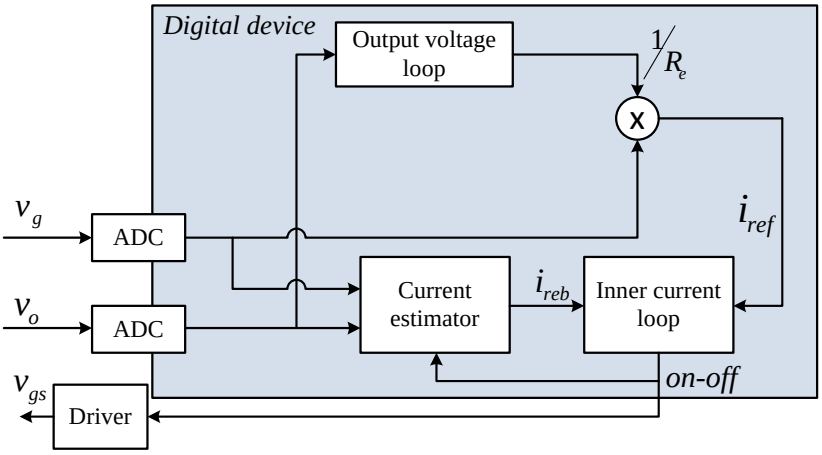


Figure 3.2: Schematic of the sensorless current controller.

any point of the switching converter using the different analysis tools [142].

This converter simulation model, connected in Simulink® to the sensorless current controller (as is presented in Fig. 3.3) is used in the next sections of this Chapter 3 to show the current estimation error that appears due to the real implementation of the proposed converter and controller, like component tolerances, inherited non-linearities, component delays.., and compares it with the obtained mathematical expressions of the current estimation error, that model the sensorless controller behavior. Errors caused due to quantization effects and the digital implementation of the controller approach are presented in Chapter 5.

3.2 Power factor correction algorithm. Non-linear carrier (NLC) control

This control approach was presented in [15] in high power boost power factor correction stages and it is American patent since 1999 [143]. Later, the same controller is modified to be applied in up-down switching converters [64] and modeled in [144]. These non-linear carrier controllers achieve power factor correction in continuous conduction mode (CCM). Many authors have presented several approaches of non-linear controls applied to switched mode power supplies, and all of them are based in a comparison of a carrier signal with the variable under control. The not use of the analog multiplier and a control based on comparison make this type of control easy to be implemented in a digital device.

In [18], *One-cycle control* (OCC) technique is presented for a buck converter, but it can be directly applicable to pulse-width-modulated, resonant based, soft-switched switching converters, inverters and rectifiers, for either voltage or current control in continuous or discontinuous conduction mode. It proposes a control of the duty cycle command of the switch such that in each switching cycle the average value of a switched variable of the converter is exactly equal to (or proportional to) the control reference in steady state or in a transient. This control is an American patent since 1994 [145].

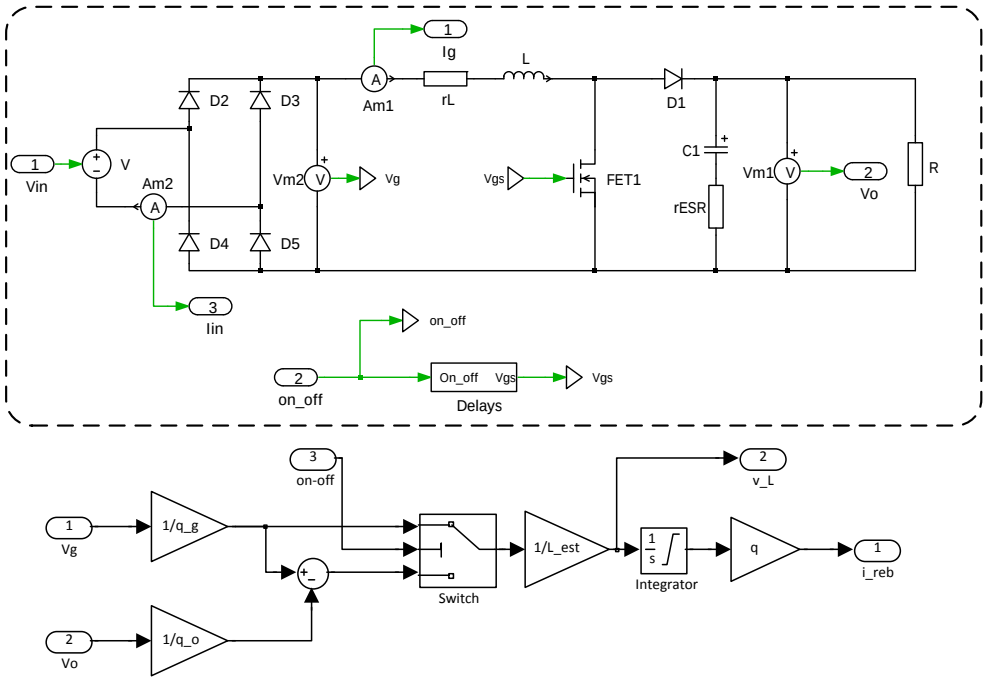


Figure 3.3: Simulations Blocks in Simulink® with PLECS® toolbox. Top: PLECS® subcircuit in Simulink® with the switching delays (explained in Section 3.3.1). Bottom: Current estimator Simulink blocks.

Another technique similar to NLC control is presented in [146], as the name of *Linear peak current mode control* (LPCMC). In [147], non-linear control approach is used to achieve a general PWM control for several converters, and in [17] is applied specifically for power factor correction stages. This technique applied for a boost converter as power factor correction stage, with the name of OCC, is presented in [16]. *Voltage-controlled compensation ramp* (VCCR) is presented in [148], being a similar approach than OCC with differences about the update of the carrier signal amplitude.

Non-linear carrier control approach is applied in this Thesis. In a boost rectifies, the first goal of the controller is to keep the low-frequency portion of the input current proportional to the input full-wave rectified utility voltage,

$$\langle i_g \rangle = \frac{v_g}{R_e}, \tag{3.5}$$

where R_e represents and the emulated resistance of the PFC stage viewed by the grid. The second goal of the rectifier is to keep the output voltage v_o, constant at a specified reference level, $V_o = V_{ref}$.

When the converter operates in CCM, the ideal quasi-steady-state conversion characteristic is given by Eq. (3.6), neglecting the output voltage ripple $\triangle v_o$, so $v_o \simeq \langle v_o \rangle_{T_u} = V_o$.

$$v_g = (1 - d)\, V_o \tag{3.6}$$

With Eq. (3.6), v_g can be eliminated from (3.5), and the duty cycle command $d = t_{on}/T_{sw}$,

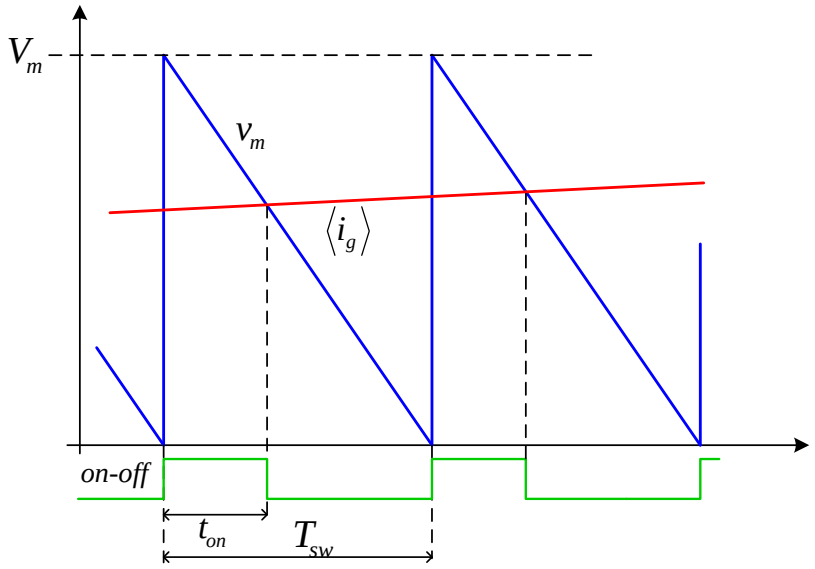


Figure 3.4: NLC control waveforms.

so (3.5) can be expressed as:

$$\langle i_g \rangle = \frac{V_o}{R_e}(1-d) = \frac{V_o}{R_e}\left(1 - \frac{t_{on}}{T_{sw}}\right) \tag{3.7}$$

Non-linear carrier (NLC) control is based on expression (3.7), trying to define the duty cycle that satisfies it. To do that, the average value of the input current each switching period $\langle i_g \rangle$, is compared with a triangular carrier waveform v_m, periodical with a frequency equal to the switching frequency f_{sw}, whose value is given by (3.8). The comparison of the two variables, according to the Fig. 3.4, generates the MOSFET drive signal v_{gs} .

$$v_m = V_m\left(1 - \frac{t}{T_{sw}}\right), \; with \; 0 \leq t \leq T_{sw} \tag{3.8}$$

In the Sensorless control approach, the measurement of the real input current i_g, is replaced by the rebuilt current i_{reb} and is compared with the carrier signal v_m, as it is shown in Fig. 3.5. The carrier waveform v_m, has an amplitude V_m proportional to the demanded power P_g, and, therefore function of the emulated resistance R_e .

$$V_m = R_s\frac{V_o}{R_e} = R_s\frac{V_o}{V_g^2}P_g, \tag{3.9}$$

being V_g the RMS value of the input voltage, and R_s the value of the current sensor (fictitious in the sensorless approach, $R_s = 1\Omega$). To achieve the goal of a current proportional to the input voltage, as is presented in Eq. (3.5), the emulated resistance R_e has to be constant, at least over the line cycle (50 - 60 Hz). So a slowly-varying V_m is used in the voltage loop in order to assure the output voltage value under load and input voltage variations.

In the analog approach, is it difficult to calculate the average value of the input current in a switching period $\langle i_g \rangle$, before the end of the switching cycle, so second order carrier signals

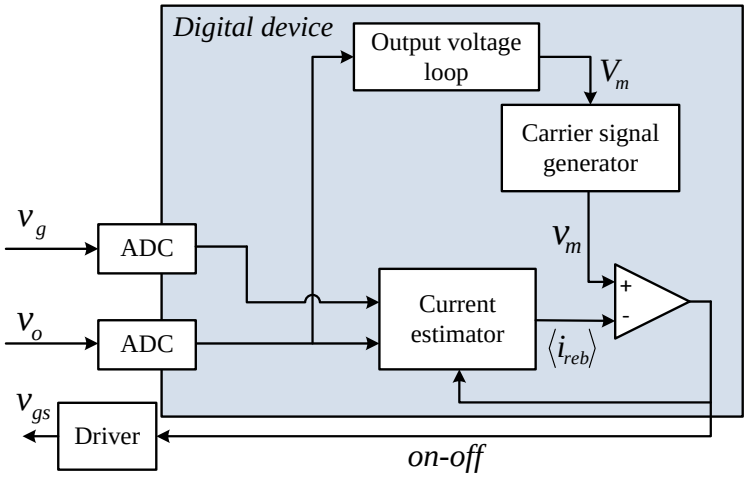


Figure 3.5: Schematic of the sensorless current controller with a NLC control.

are used to compensate this aspect, as is shown in [15] for boost converters and in [64] for other up-down topologies. With a digital value of the current it is possible to approximate the average rebuilt current $\langle i_{reb} \rangle$, with a small error.

In this work, the instantaneous values of the estimated input current is labeled in two "dimensions" as $i_{reb}[j,k]$, where j represents the switching period and k the clock period in this j^{th} switching period. Therefore, k takes values from zero to $\frac{f_{clk}}{f_{sw}} - 1$, at the beginning of the switching period as $i_{reb}[j,0]$, and $i_{reb}\left[j, \frac{f_{clk}}{f_{sw}} - 1\right]$ at the end of the same switching period, respectively. To simplify the notation in the equations, $i_{reb}\left[j, \frac{f_{clk}}{f_{sw}} - 1\right]$ is labeled as $i_{reb}^{-}[j]$.

With this, the valley value of the digitally rebuilt current in the switching cycle j is known at the beginning of each switching period, $i_{reb}[j,0]$ (that corresponds with $i_{reb}\left[j-1, \frac{f_{clk}}{f_{sw}} - 1\right]$); and the current rebuilding algorithm estimates the current value each clock period k, labeled as $i_{reb}[j,k]$. Every switching cycle, the controller computes the average value of these two signals, according to Eq. (3.10), labeled as $i_{avg}[j,k]$, compared every clock cycle with the digital carrier signal $v_m[k]$.

Figure 3.6 represents the digital waveforms of the sensorless NLC control, and the block diagram of the $i_{avg}[j,k]$ computation. When the ON-to-OFF condition occurs, $i_{avg}[j,k]$ variable is not updated, keeping i_{avg} constant with a value higher than the carrier signal, until the end of the switching cycle . This constant value is also labeled as $i_{avg}[j]$, because represents the approximation of the average current in the j^{th} switching period, given by (3.11) where $d[j]$ represents the duty cycle of the drive signal in the actual switching period j, and $n_{clk} = f_{clk}/f_{sw}$ represents the number of clock cycles in a switching period.

$$i_{avg}[j,k] = \frac{i_{reb}[j,0] + i_{reb}[j,k]}{2} \tag{3.10}$$

$$i_{avg}[j] = \frac{i_{reb}[j,0] + i_{reb}[j,d[j]n_{clk}]}{2} \approx \langle i_{reb} \rangle \tag{3.11}$$

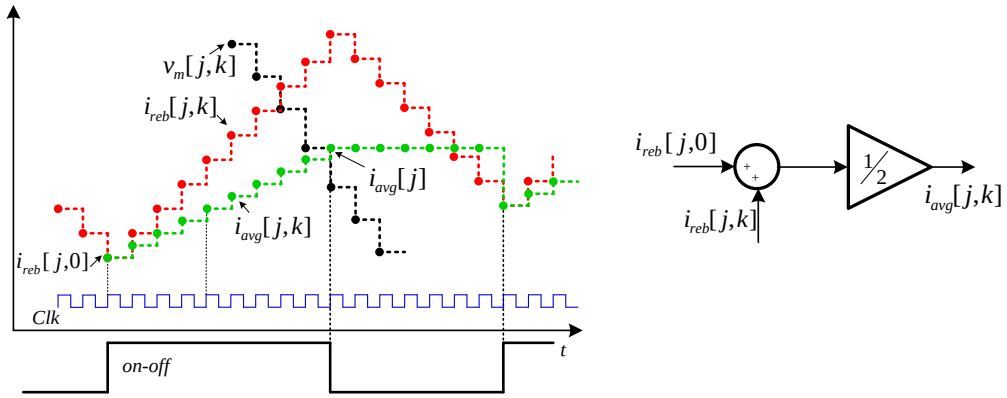


Figure 3.6: Left: Digital waveforms of the NLC control with estimation of the average rebuilt current. Right: Hardware implementation blocks of the average rebuilt current estimation.

NLC controller approach is based on CCM condition assumption, defined by Eq. (3.6), but it is not fulfilled in DCM condition so the resulting input current does not follow a shape proportional to the input voltage and a current distortion is caused by the operation in the DCM. In the discontinuous conduction mode, the current drops to zero at the end of the switching cycle, so $i_{reb}[j,0] = 0$, and $i_{avg}[j]$ is given by:

$$i_{avg}[j] = \frac{v_g[j]}{2L} t_{on}[j] \tag{3.12}$$

and the duty-cycle command is given by Eq. (3.13) and $d[j]$ can be solved according to

$$i_{avg}[j] = \frac{v_g[j]}{2L} d[j] T_{sw} = \frac{V_o}{R_e}(1 - d[j]) \tag{3.13}$$

$$d[j] = \frac{1}{1 + \frac{R_e}{R}\frac{1}{K}\frac{v_g[j]}{V_o}} \tag{3.14}$$

being R the load resistor and $K = 2Lf_{sw}/R$ is the load parameter commonly used in DCM analysis [63]. Boost PFC converter operates in DCM if

$$d[j] < 1 - \frac{v_g[j]}{V_o} \tag{3.15}$$

Working with expressions (3.13) and (3.14), it is possible to define the expression for the rebuilt input current i_{reb} when the converter operates in the DCM, given by (3.16) according to [15]. It can be seen how the average current in DCM is based from the ideal current $i_{avg}[j] = v_g[j]/R_e$, with a distortion factor :

$$i_{avg}^{DCM}[j] = \frac{v_g[j]}{R_e} \times \frac{R_e}{R}\frac{1}{K}\frac{1}{1 - \frac{v_g[j]}{V_o}}\frac{1}{\left(1 + \frac{R_e}{R}\frac{1}{K}\frac{v_g[j]}{V_o}\right)^2} \tag{3.16}$$

In Fig. 3.7 the current waveforms of the NLC controller are plotted, when a portion of the

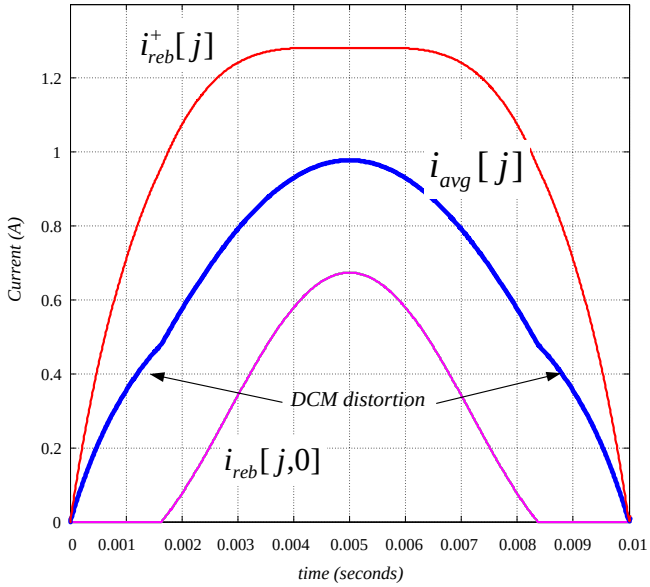


Figure 3.7: Half cycle of the input rebuilt current with distortion due to DCM operation around line zero crossings.

line period the converter is operating in the DCM. During this time, $i_{avg} = i_{avg}^{DCM}$, and the rest of the time, $i_{avg} = v_g/R_e$. The distortion due to this DCM conditions is analyzed deeply in [15, 146]. In the figure, $i_{reb}\,[j, d[j]n_{clk}]$ represents the peak value of the rebuilt current in each switching period j, represents also as $i^{+}_{reb}[j]$. These waveforms are typical when the converter operates at light load.

3.3 Current estimation errors. Boost Converter

Table 3.1a shows the correspondence between the analog variables (real variables in the converter) and their corresponding digitally estimation expressed in the same units. And all of these variables define the value of the real and the estimated input current according to the expressions presented in Table 3.1b, where Δi_g and Δi_{reb} represents the current ripple of the real and rebuilt input current, respectively. The instantaneous value of i_g is given by v_g and v_o voltages, the inductor value (L) and the ON-time (t_{on}) in the power converter. On the other hand, i_{reb} is estimated with the digital voltage values (v_g^* and v_o^*), the estimated value of the inductance (L_{est}) and the ON-time defined by the NLC controller in the digital device (t_{on}^*).

If analog and digital variables (Table 3.1a) are equivalent $v_g = v_g^* q$, $v_o = v_o^* q$, $q_g = q_o = q$, $L = L_{est}$, and $t_{on} = t_{on}^*$, both currents are matched $i_{reb} = i_g$, and the waveforms look like the ones presented in Fig. 3.8. In this situation, there is not current estimation error, defined as the difference between i_g and i_{reb}, expressed in amps by $i_{error} = i_g - i_{reb} = 0$, and therefore i_{reb} corresponds with an accurate quantization of i_g. At the beginning of the half line cycle, it is fulfilled that $i_g = i_{reb} = 0$. Since the input current is not measured, these line zero crossings are the only points where real current is known.

		Real	Estimated	Units
Inductor voltage	ON	$v_L = v_g$	$v_{L,reb} = \frac{v_g q}{q_g}$	[V]
	OFF	$v_L = v_g - v_o$	$v_{L,reb} = \left(\frac{v_g}{q_g} - \frac{v_o}{q_o}\right) q$	[V]
Inductance value		L	L_{est}	[mH]
ON-time		t_{on}	t^*_{on}	[seconds]
Input current		i_g	i_{reb}	[A]

(a)

	ON-state	OFF-state
Real input current (i_g [A])	$\Delta i_g = \frac{v_g}{L} t_{on}$	$\Delta i_g = \frac{v_g - v_o}{L} (T_{sw} - t_{on})$
Rebuilt input current (i_{reb} [A])	$\Delta i_{reb} = \frac{v^*_g q}{L_{est}} t^*_{on}$	$\Delta i_{reb} = \frac{(v^*_g - v^*_g) q}{L_{est}} (T_{sw} - t^*_{on})$

(b)

Table 3.1: (a) List of correspondence between of the analog variables and the digital. (b) Expressions that define the variation of the real and rebuilt input current in a switching period

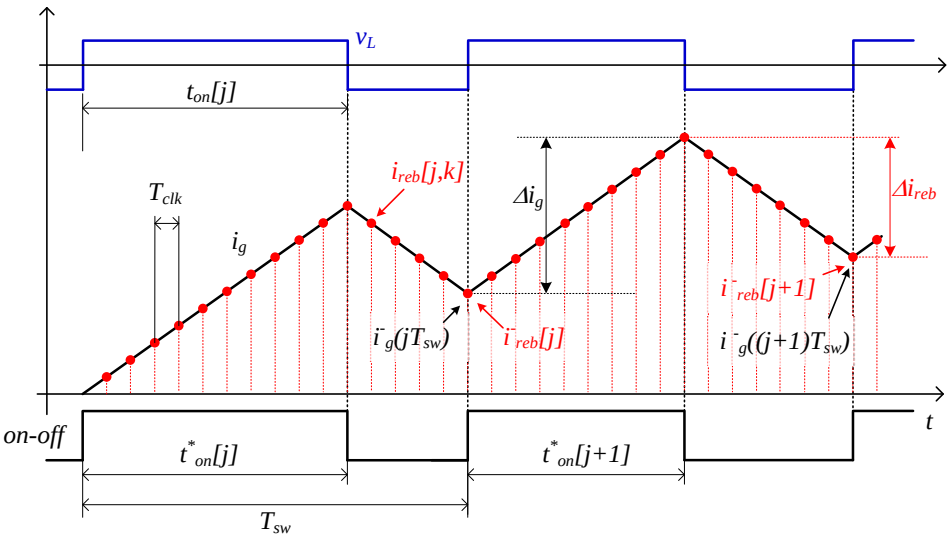


Figure 3.8: Digital signal $i_{reb}[j,k]$, compared with the analog real input current i_g, under ideal conditions. The $on-off$ signal is the output of the digital device and v_L the analog inductor voltage.

Small errors in the digital variables compared with the analog (Table 3.1a) causes a current estimation error in each switching period j. Therefore, the input current i_g, does not grow as is required and calculated by i_{reb}, and the current estimation error is accumulated over the half-line cycle. Main current estimation errors (i.e. inductance volt-seconds vs_L,) causes an input current distortion due to:

- the drive signals' delays ($t_{on} \neq t^*_{on}$),
- the difference between the estimated inductance (L_{est}) value and the real one (L), ($L \neq L_{est}$), and
- voltage data errors due to the tolerances of the voltage dividers, quantization process or nonidealities on the ADC ($v_g \neq v^*_g q$ and/or $v_o \neq v^*_o q$ and/or $q_q \neq q_o \neq q$).

All of these errors are described separately in this section, showing the current estimation error caused by these three different situations. To better illustrate the influence of these factors in the real input current waveform and in the complete behavior of the system, real values for the controller and power converter components are given, with nominal input voltage $V_g = 230\,V_{rms}$, a desired output voltage $V_o = 400\,V_{dc}$, to supply power an output power of $P_o = 640\,W$ ($R = 250\,\Omega$). The switching frequency of the system has been settled in $f_{sw} = 100\,kHz$, with reactive components $L = 1\,mH$, and $C = 220\,\mu F$. Under ideal condition, with $v_g = v^*_g q$, $v_o = v^*_o q$, $L = L_{est}$, and $t_{on} = t^*_{on}$, no current estimation error is caused and the carrier signal peak value V_m, is given by (3.9), corresponding with $V_m =$ 4.84 V. Simulated waveforms under these conditions are shown in Fig. 3.9, where i_g and i_{reb} are matched and the V_m signal given by voltage outer loop is around the theoretical value. To compare the different simulations presented in this Chapter, some important values are shown: the ratio between the RMS values of the rebuilt input current and the real one I_{reb}/I_g, the steady state value of V_m signal, the expected total harmonic distortion of i_g ($THDi$) and power factor value. Under ideal conditions, unit power factor value ($PF = 1$) is achieved with $THDi = 0\%$, and no current error estimation ($I_{reb}/I_g = 1$) .

3.3.1 Time error effect. Delays between the drive signal, output of the digital device, and the voltage across the inductor

Switching delays, caused by the MOSFET driver and the MOSFET device, cause a difference between the output drive signal of the digital device $on - off$, and the inductance voltage v_L, in each switching cycle. It is shown in Fig. 3.10 when Δt_{on-off} and Δt_{off-on} represent the ON-to-OFF delay and the OFF-to-ON delay, respectively. Figure 3.11 shows these delays when the PFC converter is operating with a IRFP27N60K Power MOSFET of Fairchild which is driven by a optocoupled driver of Avago HCPL3120.

In this case, $\Delta t_{on-off} \neq \Delta t_{off-on}$, represents the most critical error due to the difference between the ON-to-OFF delay (Δt_{on-off}) and the OFF-to-ON delay (Δt_{off-on}). It can

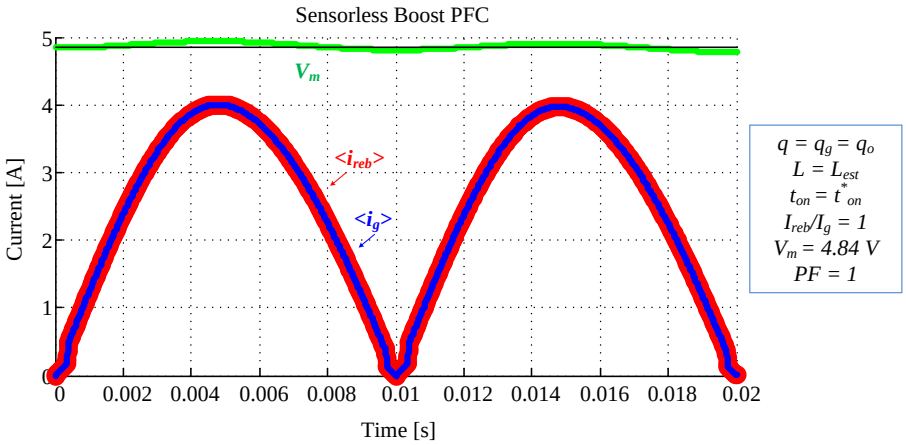


Figure 3.9: Simulated waveforms under ideal conditions obtained with the Simulink model of the system with $V_g = 230\,V_{rms}$, $V_o = 400\,V_{dc}$, $P_g \simeq P_o = 640\,W$ $(R = 250\,\Omega)$, $f_{sw} = 100\,kHz$ and reactive components $L = 1\,mH$, and $C = 220\,\mu F$, under ideal conditions.

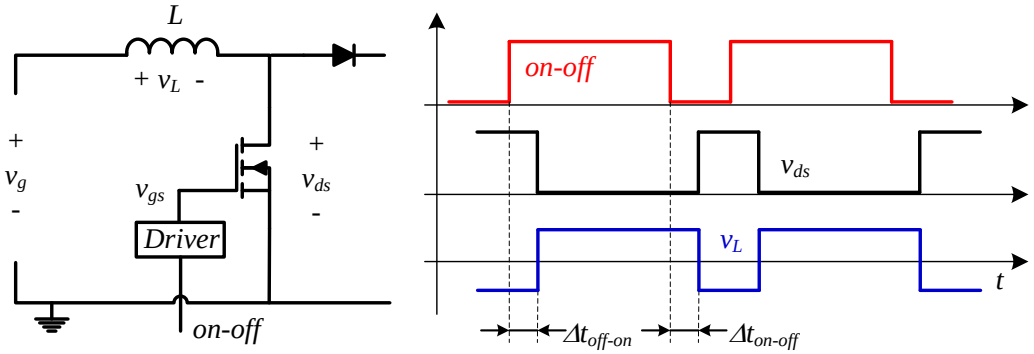


Figure 3.10: Boost converter circuit and gate drive signal vs MOSFET v_{ds} and inductor voltage to show the switching delays.

be described as the addition of two different causes: a duty-cycle modification (ON-time modification in each switching period) and a switching period displacement. The duty-cycle modification is explained previously, defining $\Delta t_{on}\,[j]$ as the ON-time modification due the switching delays and given by:

$$\Delta t_{on}\,[j] = \Delta t_{on-off}\,[j] - \Delta t_{off-on}\,[j] = t_{on}\,[j] - t^*_{on}\,[j] \tag{3.17}$$

A positive value of Δt_{on} represents an effective duty-cycle applied to the real converter input current t_{on}, higher than the used to estimate the input current t^*_{on}, and vice-versa. In [149] the influence of these delays in multiphase voltage regulation modules (VRM) is described.

The real input current i_g, is computed according to the v_L signal, and the rebuilt input current i_{reb}, according to the $on-off$ signal. This situation is presented in Fig. 3.12 for the switching periods j and $j+1$. In this case, the situation in the overall system with $v_g = v^*_g q$, $v_o = v^*_o q$, $q_g = q_o = q$, $L = L_{est}$ and $t_{on} \neq t^*_{on}$ is considered. This small error in the duty cycle causes a small estimation error every switching period. The nature of this controller,

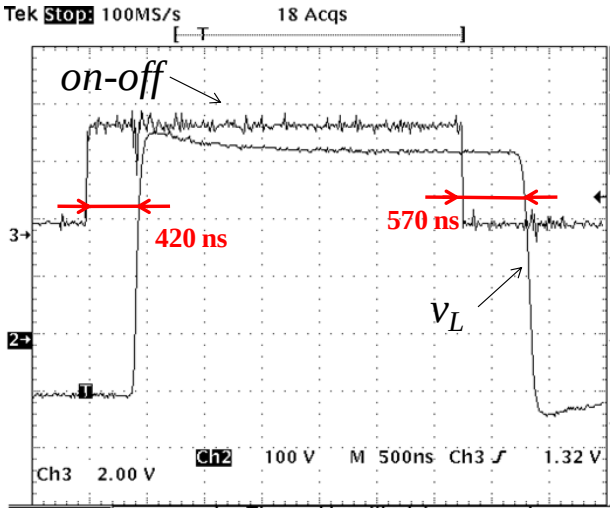


Figure 3.11: Experimental time switch transitions (v_L) compared with the output drive signal of the digital device ($on - off$).

without measurement of the real current, makes this error unknown by the controller, so it is not corrected in the next switching periods, being accumulated over the half line cycle. Line zero crossing are the only points where the controller knows that $i_g = 0$, and the error is reset $i_{error} = 0$.

The current estimation error i_{error} is defined as the difference between the real and the estimated input current $i_{error} = i_g - i_{reb}$. The evaluation of the current estimation error is carried out at the end of every switching period j, not using the index k that defines the clock period, simplifying the comprehension. Therefore the current error is given by (3.18), and each term of this expression is given by (3.19) and (3.20), respectively; being $i_g^- (jT_{sw})$ the valley value of the real input current at the end of the switching period j. To simplify the notation, $i_{reb}[j, n_{clk} - 1]$ is represented by $i_{reb}^-[j]$. The switching frequency is much higher than the utility frequency $f_{sw} \gg f_u$, so v_g and v_o are considered constant over the switching period j as $v_g[j]$ and $v_o[j]$:

$$i_{error}[j] = i_g^- (jT_{sw}) - i_{reb}^-[j] \tag{3.18}$$

$$i_g^- (jT_{sw}) = i_g^- ((j-1)T_{sw}) + \frac{v_g[j]}{L}(t_{on}^*[j] + \Delta t_{on}[j]) + \\ + \frac{v_g[j] - v_o[j]}{L}(T_{sw} - t_{on}^*[j] - \Delta t_{on}[j]) \tag{3.19}$$

$$i_{reb}^-[j] = i_{reb}^-[j-1] + \frac{v_g[j]}{L} t_{on}^*[j] + \frac{v_g[j] - v_o[j]}{L}(T_{sw} - t_{on}^*[j]) \tag{3.20}$$

Therefore, the error $i_{error}[j]$ accumulated over n switching periods ($i_{error}[n]$) and is given by:

$$i_{error}[n] = i_{error}[j-1] + \frac{v_o[j]}{L}\Delta t_{on}[j] = \sum_{j=1}^{j=n} \frac{v_o[j]}{L}\Delta t_{on}[j] \tag{3.21}$$

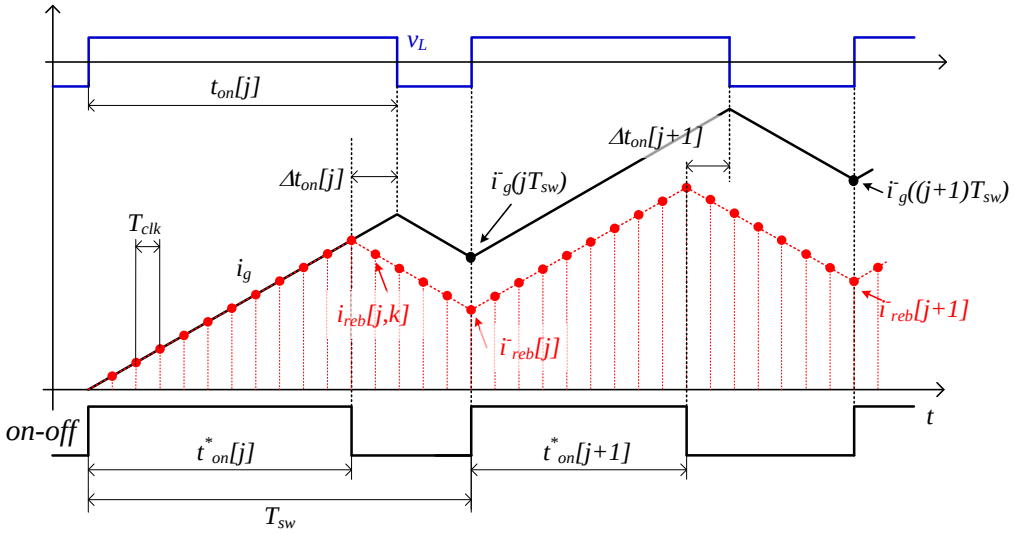


Figure 3.12: Digital estimated current $i_{reb}[j,k]$ compared with the analog real input current i_g, when the drive signal's delays $\Delta t_{on-off} \neq \Delta t_{off-on}$. The $on-off$ signal is the output of the digital device, and v_L the inductance voltage.

These expressions are only valid considering the converter operating in the CCM. Assuming this condition of operation, Eq. (3.21) can be approximated in the time domain as:

$$i_{error}(t) = \frac{1}{T_{sw}L}\int_o^t v_o(t)\triangle t_{on}(t)dt \tag{3.22}$$

that neglecting the output voltage ripple $v_o \approx V_o$, and considering a constant ON-time error/modification Δt_{on}, over the half line cycle can be rewritten as:

$$i_{error}(t) = \frac{V_o}{L}\frac{\Delta t_{on}}{T_{sw}}t \tag{3.23}$$

It can be appreciated how this current error does not depend on the demanded power. This error, accumulated at the end of the half-line cycle ($T_u/2$) is defined then by (3.24), being n_u the parameter that represents the total number of switching periods over $T_u/2$ ($n_u = T_u/2T_{sw}$). From (3.24), it can be seen how for the f_{sw}/f_u ratio influences the accumulated current error at the end of the half-line cycle.

$$i_{error}\,[n_u] = \frac{V_o}{2L}\frac{\Delta t_{on}}{T_{sw}}T_u = \frac{V_o\Delta t_{on}}{L}n_u \tag{3.24}$$

Expression (3.21), that models current estimation error due to drive signal delays (i_{error}) is compared now with the simulated current estimation error in MATLAB®/Simulink® & PLECS®, denoted as $i_{error,sim}$. The values of the power converter are the described before ($V_g = 230\,V_{rms}$, $V_o = 400\,V_{dc}$, $P_g \simeq P_o = 640\,W$ ($R = 250\,\Omega$), $f_{sw} = 100\,kHz$, $L = 1\,mH$, and $C = 220\,\mu F$), but with a constant duty cycle modification of $\Delta t_{on} = 10\,ns$ over the half line cycle. Therefore, under this conditions $v_g = v_g^* q$, $v_o = v_o^* q$, $q_g = q_o = q$, $L = L_{est}$, and $t_{on} \neq t_{on}^*$; the time evolution of the the signals i_g, i_{reb}, V_m, i_{error} and $i_{error,sim}$ is shown in

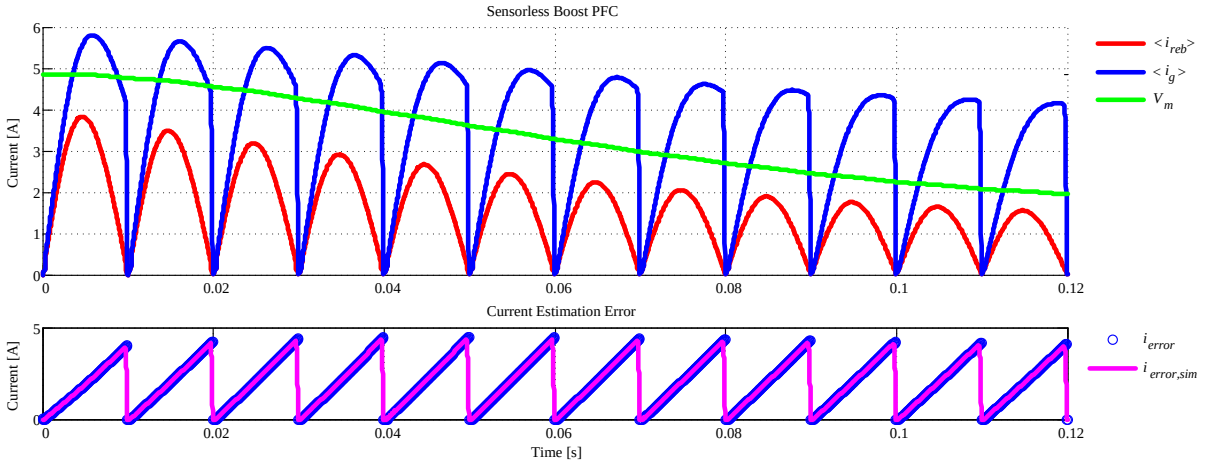


Figure 3.13: Transient state simulated waveforms obtained with the Simulink/PLECs system model with $V_g = 230\,V_{rms}$, $V_o = 400\,V_{dc}$, $P_g \simeq P_o = 640\,W$ ($R = 250\,\Omega$), $f_{sw} = 100\,kHz$ and reactive components $L = 1\,mH$, and $C = 220\,\mu F$, when Δt_{on}= 10 ns.

Fig. 3.13.

A positive value of Δt_{on}, leads to a positive current estimation error. Hence, i_g is always higher than the estimated current i_{reb}. In this simulation, the initial value of V_m is the ideal one (V_m = 4.84 V) obtaining a V_o is higher than the desired reference (400 V). Then, the output voltage loop acts with the propose of decrease V_o, decreasing the value of the control variable V_m, as it is shown in the Fig. 3.13. Finally, when the power delivered corresponds with the desired one, steady state is achieved. Waveforms in steady-state are presented in Fig. 3.14. A power factor value of PF = 0.907 is computed, with V_m = 1.85 V, I_{reb}/I_g = 0.29 and $THDi$= 32 %.

It can be observed the correspondence between the error resulted from the simulation ($i_{error,sim}$), computed as the difference between the simulated i_g and i_{reb}, and the waveform defined by the mathematical expression of i_{error} defined in (3.21).

On the other hand, the simulated current waveforms are presented are shown in Fig. 3.15 when a negative duty cycle modification (Δt_{on}= -10 ns) affects the sensorless PFC controller. Contrary to the previous case, in this situation, the duty cycle applied to the converter is lower than the computed by the controller, so i_g grows slower than i_{reb}. Therefore, i_g is always lower than i_{reb} (I_{reb}/I_g =1.53), and the voltage loop increases the value of V_m to deliver the expected power (V_m =7.65 V). A power factor value of PF = 0.957 is computed, with $THDi$ = 17 %.

It can be seen that $i_{error,sim}$ does not corresponds with i_{error} at the end of each half line cycle. When the real input current i_g, achieves DCM condition, the current value is zero at the end of the switching period, meanwhile i_{reb} continues decreasing proportional to the input voltage. During this time, i_{error} decreases as it is shown in Fig. 3.15 as well as $i_{error,sim}$ goes to zero. The mismatch is caused because DCM condition, and it is not considered in i_{error} expression.

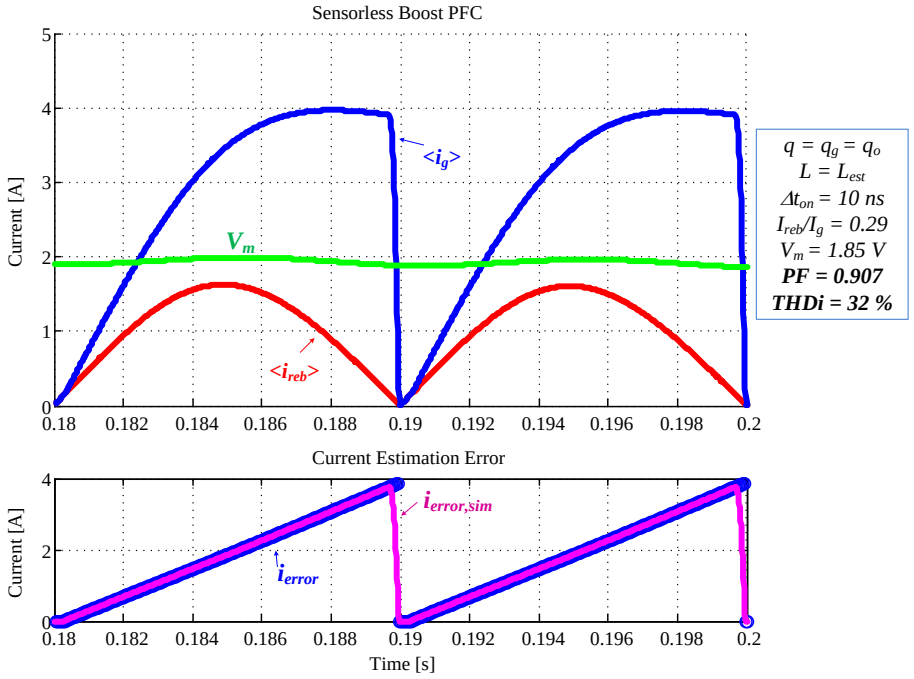


Figure 3.14: Steady state simulated waveforms with the Simulink/PLECs system model of the system with $V_g = 230\ V_{rms}$, $V_o = 400\ V_{dc}$, $P_g \simeq P_o = 640\ W$ $(R = 250\ \Omega)$, $f_{sw} = 100\ kHz$ and reactive components $L = 1\ mH$, and $C = 220\ \mu F$, when Δt_{on}= 10 ns.

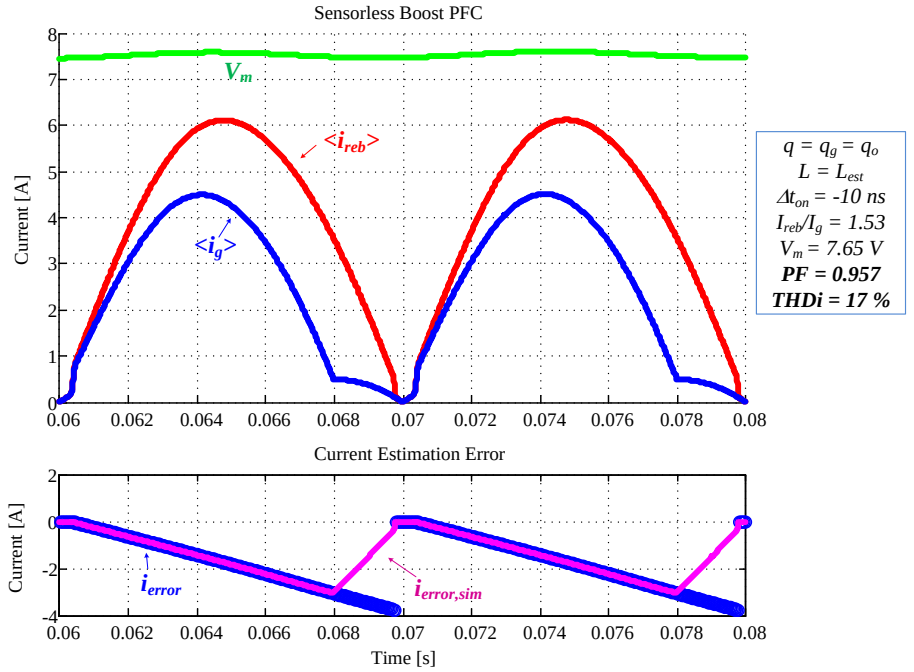


Figure 3.15: Steady state simulated waveforms with the Simulink/PLECs system model of the system with $V_g = 230\ V_{rms}$, $V_o = 400\ V_{dc}$, $P_g \simeq P_o = 640\ W$ $(R = 250\ \Omega)$, $f_{sw} = 100\ kHz$ and reactive components $L = 1\ mH$, and $C = 220\ \mu F$, when Δt_{on}= -10 ns.

When $\Delta t_{on-off} = \Delta t_{off-on}$, the current estimation error is caused only due to a constant delay between i_g and i_{reb}, using this model. According to this, the expressions (3.25) and (3.26) define current values at the end of the switching period j as:

$$i_g^- (jT_{sw}) = i_g^- ((j-1)\,T_{sw}) + \frac{v_g(jT_{sw} - \triangle T_{sw})}{L} t_{on}^*[j] + \\ + \frac{v_g(jT_{sw} - \triangle T_{sw}) - V_o}{L} (T_{sw} - t_{on}^*[j]) \quad (3.25)$$

$$i_{reb}^-[j] = i_{reb}^-[j-1] + \frac{v_g(jT_{sw})}{L} t_{on}^*[j] + \frac{v_g(jT_{sw}) - V_o}{L} (T_{sw} - t_{on}^*[j]) \quad (3.26)$$

where $\triangle T_{sw}$ represents the switching period displacement, and is defined as:

$$\triangle T_{sw} = (\Delta t_{on-off} + \Delta t_{off-on})/2$$

Working with (3.25) and (3.26), $i_{error}[n]$ is defined as:

$$i_{error}[n] = \frac{T_{sw}}{L} \sum_{j=0}^{j=n} v_g(jT_{sw} - \triangle T_{sw}) - v_g(jT_{sw}) \quad (3.27)$$

that is expressed in the time domain as:

$$i_{error}(t) = \frac{V_g\sqrt{2}}{L} \int_0^t \{sin[\omega(t - \triangle T_{sw})] - sin(\omega t)\}\, dt = \\ = \frac{V_g\sqrt{2}}{\omega L} \{cos(\omega t) - cos[\omega (t - \triangle T_{sw})]\} \quad (3.28)$$

Figure 3.16 shows the theoretical current waveforms under this condition. The current error caused by this switching period delay is much lower, in comparison with the current error when $\Delta t_{on-off} \neq \Delta t_{off-on}$ defined by (3.22). The theoretical current waveforms are shown in Fig. 3.16, and a simulated waveforms with $\Delta t_{on-off} = \Delta t_{off-on} = 500\,ns$, at the end of the utility period are presented in Fig. 3.17.

3.3.2 Effect of errors in data capture of voltage across the inductor

Input and output voltages of the converter are applied across the inductor, define the value of the real input current i_g and must be measure to estimate the current value in the digital controller. As is defined in Section 3.1, input and output voltage data, v_g^* and v_o^*, have a LSB (low significant bit) resolution (expressed in Volts per bit) represented by q_g and q_o, respectively, and given by Eq. (3.1).

A scheme of the used voltage data acquisition scheme is presented in Fig. 3.18. A resistive voltage divider adapts the input and output voltages (v_g and v_o) of the power converter, to be an analog input signal to each analog-to-digital converter v_g^s and v_o^s, respectively. In this application, without negative values in v_g and v_o, the analog full range scale in the ADC

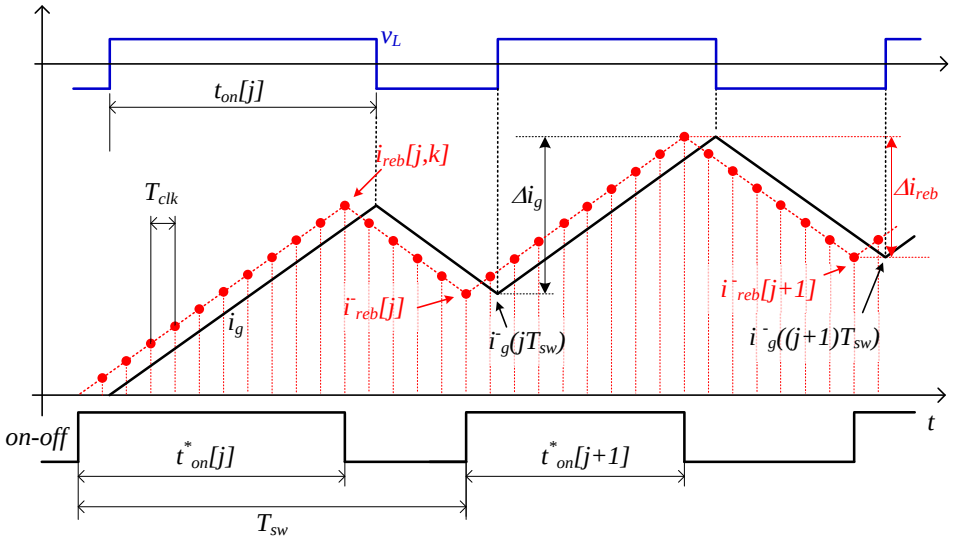


Figure 3.16: Digital estimated current $i_{reb}[j,k]$ compared with the analog real input current i_g with the drive signal's delays supposing $\Delta t_{on-off} = \Delta t_{off-on}$. The $on-off$ signal is the output of the digital device, and v_L the inductance voltage.

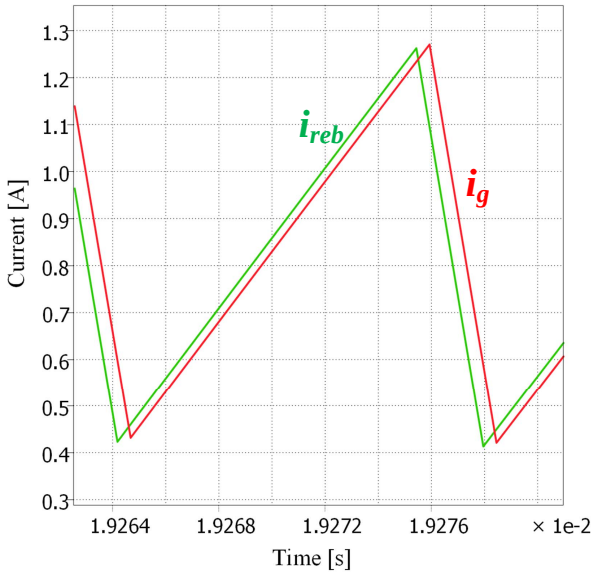


Figure 3.17: Digital estimated current i_{reb} compared with the analog real input current i_g with the drive signal's delays supposing $\Delta t_{on-off} = \Delta t_{off-on}$. The $on-off$ signal is the output of the digital device, and v_L the inductance voltage.

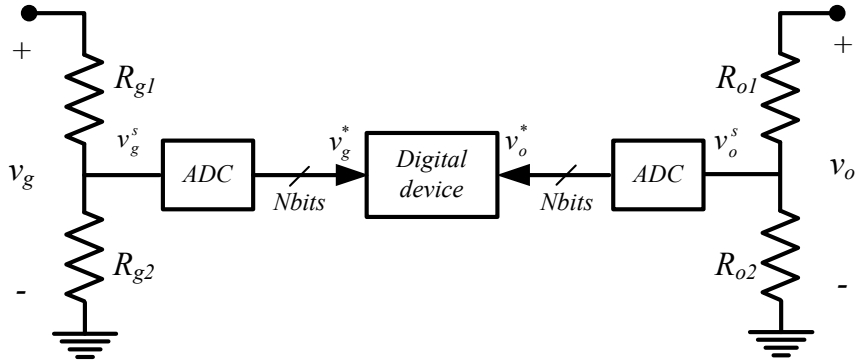


Figure 3.18: Voltage data acquisition scheme.

corresponds with the high-level input voltage of the digital device (v_{max}), both typically between 2.5 and 5.0 V defines the maximum value permitted for signals v_g^s and v_o^s.

The relationship between the power converter voltages v_g and v_o, and the voltage samples v_g^s and v_o^s, is defined by (3.29). The signals v_g^s and v_o^s are digitized in the ADCs, and assuming and an ideal analog-to-digital conversion, it can be represented by a gain k_g^{adc} and k_o^{adc}, represented by (3.30), per each voltage measurement. So the digital input and output voltage data v_g^* and v_o^*, are expressed according with (3.31).

$$\frac{v_g^s}{v_g} = \frac{R_{g2}}{R_{g1}+R_{g2}}\left(\frac{V}{V}\right); \quad \frac{v_o^s}{v_o} = \frac{R_{o2}}{R_{o1}+R_{o2}}\left(\frac{V}{V}\right) \tag{3.29}$$

$$k_g^{adc} = k_o^{adc} = \frac{2^{Nbits}-1}{v_{max}}\left(\frac{bit}{V}\right) \tag{3.30}$$

$$v_g^* = k_g^{adc} v_g^s = k_g^{adc}\frac{R_{g2}}{R_{g1}+R_{g2}} v_g; \;\; v_o^* = k_o^{adc} v_o^s = k_o^{adc}\frac{R_{o2}}{R_{o1}+R_{o2}} v_o \tag{3.31}$$

Therefore, working together with expressions (3.1) and (3.31), it yields an expression for the LSB resolution of the input and output voltage data

$$q_g = \frac{R_{g1}+R_{g2}}{R_{g2}}\frac{1}{k_g^{adc}} \;\; and \;\; q_o = \frac{R_{o1}+R_{o2}}{R_{o2}}\frac{1}{k_o^{adc}}. \tag{3.32}$$

A difference between q_g and q_o is caused due to noise, non-linearities, offsets and errors in the ADCs (affecting to k_g^{adc} and k_o^{adc} not always in the same way), and/or tolerances in the resistor divider used to sample the input and output voltage, so the real value of these variables is unknown by the designer. In this case, it is considered the situation in a more complete model with $v_g \neq v_g^* q$, $v_o \neq v_o^* q$, $q_g \neq q_o \neq q$, $L = L_{est}$ and $t_{on} = t_{on}^*$. The values of the real input current i_g and the estimated input current i_{reb}, in CCM at the end of a switching period j, $i_g^-(jT_{sw})$ and $i_{reb}^-[j]$ respectively, are defined by expressions (3.33) and

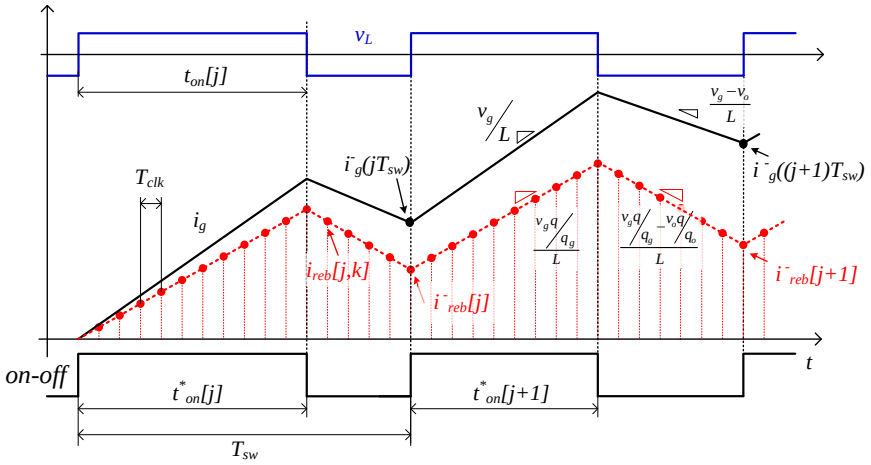


Figure 3.19: Digital estimated current $i_{reb}[j,k]$, compared with the analog real input current i_g, under errors in data capture voltage across the inductance when $q_g \neq q_o \neq q$. The $on-off$ signal is the output of the digital device and v_L the analog inductance voltage.

(3.34) according to the Fig. 3.1:

$$i_g^-(jT_{sw}) = i_g^-((j-1)T_{sw}) + \frac{v_g[j]}{L}t_{on}[j] + \frac{v_g[j]-v_o[j]}{L}(T_{sw}-t_{on}[j]) = \\ = i_g^-((j-1)T_{sw}) + \frac{T_{sw}}{L}\{v_g[j] - v_o[j]d'[j]\} \quad (3.33)$$

$$i_{reb}^-[j] = i_{reb}^-[j-1] + \frac{\frac{v_g[j]q}{q_g}}{L}t_{on}[j] + \frac{\frac{v_g[j]q}{q_g} - \frac{v_o[j]q}{q_o}}{L}(T_{sw}-t_{on}[j]) = \\ = i_{reb}^-[j-1] + \frac{T_{sw}}{L}\left\{\frac{v_g[j]q}{q_g} - \frac{v_o[j]q}{q_o}d'[j]\right\} \quad (3.34)$$

where $(1-d[j])$ in notated as $d'[j]$, and it is assumed a constant voltage value over the switching period j as $v_g[j]$ and $v_o[j]$:. Therefore, the current estimation error at the end of a switching period j is given by the difference between expressions (3.33) and (3.34):

$$i_{error}[j] = i_{error}[j-1] + \frac{T_{sw}}{L}\left\{v_g[j]\left(1-\frac{q}{q_g}\right) - v_o[j]\left(1-\frac{q}{q_o}\right)d'[j]\right\} \quad (3.35)$$

According to Eq. (3.35), the current estimation error $i_{error}[j]$, accumulated in n switching periods ($i_{error}[n]$) when the converter is operating in CCM is given by:

$$i_{error}[n] = i_g^-(nT_{sw}) - i_{reb}^-[n] = \frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_g[j]\left(1-\frac{q}{q_g}\right) - v_o[j]\left(1-\frac{q}{q_o}\right)d'[j]\right\} \quad (3.36)$$

Working now only with the last term of the expression, and with the goal of obtaining a generic expression of the current estimation error, the term $v_o[j]\left(1-\frac{q}{q_g}\right)d'[j]$ is added and

subtracted (in blue) in expression (3.36), as is done in (3.37):

$$\begin{aligned}
&\frac{T_{sw}}{L}\left\{v_g[j]\left(1-\frac{q}{q_g}\right)-v_o[j]\left(1-\frac{q}{q_o}\right)d'[j]\right\}= \\
&=\frac{T_{sw}}{L}\left\{v_g[j]\left(1-\frac{q}{q_g}\right)\textcolor{blue}{-v_o[j]\left(1-\frac{q}{q_g}\right)d'[j]}-v_o[j]\left(1-\frac{q}{q_o}\right)d'[j]\textcolor{blue}{+v_o[j]\left(1-\frac{q}{q_g}\right)d'[j]}\right\}= \\
&=\frac{T_{sw}}{L}\left\{\left(v_g[j]-v_o[j]d'[j]\right)\left(1-\frac{q}{q_g}\right)+v_o[j]d'[j]\,\frac{q}{q_g}\left(\frac{q_g}{q_o}-1\right)\right\} \qquad (3.37)
\end{aligned}$$

Comparing the first term into the curly brackets of (3.37) with (3.33), expression (3.36) can be rewritten as:

$$i_{error}[n]=i_g^-(nT_{sw})\times\left(1-\frac{q}{q_g}\right)+\frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_o[j]d'[j]\,\frac{q}{q_g}\left(\frac{q_g}{q_o}-1\right)\right\} \qquad (3.38)$$

It is possible to define the value of the real input current in the switching cycle n, $i_g(nT_{sw})$ as:

$$i_g(nT_{sw})=i_{reb}[n]\times\frac{q_g}{q}+\frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_o[j]d'[j]\left(\frac{q_g}{q_o}-1\right)\right\} \qquad (3.39)$$

and the current estimation error $i_{error}[n]$ is defined by:

$$i_{error}[n]=i_{reb}[n]\times\left(\frac{q_g}{q}-1\right)+\frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_o[j]d'[j]\left(\frac{q_g}{q_o}-1\right)\right\}. \qquad (3.40)$$

At this point, it is important to explain expressions (3.39) and (3.40). Both expressions have two different terms, the first term defines a current proportional to the estimated input current i_{reb}, which is the variable controlled by the PFC controller, and has a sinusoidal shape if the converter operates in CCM. So the first term does not create distortion (harmonics) in the real input current. The second term is not sinusoidal, describing a current distortion in i_g and then, decreasing the value of the power factor. It can be observed how this term is non-zero when $q_g \neq q_o$.

If the boost converter operates in the CCM, the relation between v_g and v_o is given, approximately, by $v_g = V_o(1-d)$. Using this approach, the digital circuit computes the duty cycle command as:

$$d[j]=1-\frac{v_g^*[j]}{v_o^*[j]}=1-\frac{v_g[j]q_o}{q_g v_o[j]} \qquad (3.41)$$

which can be used in (3.40) to write i_{error} in terms of v_g as:

$$i_{error}[n]=i_{reb}[n]\times\left(\frac{q_g}{q}-1\right)+\frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_g[j]\left(1-\frac{q_o}{q_g}\right)\right\}. \qquad (3.42)$$

As an example, the same parameters as the used in the real converter are plugged in the components of the Fig. 3.18, to illustrate the behavior of the controller. For both voltage

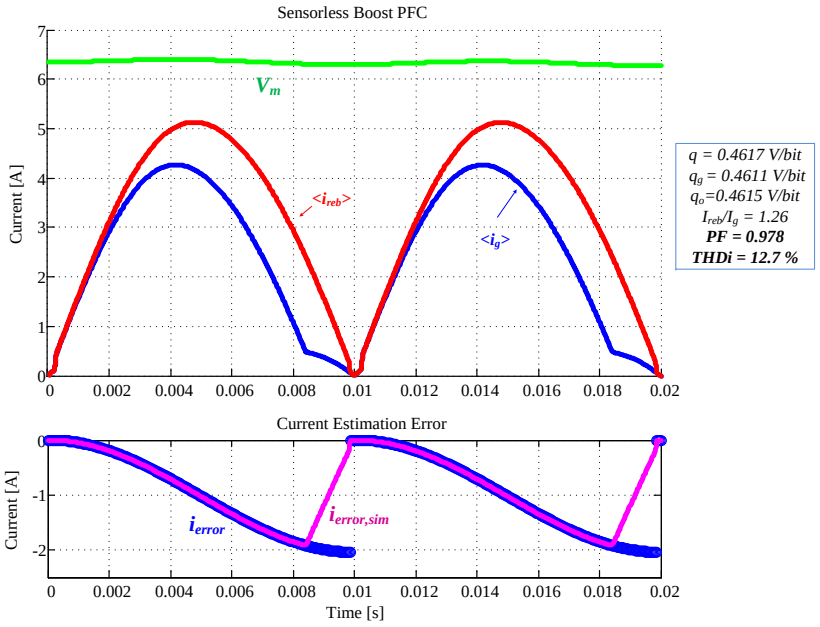


Figure 3.20: Steady state simulated waveforms with the Simulink/PLECs system model of the system with $V_g = 230\ V_{rms}$, $V_o = 400\ V_{dc}$, $P_g \simeq P_o = 640\ W$ ($R = 250\ \Omega$), $f_{sw} = 100\ kHz$ and reactive components $L = 1\ mH$, and $C = 220\ \mu F$, when $q = 0.4617\ V/bit$, $q_g = 0.4611\ V/bit$, and $q_o = 0.4615\ V/bit$.

measurements, two ADCs with $N_{bits} = 10$ and $v_{max} = 5\,V$ have been implemented. Trying to assure the same LSB resolution in both measurements, the two resistor dividers use the same resistors, defined by the catalog as $R_{g1} = R_{o1} = 1M\Omega{\pm}0.1\%$ and $R_{g1} = R_{g2} = 10.7k\Omega{\pm}0.1\%$. According to this, the nominal LSB resolution q is given by:

$$q = \frac{1\ M\Omega + 10.7\ k\Omega}{10.7\ k\Omega}\frac{5\ V}{2^{N_{bits}} - 1} = 0.4617\frac{V}{bit} \tag{3.43}$$

The real values of the resistances are function on the real tolerances, being $T_{g1}, T_{g2}, T_{o1}, T_{o2}$ the real values of the resistance tolerances of $R_{g1} = 1M\Omega{+}T_{g1}$ and $R_{g2} = 10.7k\Omega{+}T_{g2}$ for the input voltage measurement, and $R_{o1} = 1\ M\Omega + T_{o1}$ and $R_{g2} = 10.7\ k\Omega + T_{o2}$, for the output voltage divider. Considering for simulation, $T_{g1} = -0.05\%$, $T_{g2} = 0.08\%$, $T_{o1} = 0.02\%$, $T_{o2} = 0.05\%$, the value of the real q_g and q_o are given by:

$$q_g = \frac{(1\ M\Omega + T_{g1}) + (10.7\ k\Omega + T_{g2})}{10.7\ k\Omega + T_{g2}}\frac{5\ V}{2^{N_{bits}} - 1} = 0.4611\frac{V}{bit} \tag{3.44}$$

$$q_o = \frac{(1\ M\Omega + T_{o1}) + (10.7\ k\Omega + T_{o2})}{10.7\ k\Omega + T_{o2}}\frac{5\ V}{2^{N_{bits}} - 1} = 0.4615\frac{V}{bit} \tag{3.45}$$

Plugging these values in the simulation model, waveforms like the presented in Fig. 3.20 are obtained for the components described previously. The current i_g and i_{reb} are plotted at the top of the figure, and the simulated current error $i_{error,sim}$ is compared with the modeled error defined by (3.40), i_{error}, at the bottom of the figure. This simulated waveforms can occur

in the real system, because the tolerances simulated are between the limits defined by the resistor datasheet, so are inherent of the analog sampler circuit. Other sources of error that can modify the value of q, q_g and q_o, even over the half line cycle. Nonidealities of the ADC can causes this, that is analyzed in detail in Chapter 5, where the digital implementation of the sensorless controller is described.

3.3.3 Errors due to difference between real inductance L and the estimated inductance L_{est}

The last cause of current estimation error analyzed in this Chapter, is due to differences between the real inductance value (L) and the estimated (L_{est}). The behavior of the sensorless boost PFC controller is shown in Fig. 3.21 in this condition, when $t_{on} = t_{on}^*$, $L \neq L_{est}$, $v_g = v_g^* q$ and/or $v_o = v_o^* q$ with $q_o = q_g = q$. According to this, in a switching period j, the current is a function of the different inductance as is described in Eq. (3.46) and (3.47).

$$i_g\left(jT_{sw}\right) = i_g\left(\left(j-1\right)T_{sw}\right) + \frac{v_g[j]}{L} d\left[j\right] T_{sw} + \frac{v_g[j]-v_o[j]}{L} d'\left[j\right] T_{sw} = \\ = i_g\left(\left(j-1\right)T_{sw}\right) + \frac{T_{sw}}{L}\left\{v_g[j] - v_o[j] d'\left[j\right]\right\} \quad (3.46)$$

$$i_{reb}\left[j\right] = i_{reb}\left[j-1\right] + \frac{v_g[j]}{L_{est}} d\left[j\right] T_{sw} + \frac{v_g[j]-v_o[j]}{L_{est}} d'\left[j\right] T_{sw} = \\ = i_{reb}\left[j-1\right] + \frac{T_{sw}}{L_{est}}\left\{v_g[j] - v_o[j] d'\left[j\right]\right\} \quad (3.47)$$

Comparing this two expressions, the relation between the real input current and the estimated in this case, yields to expressions (3.48) and (3.49) for i_g and i_{error}, over n switching periods of the half line cycle ($T_u/2$), respectively. As it has been mentioned before, i_{reb} is the variable controlled by the NLC control algorithm, so it has a sinusoidal shape (proportional to the input voltage). Considering the real inductance constant over T_u, the real current i_g is sinusoidal too and despite the current error estimation the power factor value does not decrease.

$$i_g\left(nT_{sw}\right) = i_{reb}[n] \times \frac{L_{est}}{L} \quad (3.48)$$

$$i_{error}[n] = i_{reb}[n] \times \left(\frac{L_{est}}{L} - 1\right) \quad (3.49)$$

The PFC output voltage loop guarantees the desired output voltage (v_o) and corrects the estimation error caused by the difference between L and L_{est} adjusting the amplitude of i_{reb} and then, i_g . A simulation of a line period is presented in Fig. 3.22 for the component values said before and with an estimated inductance $L_{est} = 1.8$ mH. It can be seen how both currents, i_{reb} and i_g, are totally sinusoidal and proportional between them, so the PF do not

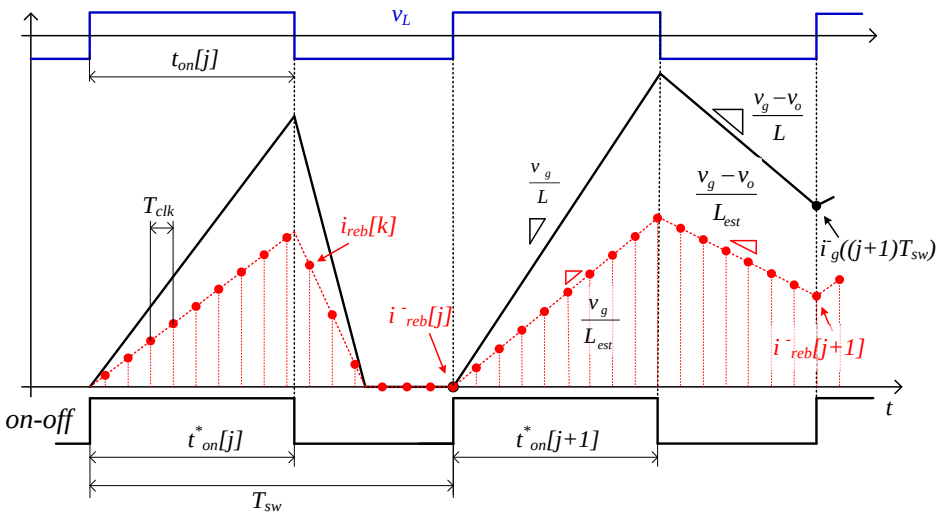


Figure 3.21: Digital estimated current $i_{reb}[k]$ compared with the analog real input current i_g when the estimated inductance value (L_{est}) is higher than the real (L). The $on-off$ signal is the output of the digital device, and v_L the inductance voltage.

decrease.

But at this point, is important to clarify that it is possible that the inductance varies over the half line cycle. Magnetic cores based on Soft Saturation material, like MPP or Kool mμ, in which the inductance is a function of the current. Ferrites cores result is almost constant inductance, but it decreases abruptly when the core is saturated. However, with soft saturation materials, it is possible to reduce the volume of the magnetic components because the flux density can reach up to 1 Tesla, i. e. around 3 times the traditional ferrites whose hard saturation is found around 350 mT [150, 151]. One of the inductors used in the experimental validation, shown in Chapter 8, has been built in a Kool mμ core 77071 whose inductance is a function of the current, given as:

$$L\left(i_L\right) = 1.5 - 0.174 i_L \; [mH], \tag{3.50}$$

so in this case, i_{error} and i_g waveforms are not sinusoidal due to this non-linearity. Figure 3.23 shows the simulated current waveforms when this inductance is used. It has been considered $V_g = 230\,V_{rms}$, $V_o = 400\,V_{dc}$, $P_g \simeq P_o = 640\,W$ $(R = 250\,\Omega)$, $f_{sw} = 100\,kHz$, $L_{est} = 1.5\,mH$, and $C = 220\,\mu F$. The simulated power factor is high, but the harmonics in the current increase in comparison with the linear inductor presented in Fig. 3.22.

3.4 Chapter conclusion

In this Chapter, several causes of current estimation error that produce a distortion in the input current i_g are analyzed and modeled in detail, in a Boost PFC rectifier controlled by the sensorless approach. Among the three sources of error analyzed in Section 3.3 the ON-time modification ($\triangle t_{on}$) due to the drive signal's delays, the difference between LSB resolution

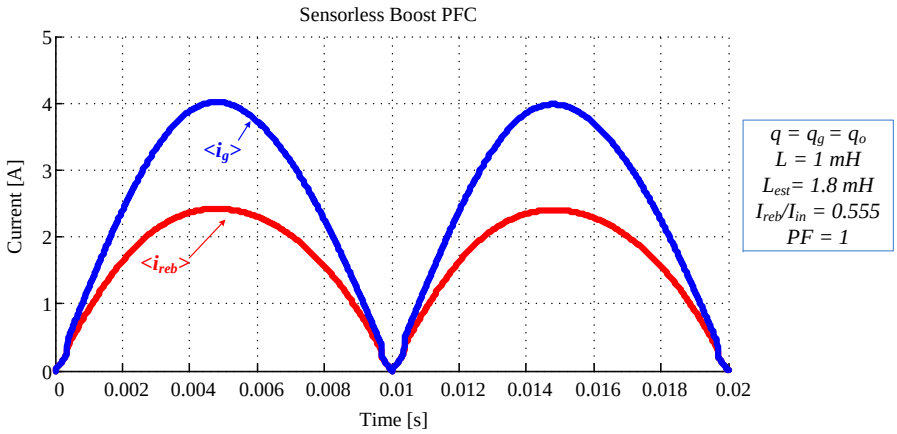


Figure 3.22: Steady state simulated waveforms with the Simulink/PLECs system model of the system with $V_g = 230\,V_{rms}$, $V_o = 400\,V_{dc}$, $P_g \simeq P_o = 640\,W$ ($R = 250\,\Omega$), $f_{sw} = 100\,kHz$ and reactive components $L = 1\,mH$, and $C = 220\,\mu F$ and $L_{est} = 1.8\,mH$.

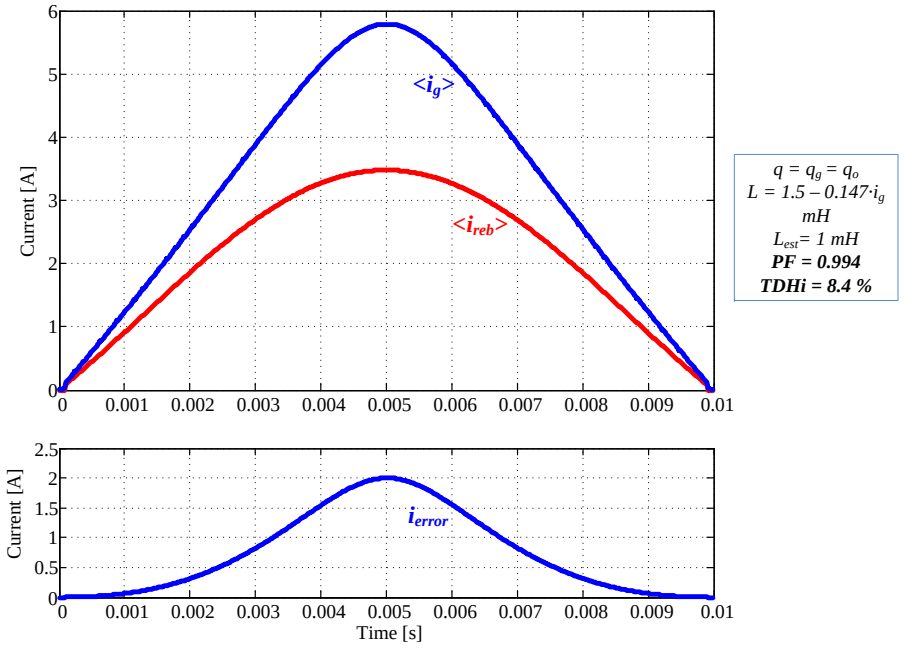


Figure 3.23: Simulated current waveforms when the real inductance value L is a function of the current $L\,(i_L) = 1.5 - 0.174 i_L\;[mH]$ and $L_{est} = 1.5\,mH$. Top: Input current i_g, and rebuilt current i_{reb}. Bottom: Current estimation error i_{error}.

of the input (q_g) and the output (q_o) voltages and nonlinearity of L causes current distortion and then decreases the PF value. The first one means a difference between the effective ON-time applied to the converter, and the estimated ON-time in the digital controller, and is given by:

$$i_{error}(t) = \frac{V_o}{L}\frac{\Delta t_{on}}{T_{sw}}t \quad with\ 0 \leq t \leq T_u/2 \tag{3.51}$$

where each half line cycle starts at $t = 0$.

The fact that $q_g \neq q_o$ means a difference between the V/bit resolution in the ON-state and in the OFF-state, and consequently, a difference in the A/bit also. So, to analyze the behavior of the PFC controller with the current estimator (Fig. 3.1b), it can be considered $q = q_g$ and $L = L_{est}$. With this consideration, the current error accumulated in the n^{th} switching period, defined previously by Eq. (3.40), can be rewritten now as:

$$i_{error}[n] = \frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_o[j]d'[j]\left(\frac{q_g}{q_o}-1\right)\right\} = \frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_g[j]\left(1-\frac{q_o}{q_g}\right)\right\} \tag{3.52}$$

which can be expressed in the time domain to obtain the expression $i_{error}(t)$, considering q_g and q_o constant over the line cycle:

$$i_{error}(t) = \frac{V_g\sqrt{2}}{L}\left(1-\frac{q_o}{q_g}\right)\int_0^t sin\,(\omega t)\,dt = \frac{V_g\sqrt{2}}{\omega L}\left(1-\frac{q_o}{q_g}\right)(1-cos\,(\omega t)) \quad with\ 0 \leq t \leq T_u/2 \tag{3.53}$$

Chapter 4

Influence of the converter parasitics in the current estimation

Up to this point, the analysis of the current estimation errors has been developed neglecting the parasitics of the different components. Figure 4.1 shows the diagram of the boost converter with the parasitic elements, which have influence in the input current estimation, i_{reb}. As first approximation, to describe the approach of current estimator, it has been considered the inductor voltage $v_L = v_g$ during ON-state and $v_L = v_g - v_o$ during OFF-state, and this instant voltage is plugged in the inductance fundamental equation $v_L = L^{di_L}/_{dt} = L^{di_g}/_{dt}$, implemented as finite difference equation in the digital device. But in the real converter the voltage applied to the inductor is given by (4.1):

$$v_L = \begin{cases} v_g - (R_L + R_{on})\, i_g & if \quad ON - state \\ v_g - (R_L + R_D)\, i_g - V_D - v_o & if \quad OFF - state \end{cases} \tag{4.1}$$

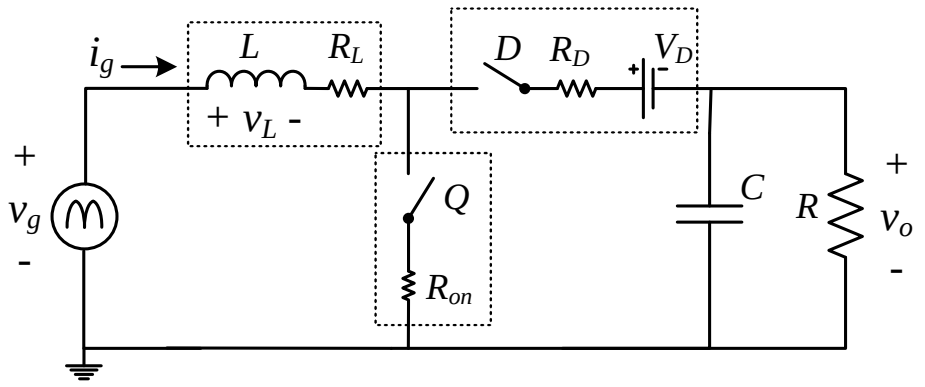


Figure 4.1: Boost converter diagram with parasitic elements.

being R_L the effective series resistor placed in series with an ideal inductance L, to emulate the behavior of the real inductor. The power MOSFET Q, is modeled with an ON-state resistance R_{on}, in series with an ideal switch; and in the power diode D, a voltage source V_D, represents the forward voltage at zero current, in series with a resistor R_D, which emulates the variation of the forward voltage with the diode current. According to this, the average voltage in the inductor is given by:

$$v_L = v_g - v_o\,(1-d) - R_L i_g - R_{on} i_g d - R_D i_g\,(1-d) - V_D\,(1-d) \tag{4.2}$$

The controller varies the duty cycle d, so that the average input current $\langle i_g \rangle$, over the switching period follows the input voltage, $\langle i_g \rangle = \frac{v_g}{R_e}$, where the emulated resistance R_e, is chosen by the controller to obtain the desired DC output voltage. By solving the volt-second balance in L, where $\langle v_L \rangle = 0$:

$$v_g - v_o\,(1-d) = R_L\,\langle i_g \rangle + R_{on}\,\langle i_g \rangle\,d + R_D\,\langle i_g \rangle\,(1-d) + V_D\,(1-d) \tag{4.3}$$

Substituting $\langle i_g \rangle = \frac{v_g}{R_e}$, in (4.3) to eliminate i_g, it is obtained:

$$v_g - v_o\,(1-d) = R_L \frac{v_g}{R_e} + R_{on} \frac{v_g}{R_e} d + R_D \frac{v_g}{R_e}\,(1-d) + V_D\,(1-d) \tag{4.4}$$

and it is possible to solve the command d calculated by the PFC controller to obtain a sinusoidal current [63]:

$$d = \frac{v_g \left[1 - (R_L + R_D)\,\frac{1}{R_e}\right] - v_o - V_D}{(R_{on} - R_D)\,\frac{v_g}{R_e} - v_o - V_D} \tag{4.5}$$

This expression neglects the converter dynamics, assuming that these dynamics are sufficiently faster than the utility voltage variation, $f_{sw} \gg f_u$. It also neglects DCM operation near the input voltage zero crossings. It can be seen how the expression (4.5) corresponds with the ideal duty cycle command $d \approx 1 - \frac{v_g}{v_o}$, neglecting the parasitic elements influence ($R_L = R_D = R_{on} = V_D = 0$).

To analyze the effect of the parasitic elements it is necessary to assess the average voltage drop across them, in each switching period T_{sw}, defined as $\langle v_{par} \rangle$. By solving the volt-second balance in L, as in Eq. (4.3):

$$v_g - v_o\,(1-d) + \langle v_{par} \rangle = 0 \tag{4.6}$$

being

$$\langle v_{par} \rangle = -R_L\,\langle i_g \rangle - R_{on}\,\langle i_g \rangle\,d - R_D\,\langle i_g \rangle\,(1-d) - V_D\,(1-d) = -v_g + v_o\,(1-d) \tag{4.7}$$

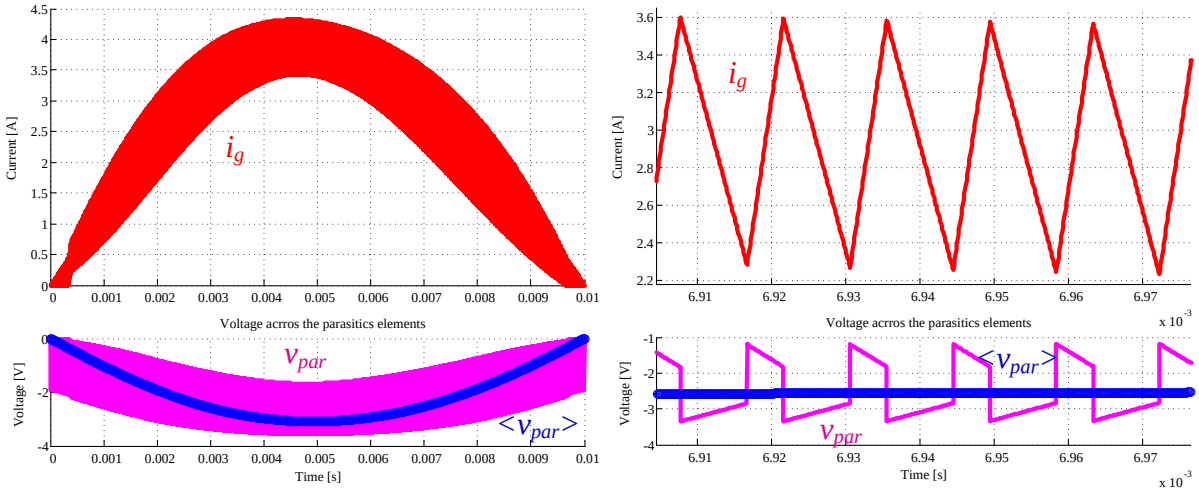


Figure 4.2: Input current waveform i_g, instantaneous v_{par} and average voltage drop over the switching cycle in the parasitic elements, $\langle v_{par} \rangle$. Left: waveforms over the half line cycle. Right: Switching waveforms.

that can be rewritten substituting (4.5):

$$\langle v_{par} \rangle = v_o \left(1 - d\right) - v_g = v_g \left(\frac{v_o \left(R_{on} + R_L - R_e\right)}{v_g \left(R_{on} - R_D\right) - \left(V_D + v_o\right) R_e} - 1 \right) \tag{4.8}$$

Figure 4.2 shows the instant v_{par} and average $\langle v_{par} \rangle$ voltage across the parasitic elements over the half line cycle, and in several switching waveforms. v_{par} is obtained with the MATLAB/PLECs simulation, and the waveform $\langle v_{par} \rangle$, is defined by expression (4.8).

An approximation to the structure of the digital current estimation, neglecting the influence of the parasitics, has been presented in Chapter 3 (Fig. 3.1). Considering no errors in the data acquisition process and no switching delays in the drive signal ($v_g = v_g^* q$, $v_o = v_g^* q$, $q_g = q_o = q$ and $t_{on}^* = t_{on}$), the inductor voltage estimated in the digital device, expressed in volts, is defined by:

$$v_{L,reb} = \begin{cases} v_g & if \quad ON - state \\ v_g - v_o & if \quad OFF - state \end{cases} \tag{4.9}$$

and then, the averaged inductor estimated voltage en each switching period $\langle v_{L,reb} \rangle$, is:

$$\langle v_{L,reb} \rangle = v_g - v_o \left(1 - d\right) \tag{4.10}$$

considering the low dynamic nature of the signals, $v_g \approx \langle v_g \rangle$ and $v_o \approx \langle v_o \rangle$. Comparing expressions (4.9) and (4.3), it can be observed that the average voltage across the inductor $\langle v_L \rangle$, is lower than the value estimated in the digital device $\langle v_{L,reb} \rangle$. This small error is due to the voltage drop in the parasitic elements:

$$\langle v_L \rangle = \langle v_{L,reb} \rangle - \langle v_{par} \rangle \tag{4.11}$$

The small error is accumulated every switching period over the half-line cycle ($i_g = \int v_L dt$

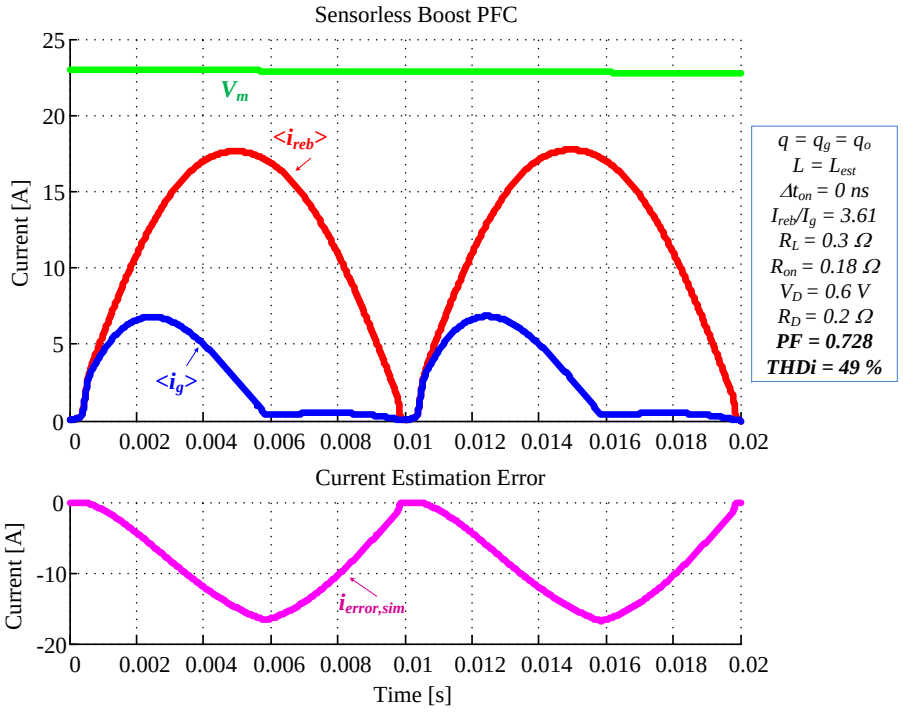


Figure 4.3: Simulated current waveforms without consideration of the parasitic elements influence. Top: Real and rebuilt input current. Bottom: Simulated current estimation error.

and $i_{reb} = \int v_{L,reb} dt$) resulting in a low power factor. Since i_g is less than the estimated i_{reb}, the voltage loop increases i_{reb}, and then i_g to obtain a RMS value of the input current I_g, which assures the expected output power ($I_g = \frac{V_o^2}{RV_g}$).

Figure 4.3 shows the case where the estimated volt-seconds across the inductor are lower than the actual ones due to non-compensated parasitics effect with $V_g = 230\ V_{rms}$, $V_o = 400\ V_{dc}$, $P_g \simeq P_o = 640\ W$ ($R = 250\ \Omega$), $f_{sw} = 100\ kHz$ and reactive components $L = 1\ mH$, and $C = 220\ \mu F$. The parasitic elements are $R_L = 0.3\ \Omega$ for the inductor, $R_D = 0.2\ \Omega$ and $V_D = 0.6\ V$ for the power diode, and $R_{on} = 0.18\ \Omega$ for the power MOSFET. These values are the ones given by the datasheets of the RHRP860 Fairchild Power Diode and the IRFP27N60K International Rectifier Power MOSFET. It can be observed that, $i_g < i_{reb}$ and then i_g operates in DCM longer than i_{reb} with a PF value of 0.729, $THDi = 49\ \%$.

Current estimation error occurs because $\langle v_L \rangle \neq \langle v_{L,reb} \rangle$, caused due to the voltage drop in the parasitic elements $\langle v_{par} \rangle$, defined by (4.11). To model the effect of the parasitic elements, it is going to be considered that the boost converter only has one equivalent parasitic element (EPE), and the average voltage drop through it in each switching period, is equal to $\langle v_{par} \rangle$. The current estimation algorithm presented in this Thesis is based on the fundamental equation of an inductor, $i_L = \frac{1}{L} \int v_L dt$; and the measurements used to estimate this inductor voltage are v_g and v_o. Two approaches are presented to analyze the effect:

1. The Equivalent Parasitic Element is placed in series with the input voltage (EPE_g).

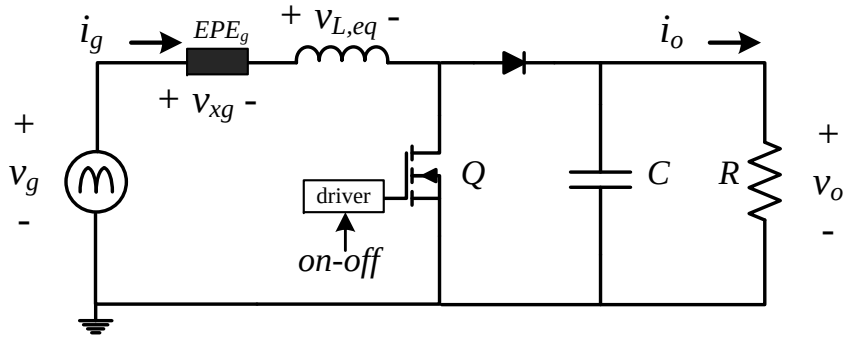


Figure 4.4: Equivalent boost converter circuit with the EPE connected in series with the inductor.

2. The Equivalent Parasitic Element is placed in series with the output voltage (EPE_o).

These two approaches are not only used to model the current estimation error caused due to the parasitic elements, they are important to understand the digital compensation of the errors, presented in Chapter 5. These models correspond with the average models of the boost converter, considering parasitic elements, shown in [63] particularized for the case of a power factor correction stage, where the current waveform and duty cycle command are known.

4.1 Modeling the parasitic elements effect with the Equivalent Parasitic Element in series with the input voltage (EPE_g)

The equivalent circuit of the boost converter with the Equivalent Parasitic Element in series with the input voltage (EPE_g), as is presented in Fig. 4.4. The instantaneous EPE_g voltage and the inductor voltage in the equivalent boost converter circuit are represented by v_{xg} and $v_{L,eq}$, respectively. The real voltage in the inductor v_L, is given by exp. (4.12):

$$v_L = \begin{cases} v_g - (R_L + R_{on})\, i_g & if \quad ON - state \\ v_g - (R_L + R_D)\, i_g - V_D - v_o & if \quad OFF - state \end{cases} \tag{4.12}$$

whose average value in each switching period $\langle v_L \rangle$ is:

$$\langle v_L \rangle = v_g - v_o\,(1-d) + \langle v_{par} \rangle \tag{4.13}$$

where $\langle v_{par} \rangle$ is defined by Eq. (4.8). And $v_{L,eq}$ by (4.14)

$$v_{L,eq} = \begin{cases} v_g - v_{xg} & if \quad ON - state \\ (v_g - v_{xg}) - v_o & if \quad OFF - state \end{cases} \tag{4.14}$$

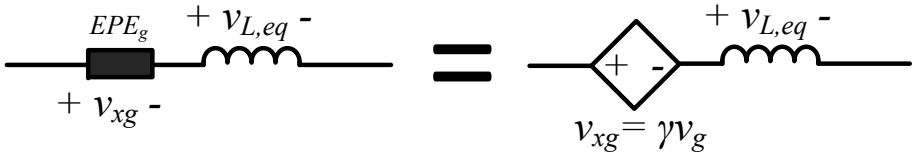


Figure 4.5: Equivalence between the Equivalent Parasitic Element (EPE_g) and a dependent voltage source function of the input voltage.

whose average value in each switching period $\langle v_{L,eq} \rangle$ is:

$$\langle v_{L,eq} \rangle = v_g - v_o\,(1-d) - v_{xg} \tag{4.15}$$

being $\langle v_{xg} \rangle$ the average voltage in each switching period of the signal v_{xg}, and corresponds with $\langle v_{xg} \rangle = v_{xg}d + v_{xg}\,(1-d) = v_{xg}$. The goal of this analysis is to match $\langle v_{L,eq} \rangle = \langle v_L \rangle$, obtaining the expression that defines v_{xg}:

$$v_{xg} = -\langle v_{par} \rangle = v_g \left(1 - \frac{v_o\,(R_{on} + R_L - R_e)}{v_g\,(R_{on} - R_D) - (V_D + v_o)\,R_e}\right) \tag{4.16}$$

It can be considered that expression (4.16) defines v_{xg} as a product of v_g (rectified sinusoidal input voltage) and a term into the brackets quasi-constant over the half-line cycle, considering a low output voltage ripple $v_o \approx V_o$ and $R_{on} \approx R_D$, the term $v_g\,(R_{on} - R_D) - (V_D + v_o)\,R_e$ is approximated as $V_g\,(R_{on} - R_D) - (V_D + V_o)\,R_e$. Then, the EPE can be considered as a dependent voltage source, as is shown in Fig. 4.5, with:

$$\gamma = \left(1 - \frac{V_{ref}\,(R_{on} + R_L - R_e)}{V_g\,(R_{on} - R_D) - (V_D + V_o)\,R_e}\right) \tag{4.17}$$

According to this, it is possible to create a circuit that models the behavior of the real boost PFC converter with the influence of the parasitic elements in series with the input voltage. This model has been developed considering a $\langle i_g \rangle$ waveform proportional to the input voltage, so it is only valid around the steady state operating point ($i_g = i_{reb}$, $V_o = V_{ref}$ and $\langle i_g \rangle = \frac{v_g}{R_e}$). But it shows how it is possible to correct the current estimation error adding to the current estimator block a digital signal v_{dig} in the input voltage data, as it is presented in Fig. 4.6, and the expression of the rebuilt/estimated inductor voltage $v_{L,reb}$, as is given in (4.18).

To avoid current estimation error due to parasitic elements, the value of $v_{dig}q_g$ must be equal to $-v_{xg}$. It can be seen how v_{xg} value is a function of the power ($R_e = \frac{P_g}{V_g^2}$), in comparison with the other causes of current estimation error presented in Chapter 3, whose influence is not a function of the power or load.

$$v_{L,reb} = \begin{cases} (v_g - v_{dig}q_g)\,\frac{q}{q_g} & if \quad ON-state \\ (v_g - v_{dig}q_g)\,\frac{q}{q_g} - v_o\frac{q}{q_o} & if \quad OFF-state \end{cases} \tag{4.18}$$

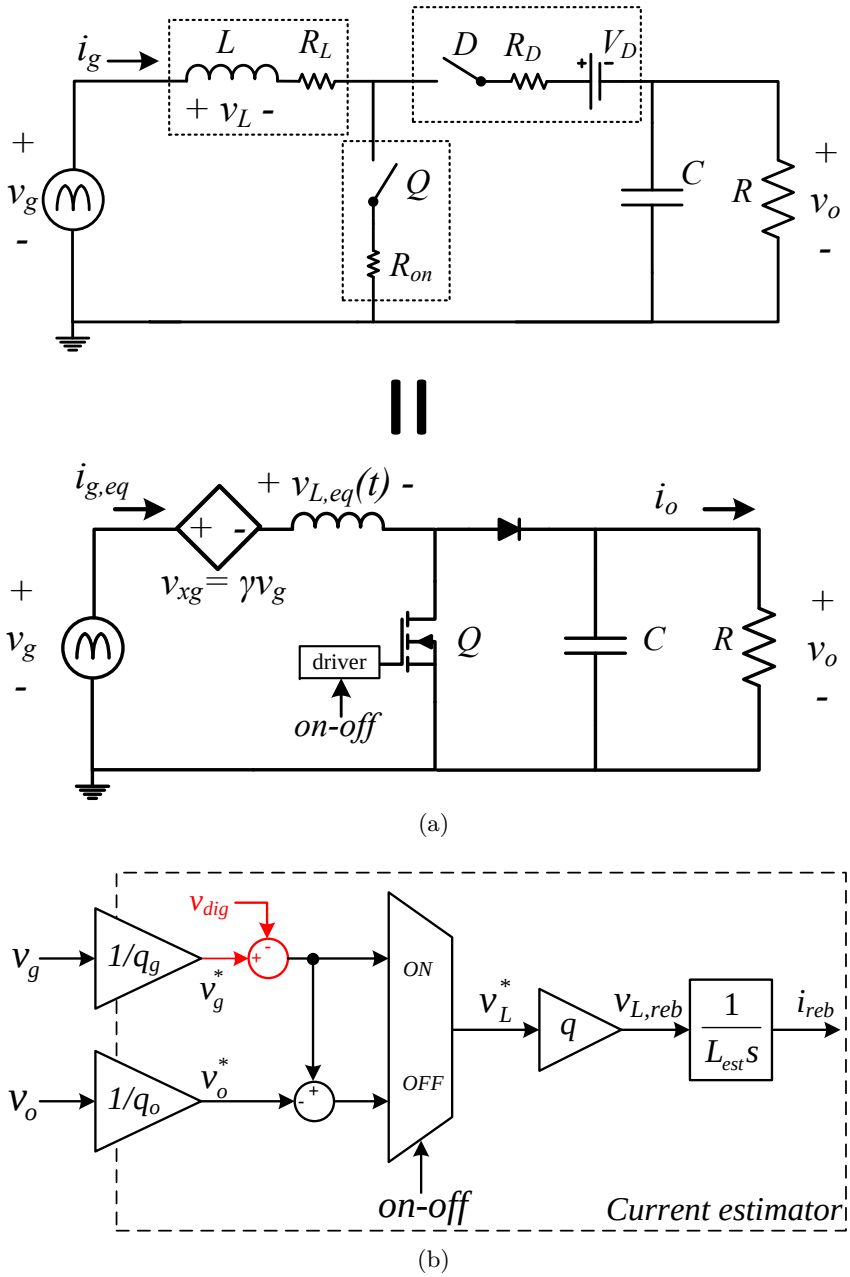


Figure 4.6: (a) Equivalent boost converter with the EPE represented by a dependent voltage source. (b) Modification of the current estimation block with the compensation in the input voltage data.

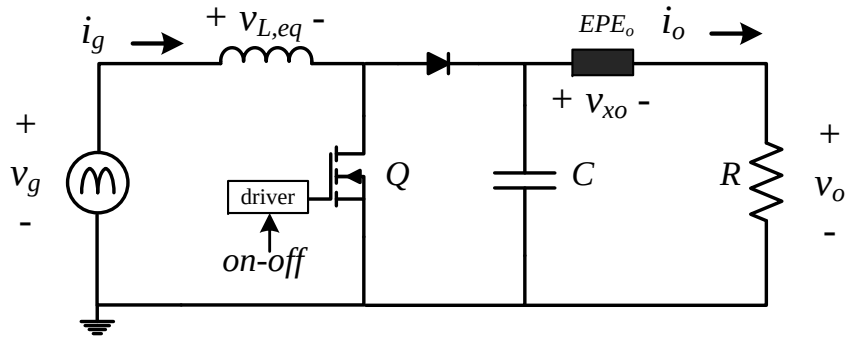


Figure 4.7: Equivalent boost converter circuit with the EPE_o connected in series with the output.

with

$$v_{dig}q = v_g\gamma \approx v_{xg} \tag{4.19}$$

so v_{dig} does not have high frequency components, being labeled as v_{dig}[1]. Comparing expressions (4.14) and (4.18), it is possible to define the value of the current estimation error over n switching periods, $i_{error}\,[n]$:

$$i_{error}[n] = \frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_o[j]d'\,[j]\left(\frac{q_g}{q_o}-1\right)\right\} + \frac{T_{sw}}{L}\sum_{j=1}^{j=n}\left(qv_{dig}[j]-v_{xg}[j]\right) \tag{4.20}$$

It can be seen that (4.20) is the sum of two terms: the first term corresponds to the quantization mismatch of the ADCs employed to sample the input and output voltages and the second term as presented in section 3.3.2 and the second term corresponds with the current error caused due to the influence of the parasitic elements. Considering no errors in the voltage data capture ($v_g = v_g^* q$, $v_o = v_g^* q$, $q_g = q_o = q$) the accumulated current error generated by parasitic elements influence over n switching periods, with a compensation in the current estimator by v_{dig}, is given by:

$$i_{error}[n] = \frac{T_{sw}}{L}\sum_{j=1}^{j=n}\left(qv_{dig}[j]-v_{xg}[j]\right) \tag{4.21}$$

4.2 Modeling the parasitic elements effect with the Equivalent Parasitic Element in series with the output voltage (EPE_o)

Figure 4.7 represents the influence of the parasitic elements in series with the output voltage (v_o). The instantaneous EPE_o voltage and the inductor voltage, in the equivalent boost converter circuit, are represented by v_{xo} and $v_{L,reb}$, respectively. In this case, v_L and $v_{L,reb}$ are defined according to (4.22):

[1]It must be remembered that, in this case, is used indifferently q and q_g, because it is considered $q = q_g$

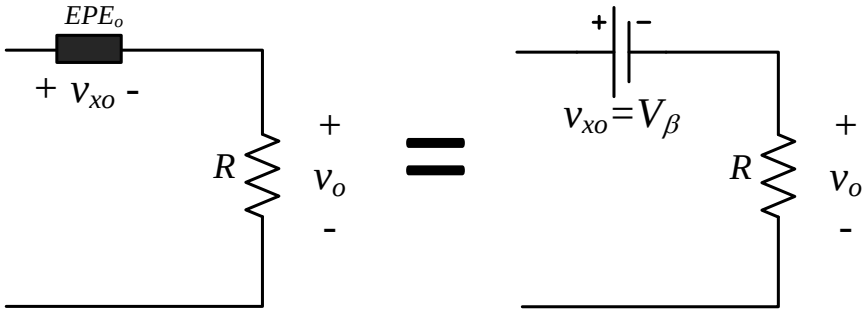


Figure 4.8: Equivalence between the Equivalent Parasitic Element and a constant voltage source.

$$v_L = \begin{cases} v_g - (R_L + R_{on})\, i_g \\ v_g - (R_L + R_D)\, i_g - V_D - v_o \end{cases} \qquad v_{L,reb} = \begin{cases} v_g & if \quad ON - state \\ v_g - (v_o + v_{xo}) & if \quad OFF - state \end{cases} \tag{4.22}$$

Hence, matching the average value in each switching period $\langle v_L \rangle$ and $\langle v_{L,reb} \rangle$:

$$\langle v_L \rangle = v_g - v_o\,(1-d) + \langle v_{par} \rangle = v_g - v_o\,(1-d) - v_{xo}\,(1-d) \tag{4.23}$$

Expression (4.23) defines the instantaneous value v_{xo}, which fulfill $\langle v_{par} \rangle = -v_{xo}\,(1-d)$:

$$v_{xo} = \frac{-\langle v_{par} \rangle}{1-d} = \frac{v_o\,(R_{on} + R_L) + V_D R_e - v_g\,(R_{on} - R_D)}{R_e - (R_{on} + R_L)} \tag{4.24}$$

Hence, with the same approximations considered previously, the EPE_o can be considered as a constant voltage source (presented in Fig. 4.8) with:

$$V_\beta = \frac{V_o\,(R_{on} + R_L) + V_D R_e - V_g\,(R_{on} - R_D)}{R_e - (R_{on} + R_L)} \tag{4.25}$$

Therefore, the behavior of the boost converter with parasitic elements can be modeled as is shown in Fig. 4.9. As it has been addressed before, the model has been obtained considering a sinusoidal $\langle i_g \rangle$ waveform, so it is only valid around the steady state operating point ($i_g = i_{reb}$, $V_o = V_{ref}$ and $\langle i_g \rangle = \frac{v_g}{R_e}$). But the aim of this model is showing how the influence of the parasitic elements in the sensorless PFC controller can be corrected adding the digital signal v_{dig}, in the output voltage data in the current estimator block, as is presented in Fig. 4.9.

Now, the expression that defines the value of the instant inductor voltage expressed in volts $v_{L,reb}$, is the next:

$$v_{L,reb} = \begin{cases} v_g \frac{q}{q_g} & if \quad ON - state \\ v_g \frac{q}{q_g} - (v_o - v_{dig} q_o)\, \frac{q}{q_o} & if \quad OFF - state \end{cases} \tag{4.26}$$

Figure 4.10 shows the current waveforms when $q v_{dig} = V_\beta$ for the same parameters used in the simulation shown in Fig. 4.3, where parasitic elements are not compensated. It can be observed that in this case $i_{reb} \approx i_g$, and the PF value increases to 0.997 with a lower current estimation error accumulated over the half line cycle around 30 mA.

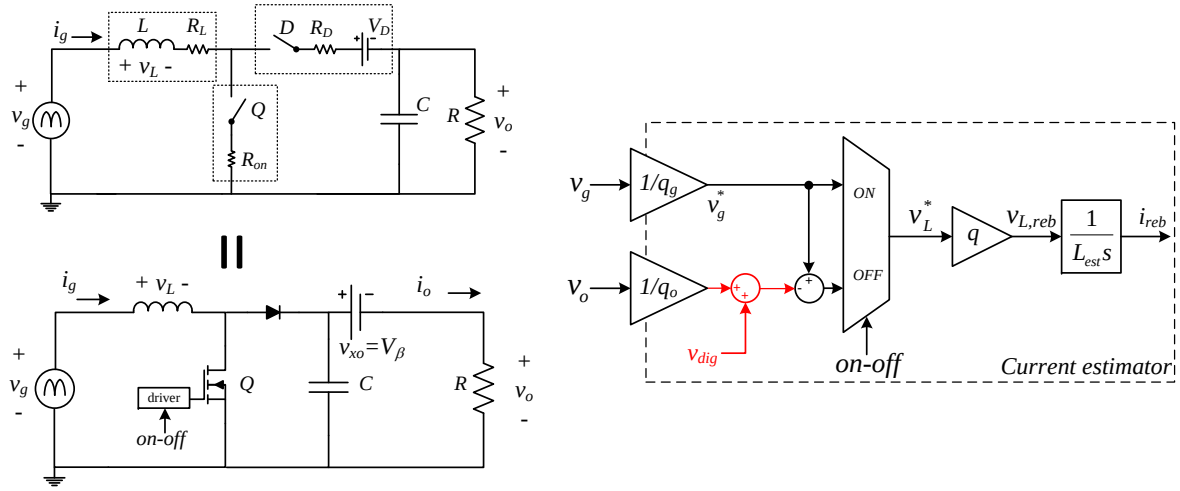


Figure 4.9: Left: Model of the Boost converter with the influence of the parasitic elements placed in series with the output voltage. Right: Behavioral model of the current estimator block with the digital compensation in the output voltage.

The current error estimation accumulated over n switching periods $i_{error}\,[n]$, can be obtained comparing (4.22) with (4.26), that yields:

$$i_{error}[n] = \frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_o[j]d'\,[j]\left(\frac{q_g}{q_o}-1\right)\right\} + \frac{T_{sw}}{L}\sum_{j=1}^{j=n}\left\{\left(qv_{dig}[j]-v_{xo}[j]\right)d'[j]\right\} \tag{4.27}$$

It can be seen that as it has been obtained in Section 4.1, i_{error} expression is an addition of the current error caused due to the errors in the data capture of the voltage across the inductor (first term), and the current error caused by the parasitic elements influence and its compensation. With a total compensation of the parasitic, $qv_{dig} = v_{xo}$, this second term is zero. Considering no errors in the voltage data capture ($v_g = v_g^* q$, $v_o = v_g^* q$, $q_g = q_o = q$) the current error generated by parasitic elements influence, and accumulated over n switching cycles, is given by:

$$i_{error}[n] = \frac{T_{sw}}{L}\sum_{j=1}^{j=n}\left\{\left(qv_{dig}[j]-v_{xo}[j]\right)d'[j]\right\} \tag{4.28}$$

One important aspect to consider at this point is the shape of the of the two terms of the exp. (4.27). Into the brackets of each term, they are the expressions presented in (4.29). The variables q_g and q_o are constants, and also qv_{dig} equal to V_β to compensate the voltage drop across the parasitic elements according to (4.25). The signals v_o and v_{xo} are constant with a small ripple, and the influence of $d' = 1 - d$ is the same in both terms, so the shape is the same for both terms.

$$(1^{st}\,term) = v_o[j]d'\,[j]\left(\frac{q_g}{q_o}-1\right)\,(2^{nd}\,term) = \left(qv_{dig}[j]-v_{xo}[j]\right)d'\,[j] \tag{4.29}$$

This concludes that with the addition of the signal v_{dig}, constant during an utility period in the current estimator block, it is possible to correct the errors caused by the parasitic elements, and also the mismatch between the LSB of the input voltage and the output

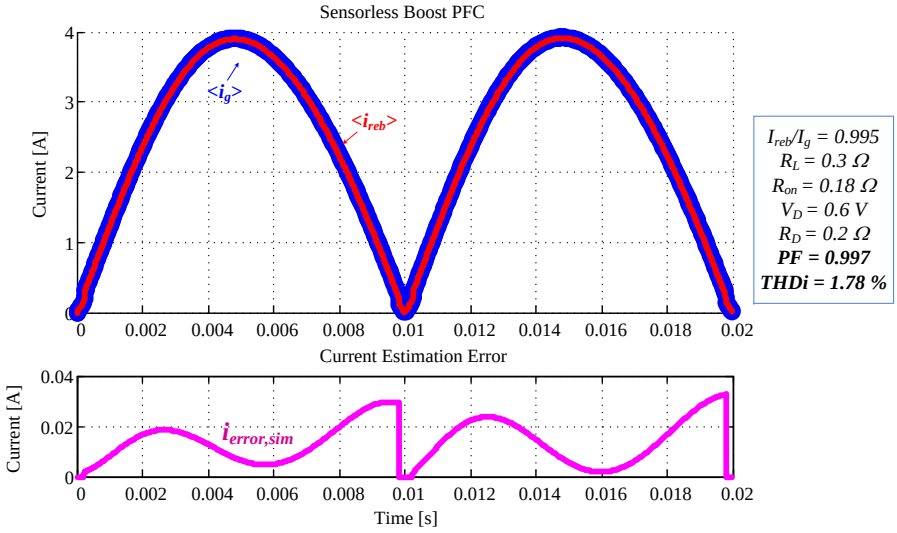


Figure 4.10: Simulated waveform for the Boost converter sensorless PFC controller when $qv_{dig} = V_\beta$.

voltage in the analog-to-digital conversion. Both sinks of error have the same effect, and then can be corrected or compensated in one way.

4.3 Chapter conclusion

Errors in the current estimation process due to the no compensation of the parasitic elements effect are studied an modeled in this Chapter, modeling their influence by the Equivalent Parasitic Element (EPE). The influence of the parasitics is a function of the operating conditions (input voltage, demanded power...). This is the main difference between this source of error and the one presented in Chapter 3 due to the mismatch between the LSB of the input voltage and the output voltage in the analog-to-digital conversion. This study is important to understand the modification of the digital current estimator with the digital signal v_{dig}, which enables the compensation of all the estimation errors in steady state.

Chapter 5

Digital controller implementation

In this Chapter the digital implementation of the controller is presented. Firstly, the input and output voltages quantization effects are taken into account to model each analog-to-digital converter in Simulink and plotting the current estimation error over a half-line cycle for different number of bits and sampling frequencies in the A/D converters. The current estimator block, previously presented, is simplified to be implemented in the digital device. The resolution of rebuilt current i_{reb}, expressed in bits, is obtained as a function of the digital clock period and the inductor value.

Furthermore, two compensation strategies for the compensation of all the current estimation errors are presented. The first one represents a time compensation with a reduced resolution called "feedforward" compensation, and the second one represents a voltage compensation, in which the resolution can be increased as necessary in the digital device. This compensation is called "feedback" because a new feedback loop is introduced to compensate all the current estimation errors.

5.1 Current rebuilding. Digital implementation and quantization effects

In Section 3.3.2, the current estimation error is modeled when a difference between the LSB resolution of the input and output voltages exists, defined as q_g and q_o respectively; representing the analog-to-digital conversion processes as a constant. This is not totally correct due to the sample and hold, and quantization processes in the v_g and v_o data acquisition process. To illustrate that aspect, Fig. 5.1 represents the analog-to-digital conversion of the input voltage (for v_o the analysis is totally the same).

The input voltage is adapted to the ADC specifications with a voltage resistive divider, obtaining v_g^s, that must be always lower than the analog range of the ADC, represented

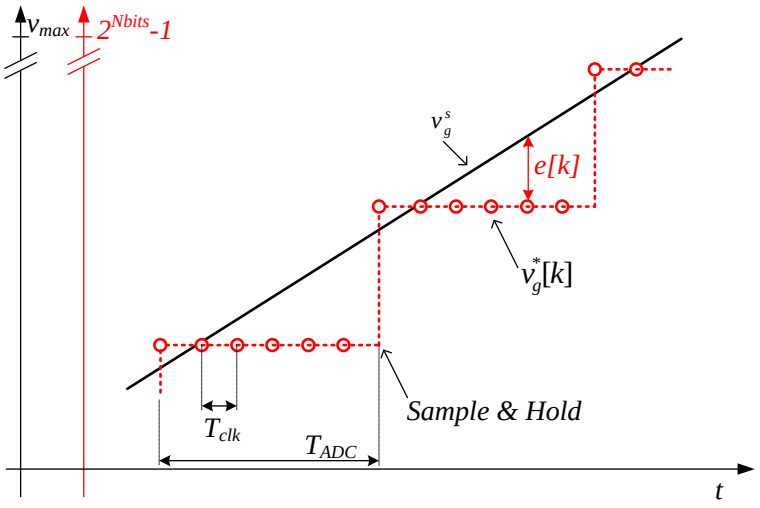


Figure 5.1: Representation of the analog-to-digital conversion of the input voltage.

by v_{max}. Therefore, if the ADC input voltage reaches v_{max}, the digital data will be $v_g^* = 2^{Nbits} - 1$. The sample and hold process is represented in Fig. 5.1 with the dotted line as a zero-order-hold (ZOH) sampler and the digital data of the voltage in red circles. This digital data $v_g^*[k]$, is used in the current estimator block where the current is computed every clock period k. Using the geometry of the Fig. 5.1, it can be written as:

$$v_g^*[k] + e[k] = \frac{2^{Nbits} - 1}{v_{max}} v_g^s = k_{adc}^g \frac{R_{g2}}{R_{g1} + R_{g2}} v_g = \frac{v_g}{q_g} \tag{5.1}$$

where $e[k]$ represents the quantization error in bits caused due to the analog-to-digital conversion in the clock period k. A new variable is defined to represent the relation between v_g and the instantaneous input voltage data $v_g^*[k]$, in the clock period k, $q_g^{'}[k]$:

$$q_g^{'}[k] = \frac{v_g}{v_g^*[k]} = \frac{v_g}{\frac{v_g}{q_g} - e[k]} = \frac{v_g q_g}{v_g - q_g e[k]} \tag{5.2}$$

The same expression is obtained for the output voltage analog-to-digital conversion, obtaining:

$$q_o^{'}[k] = \frac{v_o}{v_o^*[k]} = \frac{v_o}{\frac{v_o}{q_o} - e[k]} = \frac{v_o q_o}{v_o - q_o e[k]} \tag{5.3}$$

remembering that q_g and q_o represents the input and output analog-to-digital conversion as an ideal constant, respectively. Substituting these constants by $q_g^{'}[k]$ and $q_o^{'}[k]$ in the expressions that define i_{error} in the Chapter 3, $i_{error}(t)$ is rewritten as:

$$i_{error}(t) = \frac{V_g\sqrt{2}}{L} \int_0^t \left\{ \left(1 - \frac{q_o^{'}(t)}{q_g^{'}(t)} \right) sin\,(\omega t) \right\} dt \tag{5.4}$$

To simulate the current error generated, due to the A/D conversion error e, both analog-to-digital converters are modeled in Simulink as is shown in Fig. 5.2a, by a Transport delay block, a Zero-Order Hold block that samples the voltage signal, and a Quantizer block whose

quantization interval equals the LSB value in volts q_g, of the ADC [152]. In Fig. 5.2b different i_{error} waveforms are plotted for different bits of resolution of the input and output ADCs. Both voltage dividers have been defined to measure voltages up to 473 V (a maximum of 5 V in the control circuit, that represents the high level in the digital device), with a delay in the Transport Delay block of 500 ns and a sample frequency in the ZOH block of 1 MHz . The i_{error} waveform is quasi-sinusoidal for $Nbits \geq 10$ and is distorted for a lower number of bits. For a higher number of bits, the delay and the sample frequency of the ADC are the predominant factors that set i_{error}. In Fig. 5.2c the dependency of i_{error} for different ADC sampling frequencies f_{ADC}, with $Nbits = 10$, is shown. All of these graphs have been plotted for an input voltage of $V_g = 230\ V_{rms}$ (50 Hz) and an output voltage of 400 Vdc. To have a quasi-sinusoidal i_{error} waveform is valid for the sensorless controller, not introducing current distortion in the system.

Expression (5.5) defines the instantaneous inductor current, being $\triangle t$ the integration time and v_L the inductor voltage.

$$i_L\left(t+\triangle t\right) = i_L\left(t\right) + \int_{t}^{t+\triangle t} \frac{v_L}{L} dt \tag{5.5}$$

The voltage across the inductor v_L, is defined by the converter topology and the state of the converter (ON- or OFF-state) as is presented in Section 2.4.1. Equation (5.5) is translated into finite difference equation, to be implemented in the digital device according to (5.6). The integration time is given by the clock period of the digital device T_{clk} , setting the rebuilding update frequency $f_{clk} = 1/T_{clk}$, and the resolution of the pulse-width modulation (PWM). Therefore, the rebuilding technique is more appropriate for custom hardware (FPGA or ASIC) implementation than for DSP or microcontroller [14, 114, 135].

$$i_{reb}\left[k+1\right] = i_{reb}\left[k\right] + \frac{v_L\left[k\right]}{L} T_{clk} = i_{reb}\left[k\right] + \frac{v_L^*\left[k\right] q_g}{L} T_{clk}, \tag{5.6}$$

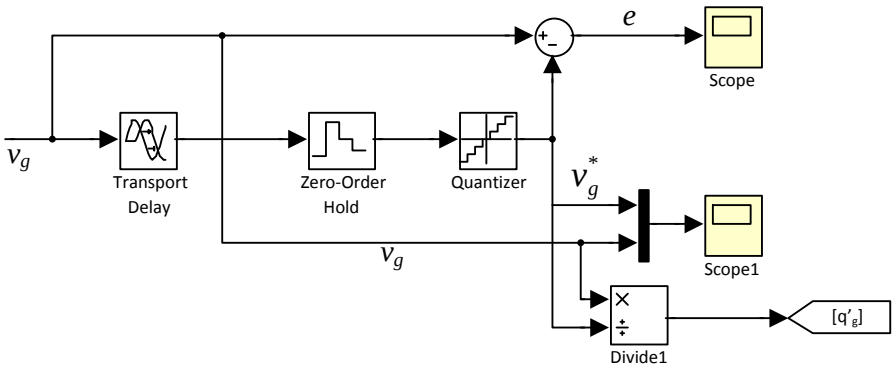
The ON- and OFF-times are known within the controller because the driving signal is generated there, and q_g and L are constant values, so a simple accumulator can represent the rebuilt input current i_{reb} according to (5.7) as is presented in Fig. 5.3a.

$$i_{reb}[k+1] = i_{reb}[k] + \begin{cases} v_g^*\left[k\right] & ON-state \\ v_g^*\left[k\right] - v_o^*\left[k\right] & OFF-state \end{cases} \tag{5.7}$$

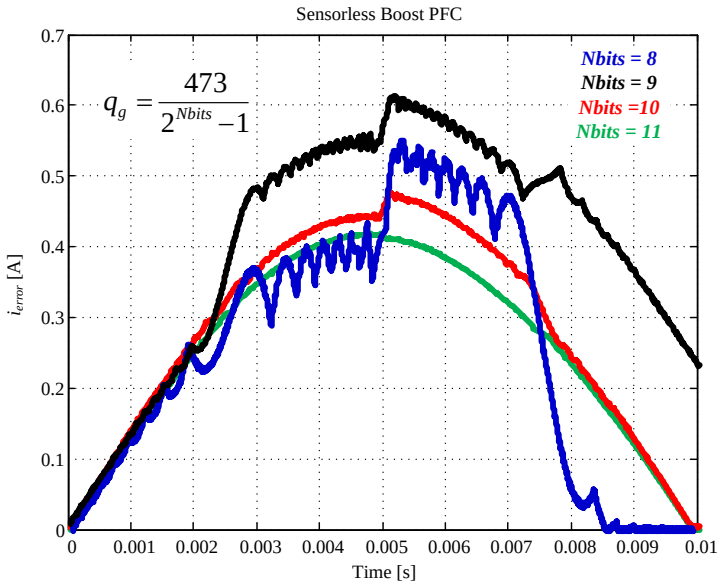
with the waveforms shown in Fig. 5.3b . Hence, now the value of i_{reb} is represented in bits, with a different scale of i_g. The value in amps of the LSB of the current is given by:

$$q_i = \frac{i_g[A]}{i_{reb}[bit]} = \frac{\sum \frac{v_L[k]}{L} T_{clk}}{\sum v_L^*\left[k\right]} = q_g \frac{T_{clk}}{L}\ \frac{A}{bit} \tag{5.8}$$

With this constant q_i, it is possible to implement the current estimator block only as an ac-



(a)



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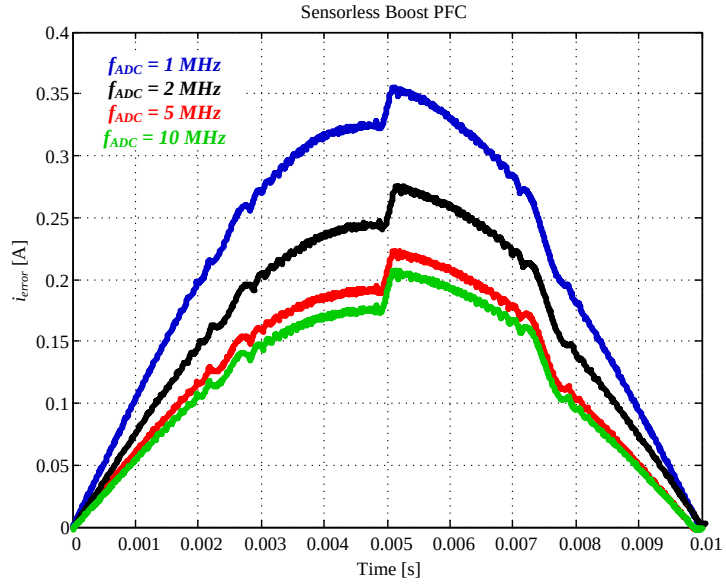
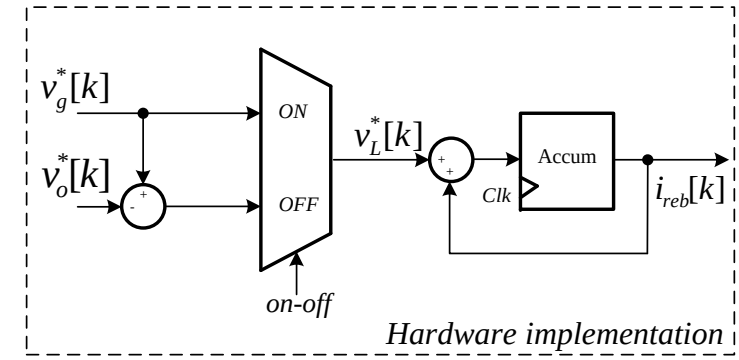
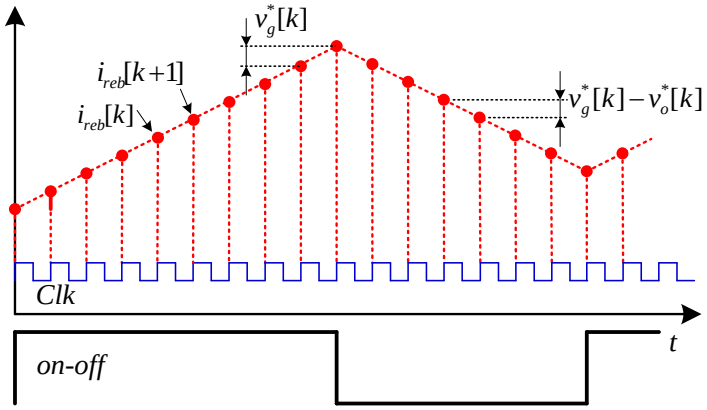


(c)

Figure 5.2: (a) Simulink model of the input voltage ADC, (b) i_{error} waveform over half utility period for different bits of resolution in the ADCs with a constant ADC sample frequency of f_{ADC} =1 MHz, and (c) for different ADC sampling frequencies and a constant $Nbits = 10$.



(a)



(b)

Figure 5.3: Current rebuilding concept. (a) Hardware architecture and (b) digital waveforms.

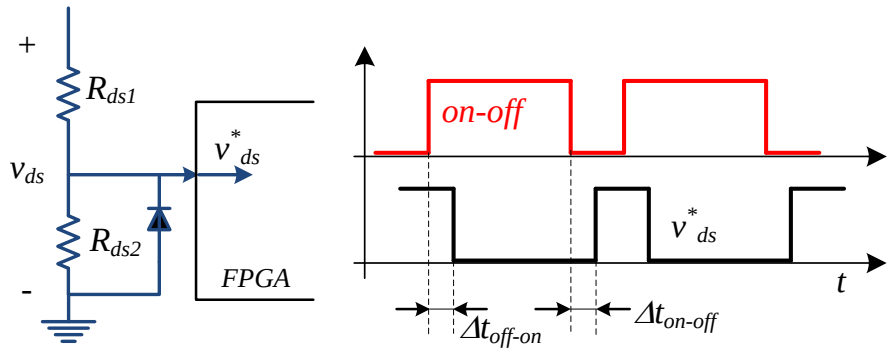


Figure 5.4: Auxiliary circuit to adapt the drain-to-source voltage as a digital signal. Comparison with the $on-off$ signal and the drive signal's delays $\triangle t_{on-off}$ and $\triangle t_{off-on}$.

cumulator without multiplications or divisions, optimizing the resources of the digital device. It can be seen in (5.8) how the clock period of the digital device and the inductance define the resolution of the current estimator. High f_{clk} and L values benefit the behavior of the estimator, but increases its cost and volume, and vice-verse.

5.2 Drive signal delays compensation. Feedforward compensation in terms of time (clock cycles)

Two compensation strategies, working at the same time, are presented in this Chapter. The first one is the time compensation. The ON-time error $\triangle t_{on}[j]$, is measured (indirectly) every switching period j, and is compensated by accounting for it when the digital circuit calculates the required ON-time every switching period.

An auxiliary circuit, which includes a resistor divider and a signal diode, is used to detect the drain-to-source voltage drop across the power MOSFET and obtain the digital signal v^*_{ds}, which indicates the real ON-OFF transitions in the boost converter, as is presented in Fig. 5.4.

The digital controller compares the signal $on-off$ with the signal v^*_{ds} to measure the ON-time modification every switching period j, in terms of clock periods of the digital circuit, defined as $\triangle t^{meas}_{on}[j]$:

$$\triangle t^{meas}_{on}[j] \approx \triangle t_{on}[j] = \triangle t_{on-off}[j] - \triangle t_{off-on}[j] \tag{5.9}$$

The resolution of the $\triangle t^{meas}_{on}[j]$ measurement depends on the clock period of the digital device, and $\triangle t_{on}[j]$ represents the real ON-time modification in the same switching period j. This strategy constitutes a coarse and fast feedforward compensation of the volt-second/current errors caused due to time errors. The original control algorithm is modified to use the measured ON-time modification, and self-compensates the duty cycle in each switching period T_{sw}.

The NLC control algorithm compensation is achieved advancing the ON-to-OFF transition

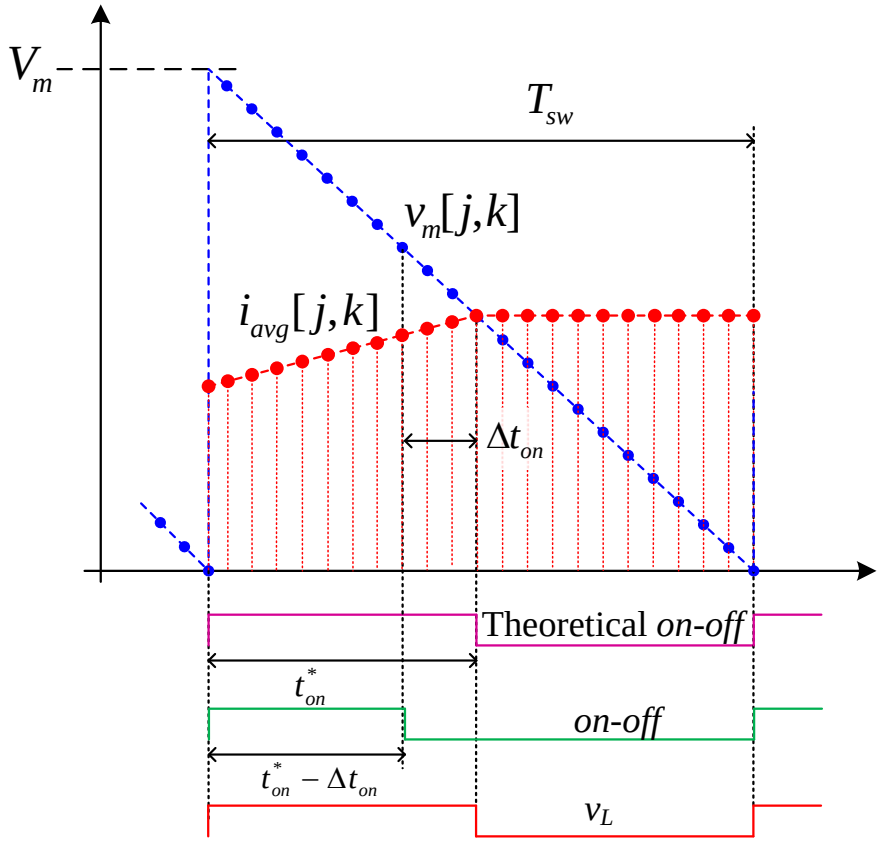


Figure 5.5: Compensated NLC control algorithm.

of the $on-off$ signal with respect the theoretical one. Figure 5.5 shows this compensation technique. When the converter is operating in the switching period j, the controller has the ON-time modification measurement of the previous period $\triangle t_{on}^{meas}[j-1]$. The theoretical ON-time $t_{on}^*[j]$, is decreased the quantity $\triangle t_{on}^{meas}[j-1]$, being $t_{on}^*[j] - \triangle t_{on}^{meas}[j-1]$ the ON-time of the $on-off$ signal that drives the MOSFET. Once the $on-off$ signal travels through the driver and switch, the real ON-time on the converter (given by v_L) is given by:

$$t_{on} = t_{on}^*[j] - \triangle t_{on}^{meas}[j-1] + \triangle t_{on}[j] \tag{5.10}$$

Considering $\triangle t_{on}^{meas}[j-1] \approx \triangle t_{on}[j]$, which is the desired behavior, the ON-time estimated in the digital device and the ON-time of the real converter are equal, compensating the current error estimation caused due to time errors.

As it has been addressed before, the resolution of the $\triangle t_{on}^{meas}$ measurement depends on the digital device clock frequency $f_{clk} = 1/T_{clk}$. Therefore, a small difference exists between $\triangle t_{on}^{meas}$ and $\triangle t_{on}$, around $\pm T_{clk}/2$. With this compensation technique, the current estimation error, accumulated over n switching periods, is rewritten as:

$$i_{error}\,[n] = \sum_{j=1}^{j=n} \frac{v_o\,[j]}{L}\left(\Delta t_{on}\,[j] - \triangle t_{on}^{meas}[j-1]\right) \tag{5.11}$$

Considering $\triangle t_{on}^{meas}[j-1] - \triangle t_{on}[j] = \pm T_{clk}/2$ constant (and with the same sign) every switching period, for a switching frequency of 100 kHz, a DC output voltage of 400 Vdc, and a inductance 1 mH working under an European Grid (50 Hz), the current estimation error accumulated over the half line cycle $T_u/2$, is given by:

$$i_{error}\,[n_u] = \pm\frac{V_o T_{clk}}{2L}\frac{T_u/2}{T_{sw}} = \pm\frac{V_o T_{clk} T_u}{4LT_{sw}} = \pm 2\ A \tag{5.12}$$

being n_u the number of switching periods in a half-line period. The clock frequency of the digital circuit limits the resolution of the feedforward error compensation in absolute terms because it fixes the minimum value of the term $\Delta t_{on}\,[j] - \triangle t_{on}^{meas}[j-1]$. Considering the duty-cycle as the parameter to be adjusted to compensate for the estimation errors, the ratio between the clock frequency and the converter switching frequency is the actual limitation for the resolution of the feedforward compensation. The higher is f_{sw}, the higher the influence in the current estimation error.

Due to this limitation of the compensation resolution and the feedforward nature of the algorithm, zero current estimation error is not assured. A feedback control with fine compensation and higher resolution is applied to fully correct the current estimation error and presented in the last section of this Chapter.

5.3 Discontinuous Conduction Auxiliary Detection Circuit

Accumulated current estimation error over the half-line cycle causes input current distortion, decreasing the power factor value. As it has been shown in previous Chapters, where the current estimations errors are defined, the time in which the discontinuous conduction mode (DCM) occurs is a parameter that enables an indirect detection of discrepancy between i_{reb} and i_g.

An auxiliary circuit, capable of detecting the converter mode of operation (CCM or DCM) without using the current variable measurement, is used to evaluate this discrepancy. Figure 5.6 shows the hardware architecture (Fig. 5.6a) and the circuit behavior (Fig. 5.6b). A digital signal $DCMi_g$, indicates the converter operation mode by its logic level (e.g. $DCMi_g$ = "0" for the CCM operation and $DCMi_g$ = "1" for the DCM operation). This circuit, similar to the one described in [41] and [87], compares the output voltage v_o, with the MOSFET drain-to-source voltage v_{ds} (that is used at the same time to measure the drive signal's delays), adapted with two equal resistors ($R_{ds1} = R_a$, $R_{ds2} = R_b$), with an analog comparator. In CCM operation $v_{ds} > v_o$ (due to the influence of the parasitic elements of the diode) during the whole OFF-time, but this is not true in the DCM operation. Drain-to-source voltage v_{ds}, adopts a value close to the input voltage as soon as input current i_g reaches zero. But inherited parasitic elements of the power switches cause oscillations in the drain-to-source voltage around v_g [153]. The analog comparator output signal x_1, is registered at the beginning of the switching period using the $on-off$ signal rising edge, that is internally

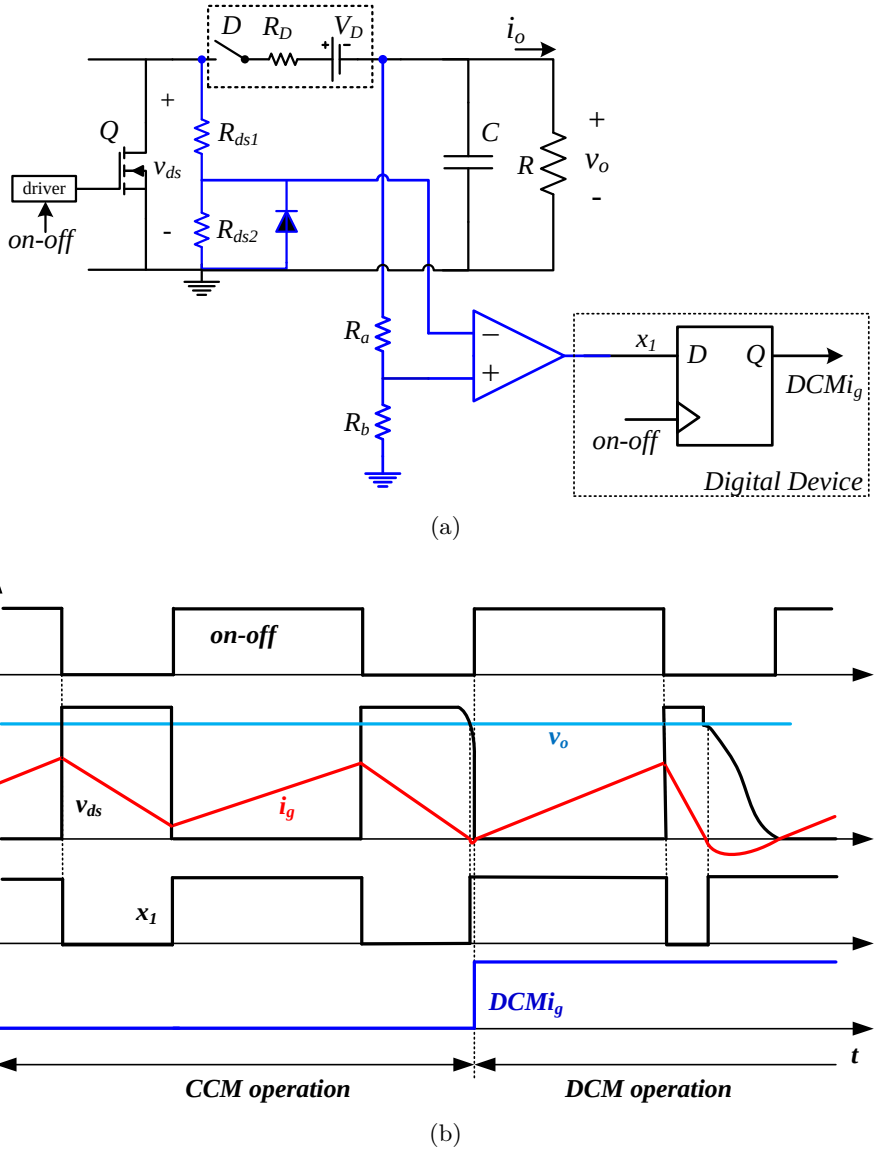


Figure 5.6: DCM condition detection auxiliary circuit for the real input current i_g. (a) Hardware architecture. (b) Circuit waveforms

available in the digital device. If x_1 is high at this sample instant, the boost converter is operating in DCM ($DCMi_g$ = "1"). Conversely, if sample x_1 is low, the converter is operating in CCM ($DCMi_g$ = "0").

In the case of the digitally rebuilt input current i_{reb}, the DCM detection is carried out internally in the digital circuit. The digital signals involved in the DCM detection are presented in Fig. 5.7. The signal $DCMi_{reb}$ indicates if $i_{reb} = 0$ at the beginning of the switching period (DCM operation is estimated and $DCMi_{reb}$ = "1") or not (DCM operation is estimated and $DCMi_{reb}$ = "0"). A digital comparison, with the threshold tuned at zero level, is performed every rising edge of the signal $on - off$.

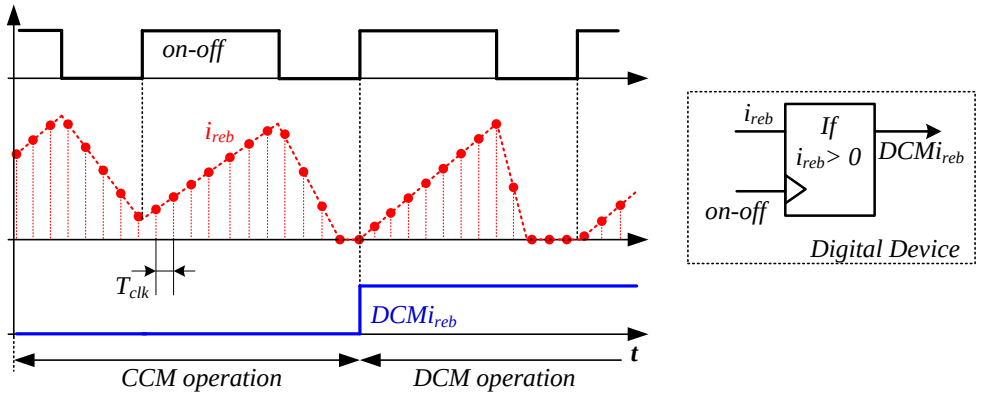


Figure 5.7: DCM condition digital detection for the rebuilt input current i_{reb}. Left: digital signals and, right: hardware architecture in the digital device.

5.4 Feedback compensation of the DCM time discrepancy

In the PFC circuits presented recently like [14, 102, 130, 134, 135, 154, 155] the input current measurement is avoided and a PFC digital control which includes the measurement of the parasitic elements R_L, R_{on}, V_D and R_D is proposed, taking into account those elements in the digital controller to compute a duty cycle command d; or simply neglecting their influence. But parasitics change with the temperature, frequency and the components used in the PFC converter.

It can be observed that in these previous solutions for the sensorless PFC controllers, the use of high inductance and low switching frequencies are required, in comparison with the state-of-art of CCM PFCs converters that include a current sensor, decreasing the influence of the considered R_L, R_{on}, V_D and R_D values, and the real ones.

All the situations that produce a current estimation error, are analyzed in Chapters 3 and 4 and have a similar i_{error} waveform, due to the accumulation of small error every switching period. The feedforward compensation, previously presented, has as bottleneck the digital device clock period, and it does not assure zero current estimation error. The resolution of the compensation is around ±5 ns, resulting a current estimation error accumulated over n switching periods:

$$i_{error}\,[n] = \sum_{j=1}^{j=n} \frac{v_o\,[j]}{L}\left(\triangle t_{on}\,[j] - \triangle t_{on}^{meas}[j-1]\right) = \sum_{j=1}^{j=n} \frac{v_o\,[j]}{L} \times \left(\pm\frac{T_{clk}}{2}\right) \tag{5.13}$$

In Chapter 4 it is explained how a signal v_{dig} added in the current estimator block is added to compensate the current estimation error caused due to the influence of the parasitic elements as

$$i_{error}[n] = \frac{T_{sw}}{L} \sum_{j=1}^{j=n} \left\{\left(q_g v_{dig}[j] - v_{xo}[j]\right) d'[j]\right\} \tag{5.14}$$

where v_{xo} is defined by (4.24). Figure 5.8 shows the current estimation error due to a constant + 5 ns (with T_{clk}= 10 ns) time error in the feedforward compensation, labeled as

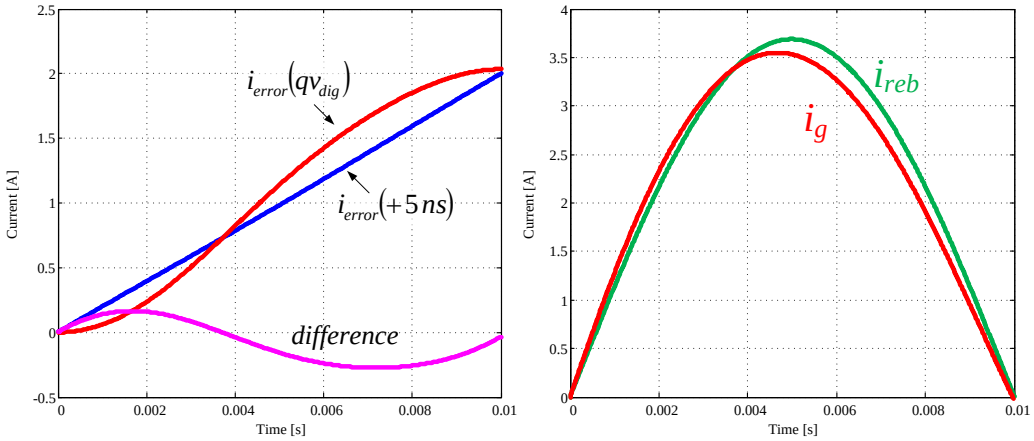


Figure 5.8: Left: Current estimation error generated by + 5 ns (with T_{clk}= 10 ns) of time error compensation (in blue) and due to a qv_{dig} value that cause the same estimation error at the end of the half line period (in red). In magenta is plotted the difference between the two current estimation errors. Right: i_{reb} and i_g current in this case

$i_{error}(+5\,ns)$. In red, the current error due to qv_{dig} is plotted. It causes a current estimation error $i_{error}(qv_{dig})$, which compensates $i_{error}(+5\,ns)$ at the end of the half utility period. In magenta, the difference between these two currents is plotted. This difference is added to the i_{reb} signal to obtain the real input current represented in red in the right side of the figure, i_g (i_{reb} is the variable controlled by the PFC controller, i.e. is sinusoidal). It can be seen that although $i_{error}(qv_{dig})$ and $i_{error}(+5\,ns)$ are not totally equal, the difference between them is small and i_g has low distortion.

The aim of this compensation technique is to increase the resolution of the signal v_{dig}, so with v_{dig} not only the parasitic elements influence is compensated, but the errors due to the small resolution of $\pm T_{clk}/2$ in the feedforward compensation are compensated too. The current estimation error for a constant given value of v_{dig} is given by (5.14), and is approached to zero if $v_{dig} = V_\beta/q_g$ as is presented in Fig. 4.10 of Chapter 4. But v_{dig} has a finite resolution, so the digital controller sets a value $v_{dig} = V_\beta/q_g \pm 0.5\,LSB$. This 1 LSB uncertainty in v_{dig} represents a current estimation error i_{error}, over the half line cycle. This error is plotted in Fig. 5.9, with the boost converter parameters previously presented. It can be seen that this compensation in terms of volts can be implemented with the required resolution in the current estimation error, for example, of one order of magnitude higher than the feedforward compensation (that results in i_{error} at the end of the half line cycle of ± 2 A), as it has been presented previously.

This higher resolution is achieved without the necessity of a high resolution ADC. As is presented in Fig. 5.10, in this case a 10-bit ADC is used for the input and output voltages ($v_g^*[k]$ and $v_o^*[k]$), and 4 LSBs are concatenated to obtain a 14 bits length. The signal v_{dig} is 14-bits length to have the resolution needed in i_{error}, and is added to $v_o^*[k]$. With this approach, the resolution can be increased by adding more LSBs in v_{dig}, without any extra cost. Only the utilized resources of the digital devices minimally increases. The value of v_{dig} is function of the demanded power, and then, some extra information is needed to set its

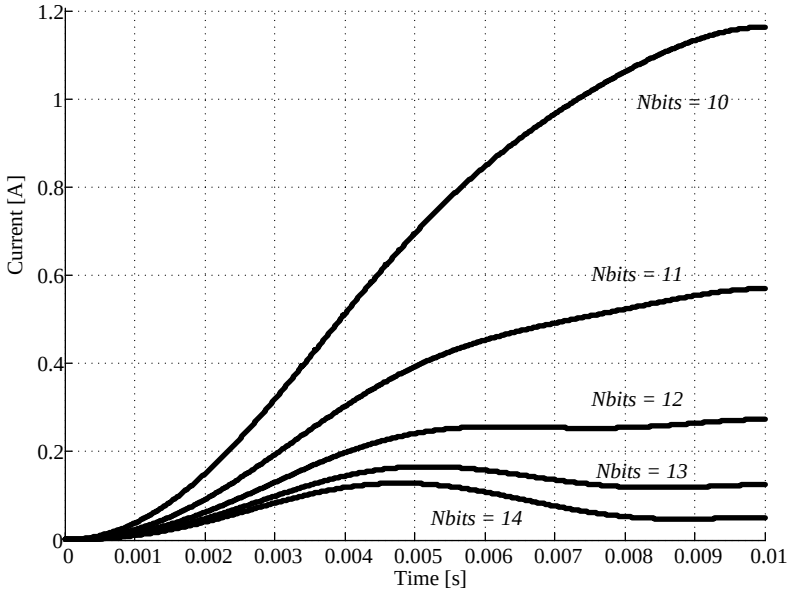


Figure 5.9: Minimum current estimation error due to the resolution of $\pm 0.5\, LSB$ in the digital control signal v_{dig}.

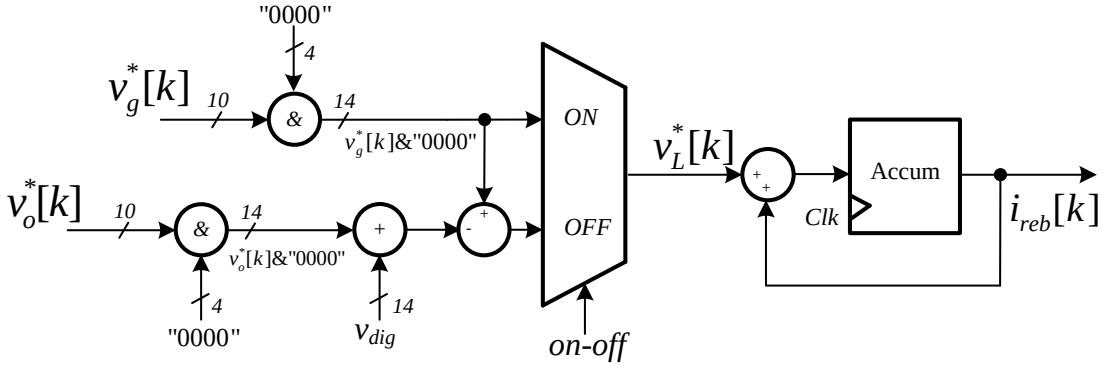


Figure 5.10: Current estimator hardware implementation with higher resolution.

value automatically. This needed information is the current estimation error, that creates a difference between the DCM time of i_{reb}, and the DCM of i_g over the half line cycle. Therefore, these DCM times are used in a new proposed feedback loop to set v_{dig} in steady state.

The estimated input current i_{reb}, has DCM time defined as T^{reb}_{DCM}, and i_g has a different DCM time T^{g}_{DCM}. A distortion in i_g leads to $T^{reb}_{DCM} \neq T^{g}_{DCM}$ reducing the power factor value. This controller captures $DCMi_g$ and $DCMi_{reb}$ as it has been presented in Section 5.3 and, measures and compares T^{reb}_{DCM} and T^{g}_{DCM}, which correspond with the period of the half line cycle in which $DCMi_{reb}$ and $DCMi_g$ are active, respectively. DCM time error e_{DCM}, is defined by the expression (5.15).

$$e_{DCM} = T^{reb}_{DCM} - T^{g}_{DCM} \tag{5.15}$$

Thus, an indirect measurement of the current estimation error is obtained by e_{DCM}.

As a real example, Figs. 5.11 and 5.12 show some real situations of the converter during operation. Figure 5.11 shows two compensation situations for different values of v_{dig} when current estimation error exists. It can be seen that these waveforms are is correspondence with the simulated waveforms shown in Chapter 3 (Fig. 3.14 and 3.15). If $e_{DCM} < 0$ is because $i_{reb} > i_g$ and $q_g v_{dig} < V_\beta$, so it is necessary to increase v_{dig}, and then decrease i_{reb} to match the DCM times of the input and rebuilt input current. On the other hand, if $e_{DCM} > 0$ is because $i_{reb} < i_g$ and $q_g v_{dig} > V_\beta$, in which it is necessary to decrease v_{dig}, to increase i_{reb}.

The value of T^{g}_{DCM}, e_{DCM} and PF for different values of v_{dig} is plotted in Fig. 5.12. The value of T^{g}_{DCM} and e_{DCM} is represented in terms of switching cycles (with $f_{sw} = 72\,kHz$). It can be seen how the maximum PF is achieved for the minimum T^{g}_{DCM}, and with a e_{DCM} close to zero, but slightly negative. This is because the auxiliary circuit used to measure the DCM in i_g with the drain-to-source voltage data is not so accurate as the DCM detection in i_{reb} (completely digital), because the v_{ds} presents a small difference with respect the ideal counterpart. Therefore, an offset measured experimentally is introduced to compensate the negative e_{DCM} value, and is the same for all the conditions presented in the experimental validation (Chapter 8)

To obtain an universal PFC controller that compensates all the current estimation errors, the proposed new feedback loop adjust v_{dig} to match $T^{reb}_{DCM} = T^{g}_{DCM}$. A block diagram of the proposed control loop is presented in Fig. 5.13. The DCM time error e_{DCM} is the input of a PID compensator, which adjust internally the value of the signal v_{dig} until DCM times match, i.e. $e_{DCM} = 0$.

This feedback loop, modeled in Chapter 6, allows a universality of the digital controller for sensorless Boost CCM power factor correction stages based on current rebuilding concept. The term "Universal" is used because the DCM time feedback loop compensates for the estimation errors which are sensitive to the input voltage specifications and power conversion rate. Therefore, the digital controller extends the operation range in comparison with the

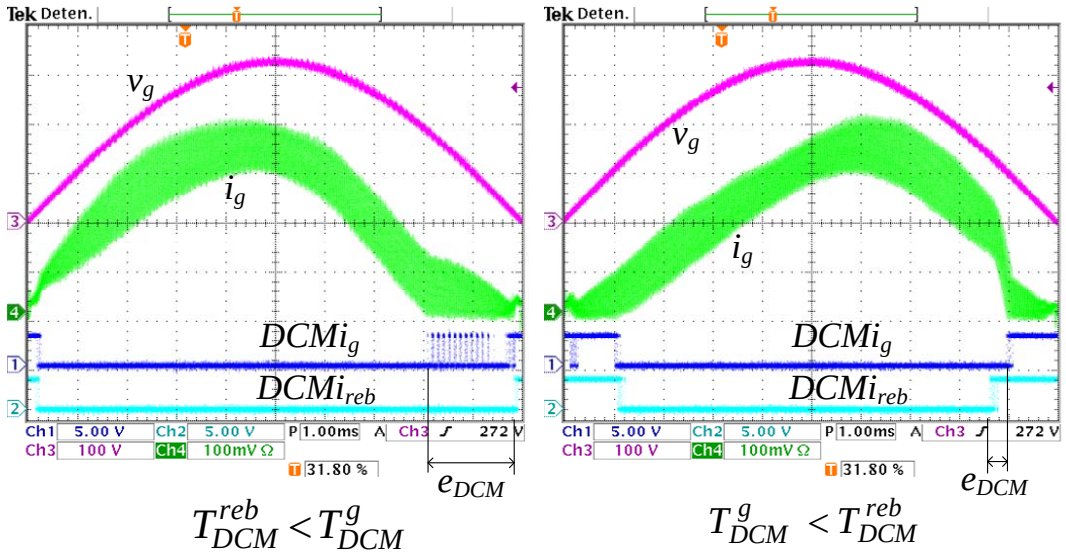


Figure 5.11: Real waveforms. Input voltage v_g, real input current i_g, waveforms and digital signals $DCMi_g$ and $DCMi_{reb}$ for: Left: $e_{DCM} < 0$, and then $i_{reb} > i_g$. Right: $e_{DCM} > 0$ and $i_{reb} < i_g$.

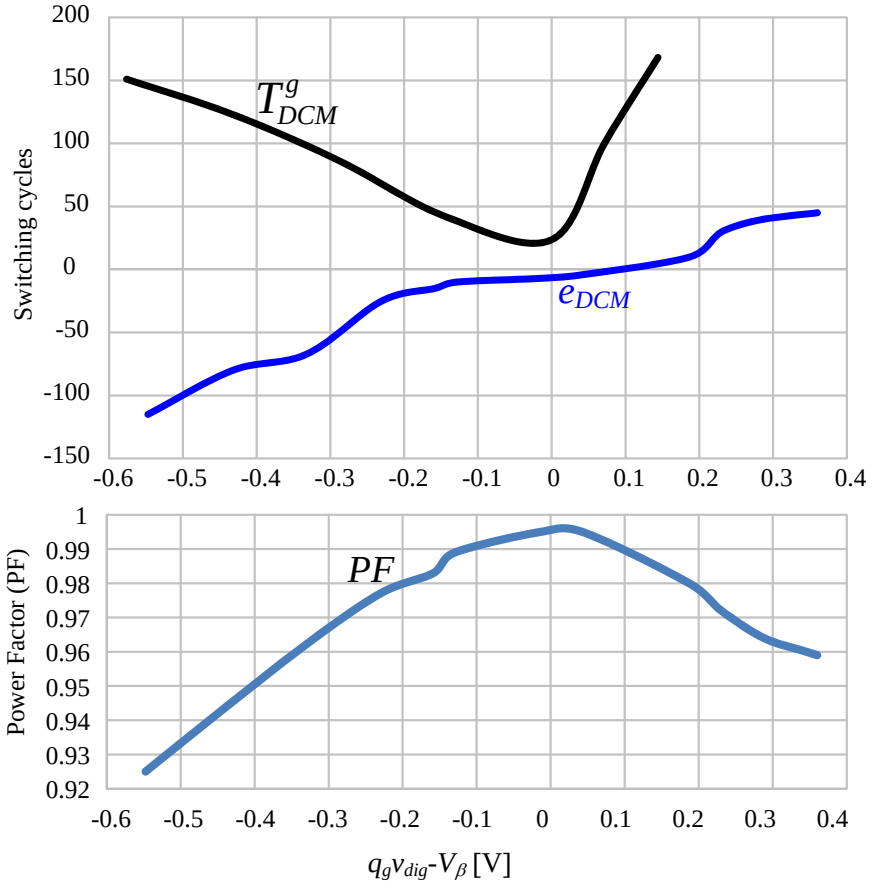


Figure 5.12: Experimental results. Top: DCM time of the input current T^g_{DCM}, and DCM time error e_{DCM} vs $q_g v_{dig} - V_\beta$. Bottom: PF vs $q_g v_{dig} - V_\beta$.

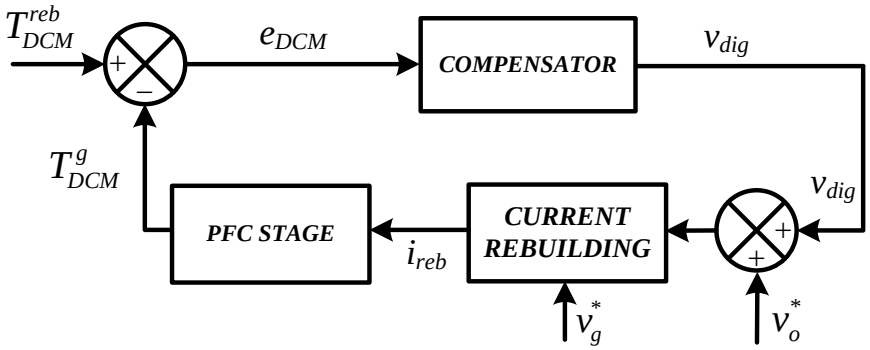


Figure 5.13: Block diagram of the DCM times compensation controller.

previous solutions/approaches presented in sensorless Boost CCM PFC controllers [14, 102, 130, 134, 135, 154, 155] .

In a PFC controller working in the CCM, the DCM condition appears around the AC line zero crossings, where the duty cycle is ideally $d = 1$, but in the real implementation is saturated (for example $D_{max} = 0.95$). Therefore, under this conditions, T^{reb}_{DCM} is constant at different power levels, and is used as reference. The compensator modifies the value of v_{dig} used in the digital current estimator (Fig. 5.10). With the i_{reb} value, the duty cycle command is obtained and applied to the power stage. The real input current waveform has a DCM time equal to T^{g}_{DCM}, which is compared with the reference T^{reb}_{DCM} generating the DCM time error e_{DCM}, which is the input of the compensator block.

5.5 Chapter conclusion

The quantization aspects of the estimator are analyzed in this Chapter. The error between the estimated and actual DCM periods close to the zero crossing of the input voltage is a key variable to accurately correct the error in the estimation of the input current and the consequent distortion.

An auxiliary circuit detects indirectly DCM condition in the input current comparing drain-to-source voltage with the output voltage during the MOSFET OFF-time. The single digital signal acquired from the MOSFET drain-to-source voltage drop is used by both, the feedforward and feedback compensator.

A feedforward and a feedback error compensation strategies, combining resolution and speed are presented, in which the current estimation error is canceled using a twofold strategy: the feedforward one represents a coarse compensation of current estimation errors due to time delays. And the new DCM time feedback loop generates a constant digital signal to compensate current estimation errors, modifying the output voltage measurement used to estimate the input current, and minimizes this DCM time error. This feedback loop sets the value of the digital signal even if the converter operates in a wide load or voltage range with a high resolution.

Chapter 6

Model of the high-resolution error compensator. Steady-state gain and low bandwidth model

The traditional approach for a PFC controller uses two control loops. One fast "inner" loop controls the current waveform, with the goal of obtaining a sinusoidal shape (in this work the controlled current by this loop is i_{reb}). And the second one is an "outer" voltage loop with a low bandwidth whose function is the control of the output voltage according to a reference value, demanding the desired power from the AC line.

In this system, a new feedback loop is introduced, whose target is to match the DCM times of the rebuilt input current and the real one, modifying the value of a digital signal v_{dig} used in the current rebuilding algorithm to cancel the current estimation error. This Chapter presents a complete model of the system under control (plant) in the time and frequency domain as a function of the control signal v_{dig}, identifying the DC steady-state values of the involved variables, and the small signal AC system model.

As presented before, the new feedback loop varies the digital signal v_{dig} according to the difference between the DCM times of the real input current i_g, and the rebuilt input current i_{reb}. This time difference constitutes an error signal which is an indirect measurement of the current estimation error.

6.1 Steady state model. DC analysis

In a single phase AC-DC rectifier, resistive emulator behavior loading the utility voltage is desired. With this, the AC line current and voltage are proportional achieving unity power

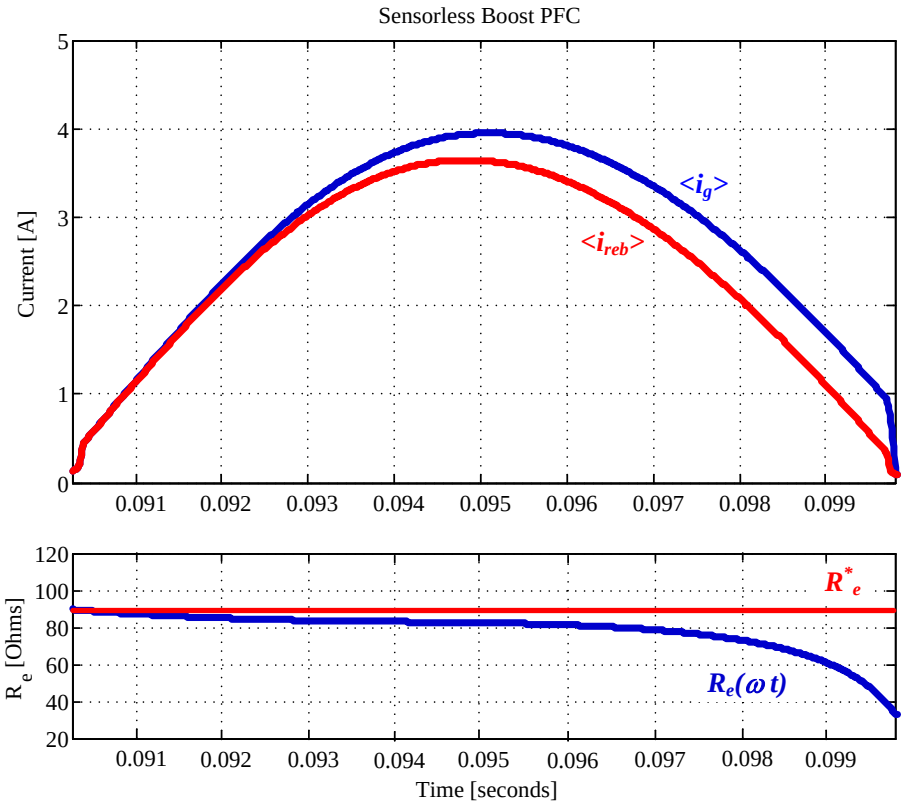


Figure 6.1: Current waveforms with current error estimation (top) and emulated resistances (real and digital) under this condition (bottom), over the half line cycle.

factor. In this work, there are two different signals in the system meaning line current: the real input current i_g, and the rebuilt or estimated input current i_{reb}. Typical current waveforms for a given power command, with not null current estimation error are presented in Fig. 6.1.

The variable controlled by the NLC control is the estimated input current (i_{reb}) which will be always proportional to v_g according to the PFC control law. On the other hand, i_g is not sinusoidal due to the estimation error i_{error}. So in this system, two different emulated resistances are defined R_e and R_e^* which are the real and digital emulated resistances, respectively; both defined by (6.1), where V_g and I_{reb} are the RMS values of v_g and i_{reb}, respectively. The instantaneous values of R_e and R_e^* are shown in Fig. 6.1 over the half line cycle. It can be seen that R_e^* is constant, while R_e depends on the estimation error $R_e = R_e(\omega t)$.

$$R_e(\omega t) = \frac{v_g}{\langle i_g \rangle}; \qquad R_e^* = \frac{v_g}{\langle i_{reb} \rangle} = \frac{V_g}{I_{reb}} \tag{6.1}$$

It has been stated before that:

$$i_g = i_{reb} + i_{error} \tag{6.2}$$

To develop the model of the plant, different assumptions are considered: 1) At the operation point, the output voltage is constant, due to the action of the voltage loop, and the voltage ripple is neglected, so $v_o = V_o = V_{ref}$ and $\Delta v_o \approx 0$. 2) The rebuilt input current i_{reb},

operates in the CCM over the whole half-line cycle, so the duty cycle command is given by the quasisteady-state characteristic of the boost converter: $d = 1 - \frac{v_g}{V_o}$. 3) The feedforward compensation has no error (i.e. $\triangle t_{on}^{meas} = \triangle t_{on}$).

The new feedback control loop has a low bandwidth, so the signal v_{dig} is considered constant over the half line cycle. The influence of the parasitic elements is modeled with the equivalent parasitic element in series with the output voltage, EPE_o, (Section 4.2), by a constant voltage drop over the half line cycle $V_\beta \approx v_{xo}$, given by (4.25) and rewritten in this Chapter:

$$V_\beta = \frac{V_o\left(R_{on} + R_L\right) + V_D R_e - V_g\left(R_{on} - R_D\right)}{R_e - \left(R_{on} + R_L\right)} \tag{6.3}$$

considering the system is around the steady operating point. With $R_e^* \approx R_e(\omega t)$. The current estimation error i_{error}, accumulated over n switching periods for a given value of v_{dig}, is given by (4.27) and remembered here in (6.4):

$$i_{error}[n] = \frac{T_{sw}}{L}\sum_{j=1}^{j=n}\left\{\left(qv_{dig}[j] - v_{xo}[j]\right)d'[j]\right\} \approx \frac{T_{sw}}{L}\sum_{j=1}^{j=n}\left\{\left(qv_{dig} - V_\beta\right)d'[j]\right\} \tag{6.4}$$

that can be rewritten in the time domain

$$\begin{aligned} i_{error} = \frac{1}{L}\int_0^t \left(qv_{dig} - V_\beta\right)d'dt = \frac{\left(qv_{dig} - V_\beta\right)V_g\sqrt{2}}{V_o L}\int_0^t sin\left(\omega t\right)dt = \\ = \frac{\left(qv_{dig} - V_\beta\right)M_g f_{sw}}{\pi K R f_u}\left(1 - cos\left(\omega t\right)\right) = \xi\left(qv_{dig} - V_\beta\right)\left[1 - cos\left(\omega t\right)\right] \end{aligned} \tag{6.5}$$

where $M_g = V_{g,peak}/V_o$ and $K = 2Lf_{sw}/R$, and then ξ represents a constant value under a defined operation conditions, being

$$\xi = \frac{M_g f_{sw}}{\pi K R f_u} \tag{6.6}$$

The derivation of the small-signal model is based on the loss-free resistor (LFR) concept [63], that is represented in Fig. 6.2 for the sensorless PFC controller with rebuilt input current, and is obtained by switching-period averaging, with the switching harmonics removed, so only line frequency (50, 60 or 400 Hz) and DC components are considered. It represents the behavior of the sensorless PFC controller with the feedback loop to compensate the current estimation error, in a straightforward manner.

Assuming that the converter 100 % conversion efficiency, and working in steady-state, the instantaneous power "dissipated" by R_e must appear at the converter output port. In this analysis, it must be addressed that although i_{reb} is the variable used to control i_g, the power delivered to the output port is given by the value of the real input current i_g. Therefore, from the large signal model, the RMS value of the real current I_g, is given by:

$$I_g = \frac{V_o^2}{R V_g} \tag{6.7}$$

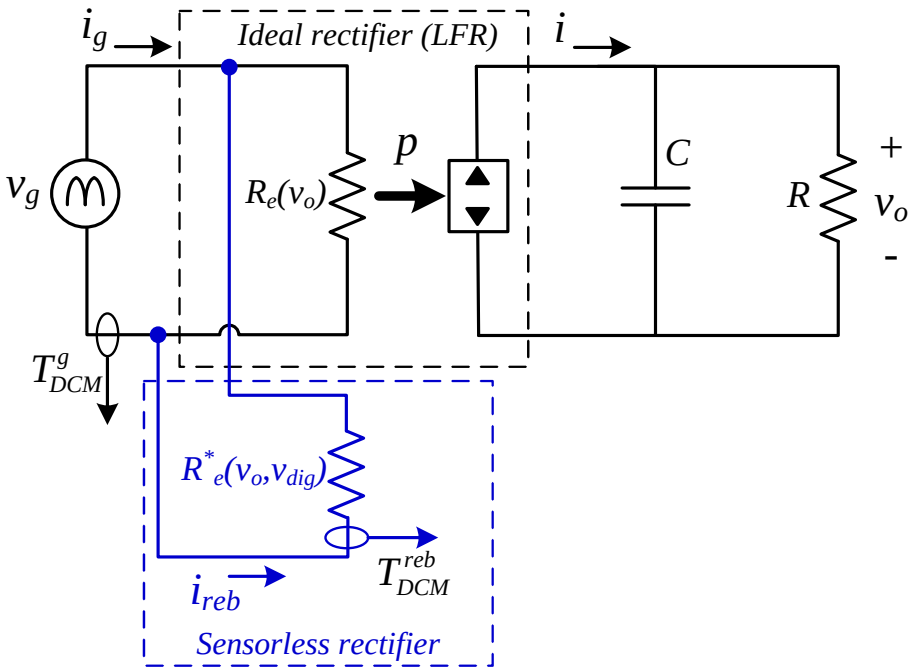


Figure 6.2: Low frequency equivalent circuit of the sensorless PFC controller.

The instantaneous rebuilt input current i_{reb}, has a sinusoidal waveshape (it is controlled by the PFC controller), so can be defined as:

$$i_{reb} = I_{reb}\sqrt{2}sin\,(\omega t) \tag{6.8}$$

Hence, (6.5) can be rewritten as:

$$i_g = I_{reb}\sqrt{2}sin\,(\omega t) + \xi\,(qv_{dig} - V_\beta)\,[1 - cos\,(\omega t)] \tag{6.9}$$

Among all the variables of (6.9), ξ and V_β are constant for a defined operation point, and v_{dig} is the control variable of the DCM time feedback loop. The RMS value of the input current I_g is defined by the outer voltage loop. To approximate the value of I_{reb} as a linear function of $\xi\,(qv_{dig} - V_\beta)$ and I_g, like is presented in (6.10), the Curve Fitting toolbox of MATLAB is used in this case:

$$I_{reb} = \gamma I_g - \alpha\xi\,(qv_{dig} - V_\beta) \tag{6.10}$$

for a given I_g, being α and γ the linear coefficients. This analysis is detailed in Appendix (A), obtaining as result $\gamma = 1$ and $\alpha = 0.9$, obtaining:

$$I_{reb} = I_g - 0.9\xi\,(qv_{dig} - V_\beta) \tag{6.11}$$

According to that, the digital emulated resistance $R^*_e$is defined as:

$$R^*_e = \frac{V_g}{I_{reb}} = \frac{V_g}{I_g - 0.9\xi\,(qv_{dig} - V_\beta)} = \frac{1}{\frac{2}{M_g^2 R} - \frac{0.9}{V_g}\xi\,(qv_{dig} - V_\beta)} \tag{6.12}$$

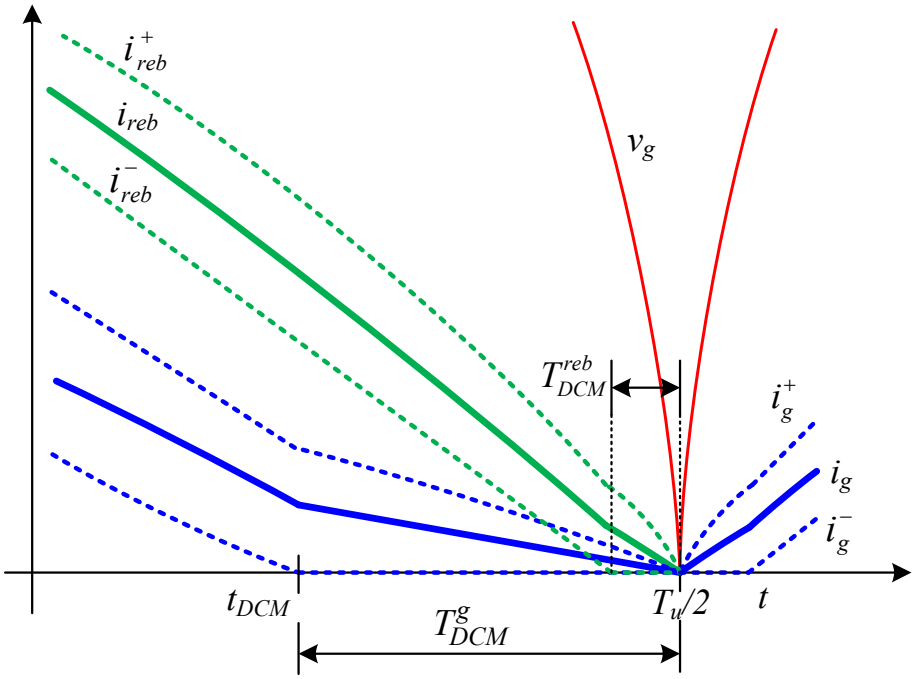


Figure 6.3: Waveforms around the AC line zero-crossings.

The rebuilt current operates in the DCM if

$$\frac{v_g}{V_o} < 1 - \frac{KR}{R_e^*} \tag{6.13}$$

as in presented in [15] for the NLC controller. For any load between these boundary values, the boost converter goes from operating in the DCM to the CCM and back to the DCM during half line cycle.

Figure 6.3 shows the typical waveforms for the PFC Boost sensorless controller when $i_{error} \neq 0$, in this case $i_{error} < 0$. The rectified input voltage v_g, is represented in red, achieves zero at the half line cycle $t = \frac{T_u}{2}$. The average, peak and valley values are represented by i_g, i_g^+ and i_g^-, respectively. In green, the same values for the rebuilt input current i_{reb}, are plotted. The DCM time in i_{reb} occurs due to the duty cycle saturation (for example, it is selected $D_{max} = 0.95$).

The ripple in the rebuilt current Δi_{reb}, is defined by (6.14). The DCM appears, at nominal power, around to the half-line zero crossings, where d is saturated, $d = D_{max}$, so Δi_{reb} can be approximated according to (6.15). Current estimation error causes a DCM time modification in i_g around this point.

$$\Delta i_{reb} = \frac{v_g d}{2 f_{sw} L} \tag{6.14}$$

$$\Delta i_{reb} \approx \Delta i_{reb}|_{d=D_{max}} = \frac{v_g D_{max}}{2 f_{sw} L} \tag{6.15}$$

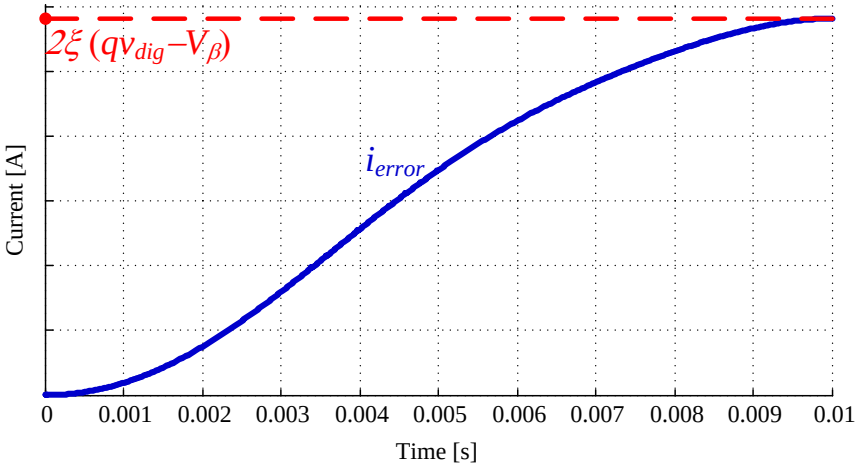


Figure 6.4: Current error waveform i_{error}, and its linear approximation.

From (6.11), the instantaneous value of the rebuilt current i_{reb}, is given by:

$$i_{reb} = \left[\frac{V_o^2}{RV_g} - 0.9\xi\left(qv_{dig} - V_\beta\right)\right]\sqrt{2}sin\left(\omega t\right) \tag{6.16}$$

According to this, the valley value of the rebuilt current is given by $i_{reb}^- = i_{reb} - \Delta i_{reb}$, and with (6.16) and (6.15) it can be rewritten as:

$$i_{reb}^- = \left[\frac{V_o^2}{RV_g} - 0.9\xi\left(qv_{dig} - V_\beta\right) - \frac{V_g D_{max}}{2f_{sw}L}\right]\sqrt{2}sin\left(\omega t\right) \tag{6.17}$$

Rewriting (6.2) for the case of the valley values of the real input current $i_g^- = i_{reb}^- + i_{error}$:

$$i_g^- = \left[\frac{V_o^2}{RV_g} - 0.9\xi\left(qv_{dig} - V_\beta\right) - \frac{V_g D_{max}}{2f_{sw}L}\right]\sqrt{2}sin\left(\omega t\right) + \xi\left(qv_{dig} - V_\beta\right)\left[1 - cos\left(\omega t\right)\right] \tag{6.18}$$

The DCM condition starts at $t = t_{DCM}$, when $i_g^- = 0$. Hence, according to this:

$$\left[\frac{V_o^2}{RV_g} - 0.9\xi\left(qv_{dig} - V_\beta\right) - \frac{V_g D_{max}}{2f_{sw}L}\right]\sqrt{2}sin\left(\omega t_{DCM}\right) + \xi\left(qv_{dig} - V_\beta\right)\left[1 - cos\left(\omega t_{DCM}\right)\right] = 0 \tag{6.19}$$

To obtain t_{DCM}, it is necessary to linearize (6.19). Around the operating point, the DCM occurs near to the half line zero crossings, so the time in which the real current is operating in the DCM T_{DCM}^g, is small. Therefore, the function $sin\left(\omega\left(\frac{T_u}{2} - t\right)\right)$ can be approximated to ωT_{DCM}^g. According to that, i_{reb}^- can be rewritten as:

$$i_{reb}^- \approx \left[\frac{V_o^2}{RV_g} - 0.9\xi\left(qv_{dig} - V_\beta\right) - \frac{V_g D_{max}}{2f_{sw}L}\right]\sqrt{2}\omega T_{DCM}^g \tag{6.20}$$

On the other hand, the linear approximation of i_{error} at the end of the half line cycle $(T_u/2)$ is given by:

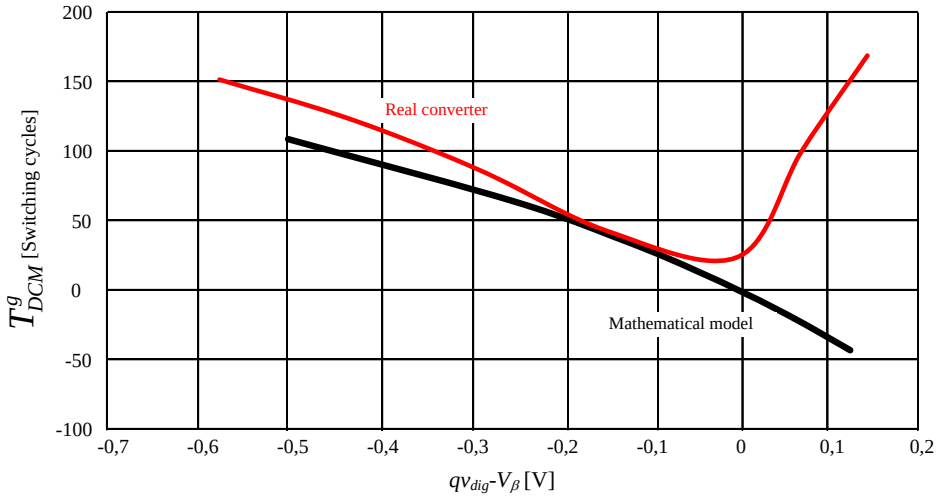


Figure 6.5: Operation time in DCM of the real input current T^g_{DCM}, in terms of switching periods, of the real converter and the mathematical model.

$$i_{error} \approx i_{error}\left(\frac{T_u}{2}\right) + \left.\frac{di_{error}}{dt}\right|_{t=\frac{T_u}{2}} \times \left(t - \frac{T_u}{2}\right) = 2\xi\left(qv_{dig} - V_\beta\right) \tag{6.21}$$

And shown in Fig. 6.4, so at the time $t = t_{DCM}$, the condition $i_g^- = i_{reb}^- + i_{error} = 0$, is used to define the dependency between v_{dig} and t_{DCM}:

$$\left[\frac{V_o^2}{RV_g} - 0.9\xi\left(qv_{dig} - V_\beta\right) - \frac{V_g D_{max}}{2f_{sw}L}\right]\sqrt{2}\omega T^g_{DCM} + 2\xi\left(qv_{dig} - V_\beta\right) = 0 \tag{6.22}$$

Working with (6.22), it is possible to obtain the value of T^g_{DCM} as a function of v_{dig}, given by (6.23):

$$T^g_{DCM} = \frac{qv_{dig} - V_\beta}{0.9\sqrt{2}\pi f_u\left(qv_{dig} - V_\beta\right) - \Gamma} \tag{6.23}$$

where Γ is a constant factor defined by:

$$\Gamma = \frac{V_o \pi^2 f_u^2 L}{R}\left(\frac{2}{M_g^2} - \frac{D_{max}}{K}\right) \tag{6.24}$$

The DCM operation time of the real input current T^g_{DCM}, is plotted in black in Fig. 6.5 in terms of switching periods (with a switching frequency of $f_{sw} = 72$ kHz) for different values of v_{dig}. It is compared with the experimental results obtained in the converter, which are plotted in red. To obtain the mathematical model, the DCM time that occurs due to the duty cycle saturation around the line zero crossings has not been considered, so $T^g_{DCM}\left(v_{dig} = V_\beta/q\right) = 0$.

6.2 Small-signal AC model. Low bandwidth loop.

The small-signal AC model, is obtained assuming that the power rectifier is working at the operating point with the current estimation error totally compensated, and the output voltage

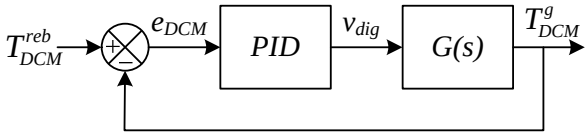


Figure 6.6: Block diagram system representation.

constant $V_o = V_{ref}$ (due to the action of the output voltage loop).

The output voltage loop in a PFC controller has a typical bandwidth around $f_c = 5 - 10\,Hz$ to set the output voltage v_o according to the reference. To not interfere with this, the DCM time compensation loop has a lower bandwidth, using a sample period equal to $T_s = 1/f_c$.

The input perturbation, which causes a variation in T^g_{DCM} around the operating point, is imposed by v_{dig}.

The block diagram of the system with the feedback loop is presented in Fig. 6.6, being $G(s)$ the small signal transfer function that represents the plant and given by:

$$G(s) = \frac{T^g_{DCM}(s)}{v_{dig}(s)} \tag{6.25}$$

obtained by the linearization (6.23) around the operating point:

$$T^g_{DCM}(s) = \left.\frac{\partial T^g_{DCM}}{\partial v_{dig}}\right|_{v_{dig}=V_\beta/q} v_{dig}(s) \tag{6.26}$$

where

$$\frac{\partial T^g_{DCM}}{\partial v_{dig}} = \frac{-q\Gamma}{\left[0.9\sqrt{2}\pi f_u \left(q v_{dig} - V_\beta\right) - \Gamma\right]^2} \tag{6.27}$$

Substituting (6.27) in (6.26), the compensation signal v_{dig} is given by:

$$\frac{T^g_{DCM}(s)}{v_{dig}(s)} = -\frac{q}{\Gamma} \tag{6.28}$$

In consistency with the assumptions previously enumerated, no dynamics appear in this transfer function, but a digital controller, introduces a sample period delay, so the transfer function in the z-domain, with a sample period $T_s = 1/f_c$ is:

$$\frac{T^g_{DCM}(z)}{v_{dig}(z)} = -\frac{q}{\Gamma} z^{-1} \tag{6.29}$$

From (6.29), the transfer function is translated into the Laplace domain considering the Forward Euler relationship $z = T_s s + 1$. Hence, (6.28) is rewritten as:

$$\frac{T^g_{DCM}(s)}{v_{dig}(s)} = \frac{-q/\Gamma}{T_s s + 1} \tag{6.30}$$

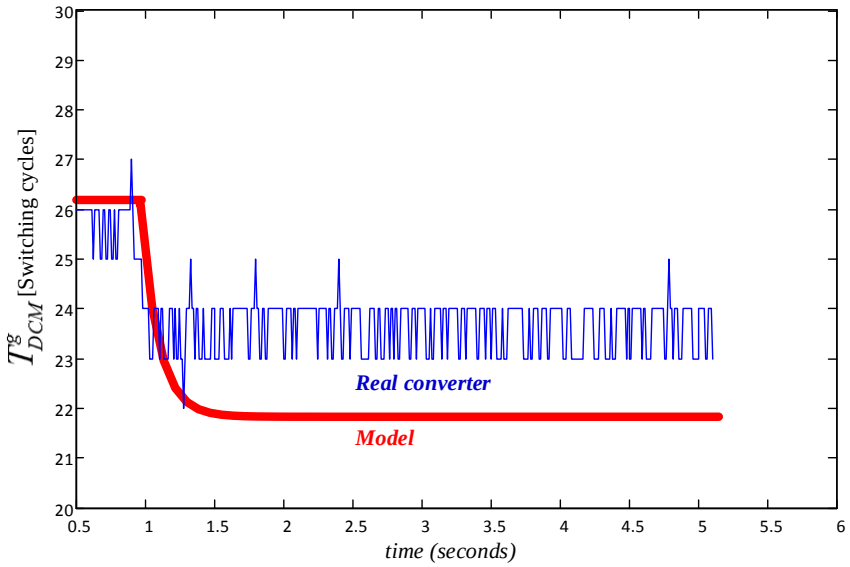


Figure 6.7: Actual vs theoretical response time of the plant under a 2-bit v_{dig} step-up. $V_g = 230\,V_{rms}$, $V_o = 400\,V$, $f_{sw} = 96\,kHz$ P_g =460.9 W with $q = 435/\left(2^{14}-1\right)$ V/bit.

Using a PI compensator defined as:

$$PI(z) = \frac{K_{PI}}{z-1} \tag{6.31}$$

the Jury stability criterion defines the range of values of K_{PI} for a stable system as:

$$0 > K_{PI} > \frac{-\Gamma}{q} \tag{6.32}$$

A comparison of the actual and the theoretical step responses, under a 2-bits v_{dig} step-up input is shown in Fig. 6.7 with a LSB resolution in v_{dig} of $q = 435/\left(2^{14}-1\right)$. The response of the model defined by (6.30), with $f_c = 1/T_s = 3$ Hz, is plotted in red. The actual response of the plant, $G(s)$, is represented in blue.

6.3 Chapter conclusion

A model of the plant that enables the correction of the input current distortion due to estimation errors has been presented. The steady state model of the plant defines the value of the DCM time of the real input current T^g_{DCM}, as a function of v_{dig}, that is represented in this case by a constant due to the low frequency nature of the current estimation error controller and the low bandwidth of the control loop designed to cancel the current estimation errors. The dynamic behavior of the plant, is dominated by the inherent delay of the digital sampler, and the value of the PI compensator gain is limited using the Jury stability criterion. The loop model is compared with the values measured in the real system, showing a good agreement around the operating point.

Chapter 7

Low THDi controller for Single Phase Rectifiers

7.1 Introduction to distorted grids

The International Standards, like EN-61000-3-2 [1], defines the limits of the current harmonics that must be complied by every load connected to the grid. These limits are different depending on the load type (Class A, B, C or D for the EN-61000-3-2 Std) and impose absolute or relative limits on particular harmonics. The IEEE Std 519 [22] sets limits on particular harmonics as well as on the THD of the current (specified in Section 2.2), but the most of the limits are given as a percentage of the fundamental component.

Other agencies have defined additional and very tight harmonic restrictions for critical applications. For example, for military and commercial aircraft electronics, it is typically required to have all the harmonics magnitudes lower than 3 % of the fundamental and a total THDi $\leq$ 5 % [23, 156]. Table 7.1 summarizes the harmonic current limits specified in DO-160D Std for airborne applications [24].

Harmonic Orders	Single Phase
Odd Triplen (h=3, 9,..., 39)	$I_h = 0.15I_1/h$
h=5, 7, 11, 13	$I_h = 0.3I_1/h$
h= 17, 19	
h= 23, 25	
Other Odd Non-Triplen (h=29, 31,..., 37)	
h=2, 4	$I_h = 0.01I_1/h$
Other Even (h=6,..., 40)	$I_h = 0.025I_1/h$

Table 7.1: DO-160 Harmonic Current Limits

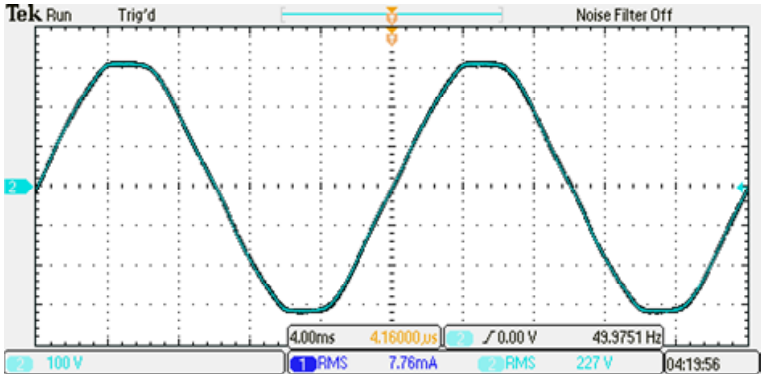


Figure 7.1: Grid voltage in the Power Electronics Laboratory, on March 13th of 2013.

The aim of the traditional PFC controllers is to obtain a resistance behavior:

$$\langle i_g \rangle = \frac{v_g}{R_e} \tag{7.1}$$

According to this, the input impedance is constant for all the frequencies. For an ideal utility voltage $v_g = \sqrt{2} V_g sin\,(\omega t)$, the resistance behavior leads to a sinusoidal input current, and theoretically, the harmonic distortion is due to the switching ripple of the current (very high frequency component).

All the limits defined by the International Standards are given supposing an ideal sinusoidal input voltage. Undesired harmonics affecting the performance of the grid may arise when the line voltage is not totally sinusoidal, even with an harmonic distortion that meet the limits defined by the Standards of $THDv \leq 5$ %. In a resistor emulator mode, the input current waveform is a replica of the input voltage, so the minimum current harmonic distortion will be, in the best case, equal to the $THDv$. Considering the current ripple and the non-idealities in the real implementation of the controller, $THDi \geq THDv$ for every PFC rectifier controller by the typical controllers.

When the specifications of a design are given only in terms of current harmonics (for example, $THDi < 3\%$) like in airborne applications [23, 156], if the line voltage is not sinusoidal, the harmonic requirements would be almost impossible of being complied with traditional PFC rectifiers that uses the input voltage as current shape reference. In order to try to improve this behavior an extra capability in the digital PFC controller is presented in this Chapter, where the line current can be pure sinusoidal, independently on the input voltage waveshape. Works like [134, 157] present controller with the same goal of sinusoidal current. In these cases, both use in the current loop a sine wave generated in the digital device as current reference.

Figure 7.1 shows the real phase voltage on the Power Electronics Lab of the University of Cantabria, in Santander. The harmonic content data are presented in Table 7.2. It can be seen how the waveform is not totally sinusoidal, with an harmonic distortion of 3.89 %. The trapezoidal waveshape, as in the figure, is typical in the utility voltage.

V_{rms}	$THDv$	$V_{1,rms}$	$V_{3,rms}$	$V_{5,rms}$	$V_{7,rms}$	$V_{9,rms}$	$V_{11,rms}$
227.60	3.89 %	227.15	3.86	7.58	2.44	0.94	0.23

Table 7.2: Voltage harmonics in the line voltage shown in Fig. 7.1.

7.2 Definitions of Electric Power Quantities

The IEEE Std 1459 [158] defines the electric power to quantify the flow of electrical energy in single-phase and three-phase circuits under sinusoidal, non-sinusoidal, balanced and unbalanced conditions. Considering an non-sinusoidal (distorted) voltage v_g, or current i_g, in a single-phase system, they can be written as:

$$v_g = v_{g1} + v_{gH} \tag{7.2}$$

$$i_g = i_{g1} + i_{gH} \tag{7.3}$$

where v_{g1} and i_{g1} are the fundamental components defined by (7.4) and (7.5), respectively. And the harmonic content of the voltage v_{gH}, and the current i_{gH}, defined by (7.6) and (7.7). h represents the harmonic component number, α_h the phase of the h^{th} harmonic voltage component and β_h the phase of the h^{th} harmonic current.

$$v_{g1} = \sqrt{2} V_{g1} sin\left(\omega t\right) \tag{7.4}$$

$$i_{g1} = \sqrt{2} I_{g1} sin\left(\omega t - \beta_1\right) \tag{7.5}$$

$$v_{gH} = V_{g0} + \sqrt{2} \sum_{h \neq 1} V_{gh} sin\left(h\omega t - \alpha_h\right) \tag{7.6}$$

$$i_{gH} = I_{g0} + \sqrt{2} \sum_{h \neq 1} I_{gh} sin\left(h\omega t - \beta_h\right) \tag{7.7}$$

The RMS values squared of the input current and voltage are as follows:

$$V_g^2 = V_{g1}^2 + V_{gH}^2 \tag{7.8}$$

$$I_g^2 = I_{g1}^2 + I_{gH}^2 \tag{7.9}$$

being V_{g1} and I_{g1} the RMS values of the both fundamental components, and V_{gH} and I_{gH} the square of the RMS values of v_{gH} and i_{gH}, which are defined as:

$$I_{gH} = \sqrt{I_g^2 - I_{g1}^2} \tag{7.10}$$

and

$$V_{gH} = \sqrt{V_g^2 - V_{g1}^2}, \tag{7.11}$$

respectively. With these terms, the total harmonic distortion (THD) of the current and voltage are expressed as:

$$THDv = \frac{V_{gH}}{V_{g1}} = \sqrt{\left(\frac{V_g}{V_{g1}}\right)^2 - 1} \tag{7.12}$$

$$THDi = \frac{I_{gH}}{I_{g1}} = \sqrt{\left(\frac{I_g}{I_{g1}}\right)^2 - 1} \tag{7.13}$$

The total active power (P_g) generated by all the components involved can be divided in two terms $P_g = P_{g1} + P_{gH}$, where P_{g1} represents the fundamental active power, and P_{gH} the harmonic active power (or non-fundamental active power). Both terms are written as:

$$P_{g1} = V_{g1} I_{g1} cos\left(\beta_1\right) \tag{7.14}$$

$$P_{gH} = V_{g0} I_{g0} + \sum_{h \neq 1} V_{gh} I_{gh} cos\left(\beta_h - \alpha_h\right) = P_g - P_{g1} \tag{7.15}$$

The total apparent power ($S_g = V_g I_g$) represents the amount of total power that can be supplied to a load under ideal conditions (sinusoidal voltage and current). In the same manner, the fundamental apparent power is "generated" only by the fundamental components $S_{g1} = V_{g1} I_{g1}$. The IEEE Std 1459 defines the fundamental power factor (PF_1) and the power factor (PF) as function of the variables presented before as:

$$PF_1 = \frac{P_{g1}}{S_{g1}} = cos\beta_1 \tag{7.16}$$

$$PF = \frac{P_g}{S_g} = PF_1 \frac{1 + {}^{P_{gH}}/_{P_{g1}}}{\sqrt{1 + THDi^2 + THDv^2 + \left(THDi \cdot THDv\right)^2}} \tag{7.17}$$

The approach presented in this Chapter is a digital controller for front-end Boost converters working in the CCM, in which the input current can be pure sinusoidal (Case A), or can be proportional to the input voltage and work as a traditional PFC stage (Case B). The user decide among the two possibilities.

A study of the value of PF as function of the $THDv$ for the two cases is done as follows:

- Case A: The current is sinusoidal: $THDi = 0\%$, consequently no harmonic active power flows through the system: $P_{gH} = 0\,W$. Fundamental components of the current and the voltage are in phase, $cos\beta_1 = 1$. According to that, the PF value is rewritten as:

$$PF = \frac{1}{\sqrt{1 + THDv^2}} \tag{7.18}$$

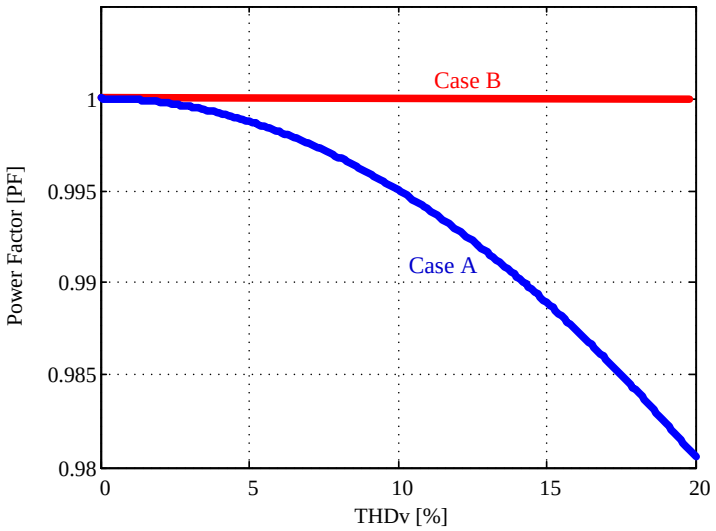


Figure 7.2: Value of the power factor as function of the voltage harmonic distortion for Case A and Case B.

- Case B: The current is proportional to the input voltage (traditional behavior as a resistor with a value R_e): $THDi = THDv$, and due to that, the harmonic active power flows through the system: $P_{gH} = {}^{V_{gH}^2}/_{R_e}$. The fundamental components of the current and the voltage are in phase, $cos\beta_1 = 1$. According to that, the PF value can be rewritten as:

$$PF = \frac{1 + THDv^2}{\sqrt{1 + 2 \cdot THDv^2 + THDv^4}} = 1 \tag{7.19}$$

Figure 7.2 shows the value of PF as a function of the $THDv$. In both cases, the value of the fundamental power factor $PF_1 = 1$, but it can be seen how the PF value decreases with the harmonic distortion if the current taken from the grid is sinusoidal . From the user point of view, the case preferred is the resistance behavior (Case B, as a traditional PFC controller), because the power factor is the higher. The behavior with a totally sinusoidal current (Case A) is preferred only if the specifications are given in terms of current harmonics, because ideally, it is possible to obtain a pure sinusoidal waveform without dependence on the voltage source. From the point of view of the utility grid, Case A is preferred because the load performs some active filter action avoiding the propagation of the harmonics presented in the utility voltage.

7.3 Low THDi controller under distorted voltages

The goal of the new approach presented in this Chapter, is to implement an extra capability in the controller in which the low-frequency portion of the input current is pure sinusoidal, according to:

$$\langle i_g \rangle = \frac{P_g}{V_g} \sqrt{2} sin\left(\omega t\right) \tag{7.20}$$

This controller based on the NLC controller presented in [15] to obtain an input current proportional to the AC voltage. Defining the distorted AC line voltage as $v_g = v_{g1} + v_{gH}$, with the fundamental component $v_{g1} = \sqrt{2}V_{g1}sin(\omega t)$, exp. (7.20) can be rewritten as a function of v_{g1}:

$$\langle i_g \rangle = \frac{v_{g1}}{R_{fict}} \tag{7.21}$$

where R_{fict} is a fictitious resistor that represents the proportionality between the input current i_g and the fundamental component of the voltage v_{g1}. Substituting (7.2) in (7.21), it is obtained:

$$\langle i_g \rangle = \frac{v_g - v_{gH}}{R_{fict}} \tag{7.22}$$

Considering the converter operating in the CCM, the ideal quasisteady-state conversion characteristic is given by:

$$v_g = V_o(1-d) \tag{7.23}$$

and v_g can be eliminated from exp. (7.22), obtaining

$$\langle i_g \rangle = \frac{V_o(1-d)}{R_{fict}} - \frac{v_{gH}}{R_{fict}} \tag{7.24}$$

The output voltage is considered a DC constant value at the specified reference level $V_o = V_{ref}$. The first term $\frac{V_o(1-d)}{R_{fict}}$, is similar to the NLC control law shown in [15] or as LPCM control in [146], that is a modification of the NLC controller presented before and corresponds with the expression that describes a PWM block. According to (7.24), the duty cycle command can be obtained by comparing a sample the average value of the current i_g, with a triangular carrier signal v_m, defined as:

$$v_m = V_m\left(1 - \frac{t}{T_{sw}}\right) - r_s\frac{v_{gH}}{R_{fict}}, \quad 0 \le t \le T_{sw} \tag{7.25}$$

where $V_m = r_s V_o / R_{sfict}$, being r_s the value of the current sensor used to sample the input current. Figure 7.3 shows the control waveforms over a half line cycle, for an input voltage with a $THDv = 6$ % with $v_{g3} = 0.05V_{g1}\sqrt{2}sin(3\omega t)$, $v_{g5} = 0.03V_{g1}\sqrt{2}sin(5\omega t + \pi)$ and $v_{g7} = 0.01V_{g1}\sqrt{2}sin(7\omega t)$. For clarification purposes, T_{sw} has been depicted much longer than the actual implemented switching period. The carrier signal has a frequency equal to the switching frequency $f_{sw} = 1/T_{sw}$, and the second term, $\frac{v_{gH}}{R_{fict}}$, offsets the carrier signal in each switching period. Considering the utility period, the second term means a low frequency harmonic content in the carrier signal.

The value of R_{fict} changes with the load and is given by the outer voltage loop in terms of V_m [15]. A block diagram of the boost rectifier with the low THDi controller is shown in Fig. 7.4. In grey, the part of the controller that is completely digital is highlighted. In this case, the current used in the controller is the rebuilt current i_{reb}, but this approach can be used too for the sensed input current i_g, without any modification in the control law (r_s is not used in the current estimation case, where i_{reb} and v_m signal are both digital). The input

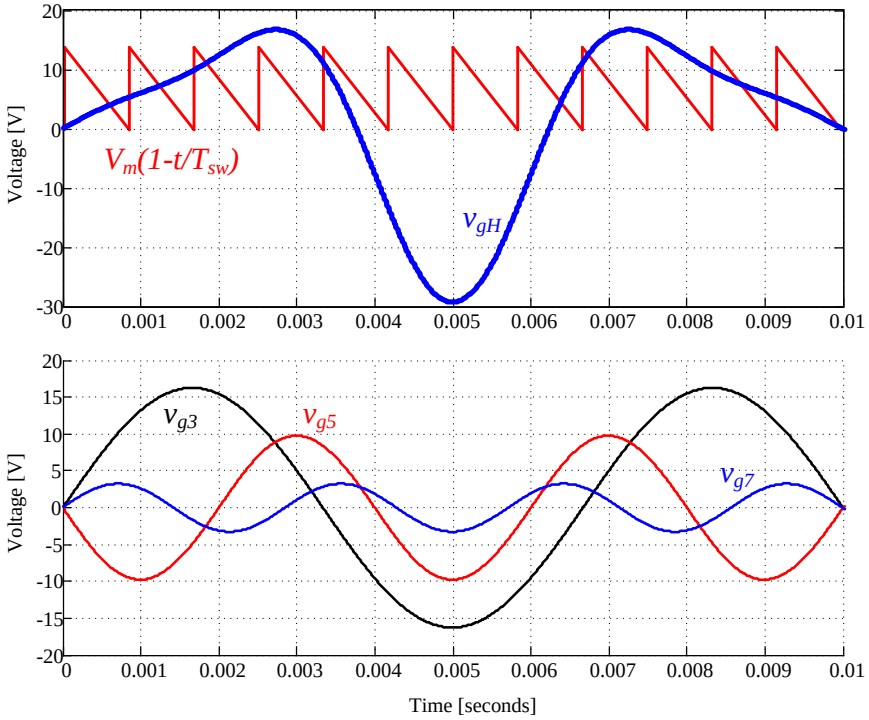


Figure 7.3: Top: First term of the carrier signal (red) and the harmonic voltage (blue) waveforms. Bottom: Voltage harmonics in an example of input voltage with $THDv = 6\,\%$.

voltage v_g, is digitized by the input voltage ADC, and with a digital zero crossing detector (ZCD) and sinusoidal pattern ins synchronized with the utility line voltage. A peak detector for the input voltage is used to approximate the value of v_{g1} as: $v_{g1} \approx V_{g,peak} sin\,(\omega t)$. Hence, (7.21) can be rewritten as:

$$\langle i_g \rangle = \frac{V_{g,peak}}{R_{fict}} sin\,(\omega t) \tag{7.26}$$

In the case that $v_{g1} \neq V_{g,peak} sin\,(\omega t)$, in the initial transient state i_g is totally sinusoidal according to (7.26), but with a RMS value different to reference the demanded by the load. The outer voltage loop modifies then V_m and R_{fict} to adjust the input RMS current I_g.

With this, it is possible to obtain an indirect measurement of the harmonic voltage $v_{gH} = v_g - V_{g,peak} sin\,(\omega t)$. Using as digital device a microcontroller or an FPGA, the Fast Fourier Transforms (FFT) is a good choice to obtain the harmonic content of a variable, with dedicated blocks to compute this, like [159,160], but it needs an important quantity of resources. In this case, the particular value of each voltage harmonic is not needed, so only the total harmonic voltage v_{gH}, is enough. Therefore, FFT blocks can be avoided, simplifying the design of the digital controller.

Note that with the proposed controller, the load viewed by the grid R_e, is now a function of the input voltage phase, $R_e = R_e\,(\omega t)$. In steady state, and for a defined input power P_g, the

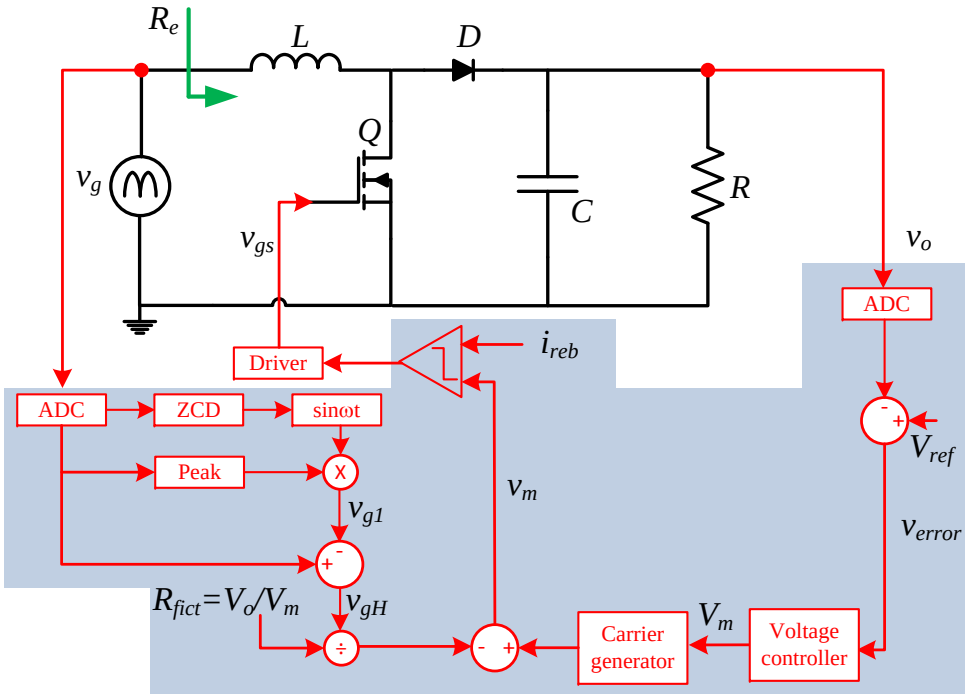


Figure 7.4: Block diagram of the low THDi controller with the boost converter.

input current can be rewritten as:

$$\langle i_g \rangle = \frac{P_g}{V_g}\sqrt{2}sin\,(\omega t) \tag{7.27}$$

that compared with (7.26) yields an expression for R_{fict}:

$$R_{fict} = \frac{V_{g,peak}V_g}{P_g\sqrt{2}} \tag{7.28}$$

From (7.1) and (7.21), it is possible to obtain the expression for the input impedance R_e:

$$R_e\,(\omega t) = R_{fict}\frac{v_{g1}}{v_g} = R_{fict}V_{g,peak}\frac{sin\,(\omega t)}{v_g} \tag{7.29}$$

Equation (7.23) in only valid if the converter operates in the CCM. So around the AC line zero crossings, where the converter operates in the DCM, a little distortion in the input current occurs. It is presented in detail in [15] and in Section (3.2) of this document for the traditional NLC controller, and affects in the same way in this low THDi controller. NLC control is presented in [64] for rectifiers based on buck-boost, Ćuk or SEPIC topologies, and in the same way as presented here, the low THDi controller can be extrapolated to them. If the bandwidth of the linear input current loop keeps constant but the line frequency increases, the typical distortion around the line zero-crossing could make impossible to meet the harmonic limits. This issue is addressed in [161,162]. Nonlinear controllers can deal with this problem, offering responses cycle-by-cycle [18,148,163].

7.4 Chapter conclusion

In this Chapter, a modification in the NLC controller has been presented, in order to demand a sinusoidal input current despite input voltage distortion. Therefore, no currents harmonics are injected to the grid, no contributing in the propagation of the voltage distortion. The input voltage measurement is compared with a digital sinusoidal pattern to compute the harmonics in the input voltage, and modify the amplitude of the carrier signal used in the NLC control law.

No additional analog components are needed in comparison with the traditional control, because the modification is completely digital. The user selects the desired behavior (resistance behavior or pure sinusoidal current).

Chapter 8

Experimental validation

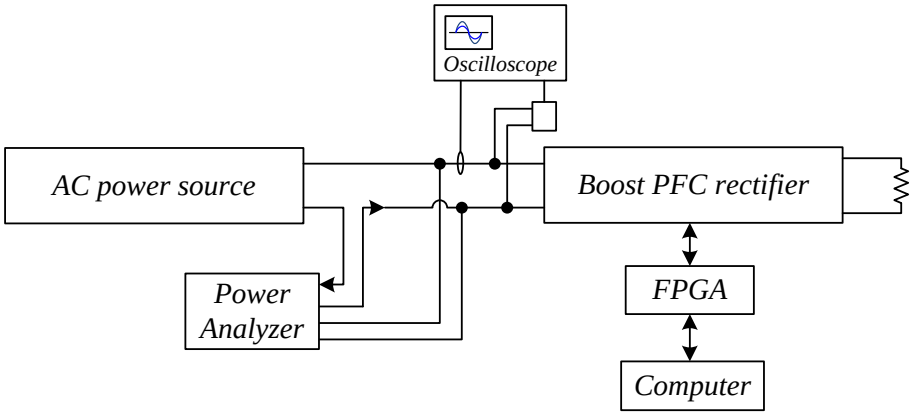
The previous Chapters have presented the theoretical approach and simulations of the digital Sensorless controller for Boost PFC rectifiers based on the current estimation concept. In this Chapter, an experimental validation is presented. A scheme and a picture of the laboratory set-up are presented in Fig. 8.1a and 8.1b, respectively. An AC power source supplies the Boost PFC rectifier to emulate the electrical grid under different conditions, a power analyzer samples the input voltage and current RMS values with a 1-second sample period, and an oscilloscope is used to capture different signals of the system. The boost converter is controlled with a Spartan 3 FPGA used as digital device. A resistor array is used as load.

The aim of all the results presented in this Chapter is to show the behavior of the digital controller under several conditions, illustrating its "universality".

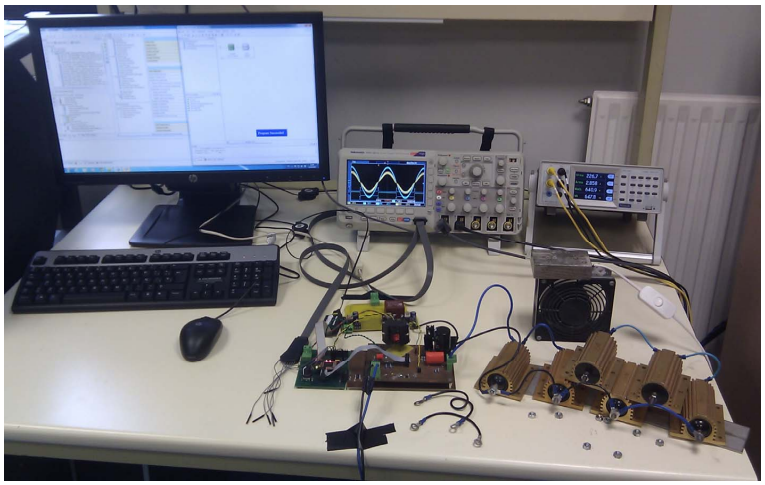
8.1 Boost converter prototype

A 1 kW Boost PFC rectifier is built to verify the Sensorless PFC controller presented in this Thesis, based on the input current rebuilding concept. The circuit scheme corresponding to the experimental prototype is shown in Fig. 8.2a, in which the control circuitry is represented in blue and green. The values of all the parameters and components of the laboratory prototype are listed in Table 8.1.

The part of the control circuit drawn in green does not represent any novelty in comparison with other types of digital controllers presented in PFC rectifiers; and corresponds with the input and output voltage sampling circuit, with the ADCs, and the circuit that adapts the $on - off$ signal generated in the digital device to drive the MOSFET. Two voltage dividers (R_{g1} and R_{g2} for the input voltage, and R_{o1} and R_{o2} for the output voltage) set the voltage samples into the full scale range ($v_{max} = 5$ V) of the control circuit.



(a)

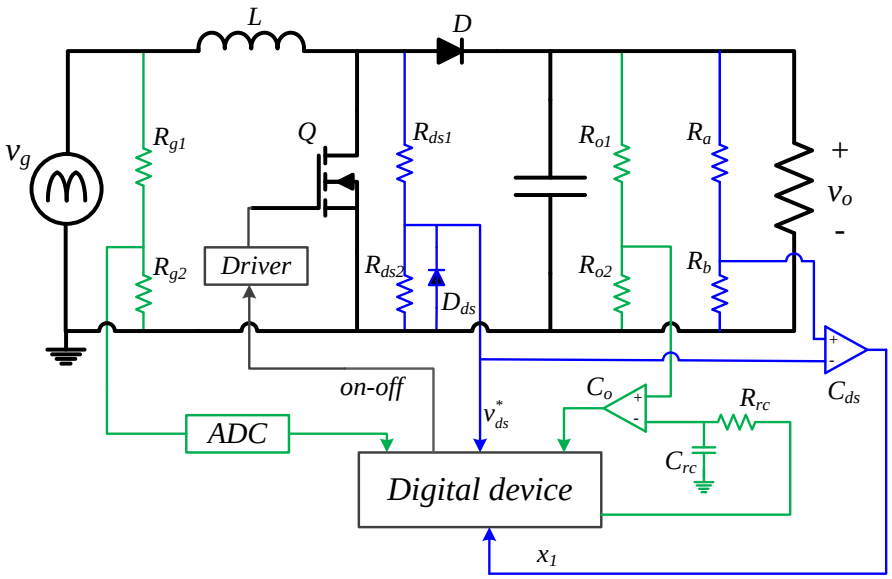


(b)

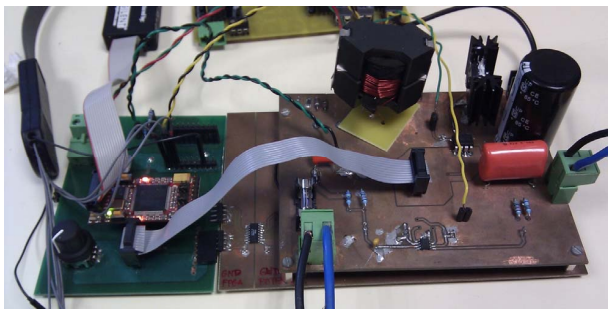
Figure 8.1: (a) Block diagram and (b) picture of the of the Laboratory Test bench

Element	Value/Component
Inductor (L)	L =1 mH, R_L =0.25 Ω
Power Diode (D)	IDH12S60, V_D =0.8 V, R_D =0.07 Ω
Output Capacitor (C)	C =220 μF, 450 V
Power MOSFET (Q)	IRFP27N60K, R_{on} =180 mΩ
Driver	HCPL 3120
Signal resistor $R_{g1} = R_{o1}$	1 MΩ ±0.1 %
Signal resistor $R_{g2} = R_{o2}$	10.7 kΩ ±0.1 %
Signal resistor $R_a = R_{ds1}$	1.2 MΩ ±1 %
Signal resistor $R_b = R_{ds2}$	9.31 kΩ ±1 %
Signal diodeD_{ds}	1N4148
Signal comparator C_o and C_{ds}	MAX942CPA
Signal resistor R_{rc}	2.2 kΩ ±5 %
Signal capacitor C_{rc}	3.3 nF ± 20 %
ADC	TLV1572, $Nbits = 10$, v_{max} =5 V

Table 8.1: Parameters of the components used in the Boost prototype.



(a)



(b)

Figure 8.2: (a) Circuit scheme of the proposed digital controller. (b) Picture of the boost converter prototype and the FPGA.

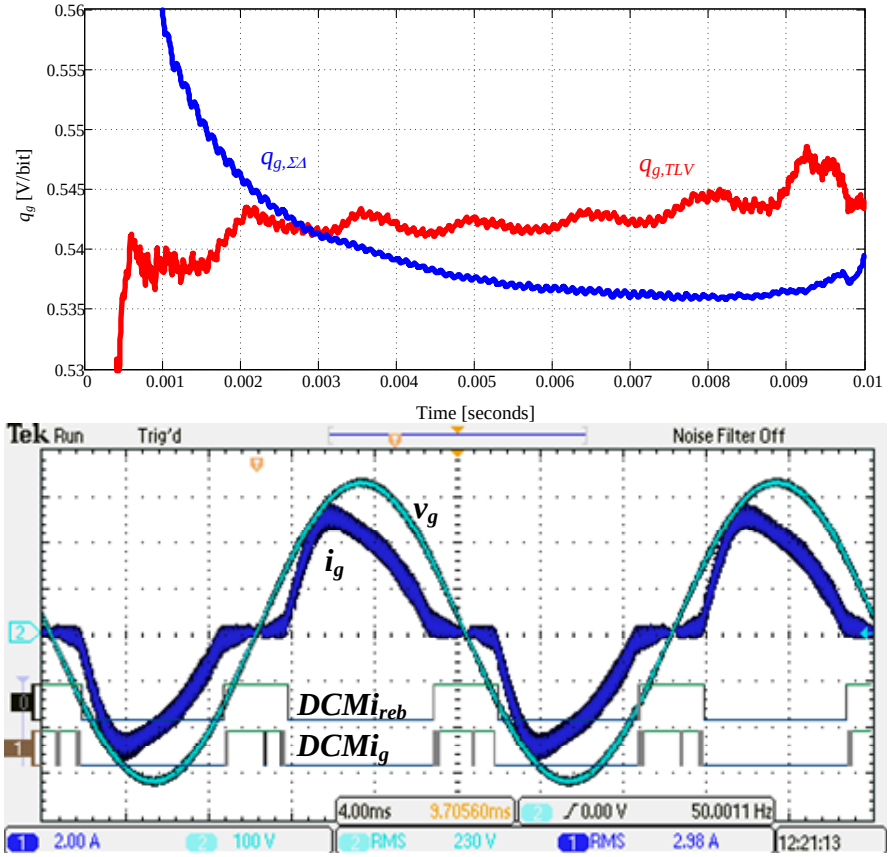


Figure 8.3: Top: Measured value of q_g over the half line cycle, for two different input voltages ADCs, under 230 V_{rms} (50 Hz). In red it is plotted the measured value using the TLV1572 commercial ADC. In blue is plotted the q_g value using the $\Sigma\triangle$ ADC used in the output voltage measurement, that leads to the i_g current waveform at 648 W. Bottom: Experimental waveforms when the $\Sigma\triangle$ ADC is used in the output, and also in the input voltage measurement.

With these values of the divider resistances, the maximum voltage in the converter that can be quantized, without saturation of the ADCs, is 473 V. As input voltage ADC, a commercial TLV1572 10-bits is used, with 1.25 MSPS. And an $ad-hoc$ sigma-delta, as the ADCs presented in Section 2.6 (Fig. 2.18) is used to measure the output voltage with the concepts presented in [10, 14, 122–124].

A commercial ADC is used to discretize the input voltage to avoid non-linearities (v_g is a rectified sinusoidal waveform with a zero minimum value and a peak value up to 325 V), trying to keep q_g constant over the half line cycle. Figure 8.3 shows the measured q_g over the half line cycle under the European line voltage (230 V_{rms} - 50 Hz) for the commercial ADC, labeled as $q_{g,TLV}$; and using a low-cost $\Sigma\triangle$ ADC similar to the ADC used in the output voltage, $q_{g,\Sigma\Delta}$. The higher variation of $q_{g,\Sigma\Delta}$ in comparison with $q_{g,TLV}$ makes this type of ADCs not valid for this sensorless controller to quantize v_g. In Fig. 8.3, the input current waveform at 648 W is also presented, with a power factor of PF =0.948 and $TDHi$ =29.35 % using the $\Sigma\triangle$ ADC in the input voltage.

On the other hand, the output voltage is quasi-constant over the half line cycle (with a small

ripple), so the $\Sigma\triangle$ ADC approach can be used, because its behavior is linear around the reference voltage.

The part of the control circuit highlighted in blue is a contribution of this work, and corresponds with the analog part that substitutes the current sensing circuit. R_{ds1}, R_{ds2} and D_{ds} adapts the MOSFET drain-to-source voltage to be an input of the digital device (v^*_{ds}). At the same time v^*_{ds} is compared by C_{ds} with the output voltage, adapted by R_a and R_b to obtain the digital signal x_1 used to detect the DCM in i_g.

The whole digital controller is described in VHDL and implemented on a XC3S200E FPGA of Xilinx. The input current and power are measured with a Power Analyzer Voltech PM1000+, and the captures presented in this Chapter are taken with MSO2014 mixed Signal Oscilloscope of Tektronix. The output voltage reference is 400 V_{dc}, with an input voltage ranging from 85 V_{rms}-60 Hz to 250 V_{rms}-50 Hz (universal input voltage range). Three different switching frequencies has been used to test the proposal (72 kHz, 96 kHz and 144 kHz), and the prototype is also tested under high frequency grids, typical of airborne applications (360 - 800 Hz).

8.2 Operation in Steady state

The experimental results obtained in steady state under different input voltages and power levels are presented in this section, with three different subsections depending on the switching frequency value. In all the captures, the input voltage (v_g) and current (i_g) are plotted along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Five different input voltage levels have been tested, three of them at 50 Hz (250, 230 and 180 V_{rms}), and two at 60 Hz (120 and 85 Vrms).

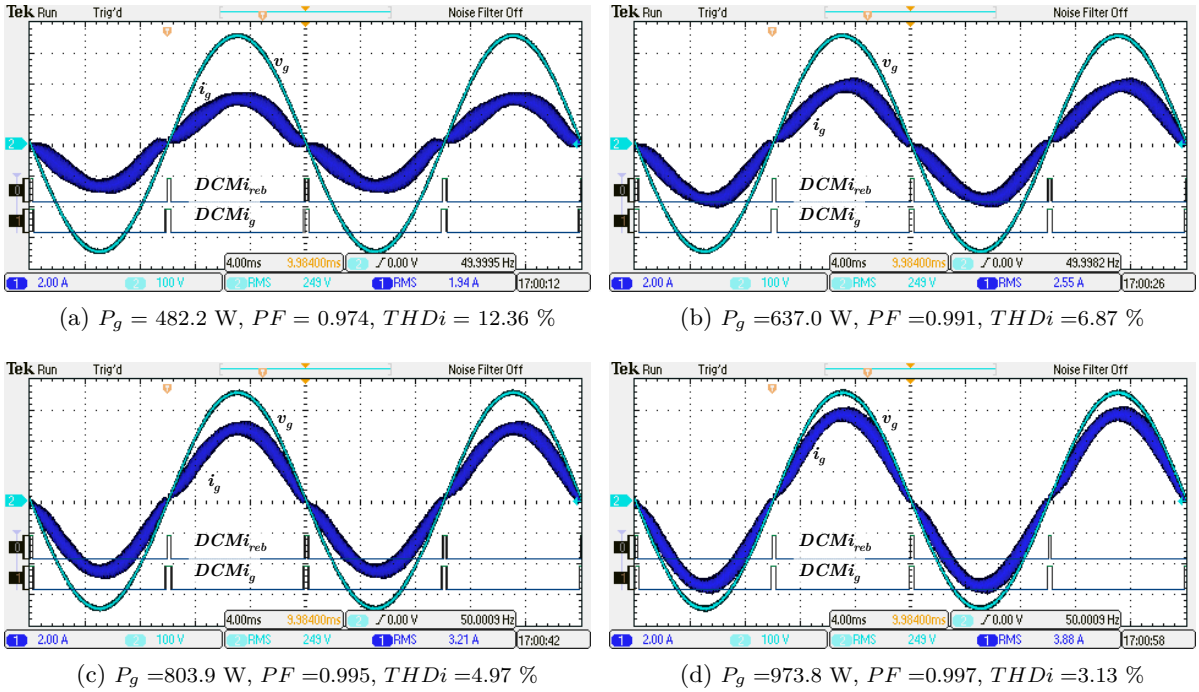
The steady state experimental results, with the digital controller settled with a constant switching frequency of 72 kHz, presented in figures 8.4, 8.5, 8.6, 8.7, 8.8, show the waveforms captured under 250, 230, 180, 120 and 85 V_{rms} input voltage, respectively; at different power levels. The power level, power factor and total harmonic distortion values are introduced in each capture caption. Furthermore, Table 8.2 presents all the captured values together for the waveforms previously presented. In each case, the current harmonics (up to 11^{th} harmonic) are addressed too, compared with the current limits defined by the IEC 61000-3-2 Std for Class C equipment.

It can be seen that in all the cases, power factor correction is achieved and DCM signals $DCMi_{reb}$ and $DCMi_g$ are matched despite not measuring the input (inductor) current. The best PF and $THDi$ are obtained at higher power levels, and in all the tested conditions, the current limits given by the standard are higher than the experimental results. It must be remarked that the digital controller has not been re-tuned or modified to operate under the different conditions, showing the universality of the approach presented in this work.

The ON-time (t^*_{on}), and the ON-time modification measurement ($\Delta t^{meas}_{on} \approx \Delta t_{on}$) due to the drive signal delays over the half line cycle are shown in Fig. 8.9 for different loads (320 W,

				Current Harmonics (A)						
V_g	P_g	PF	$THDi$	I_1	I_2	I_3	I_5	I_7	I_9	I_{11}
250 V	482.2 W	0.974	12.36 %	1.726	0.006	0.195	0.06	0.032	0.024	0.016
				Limits	0.035	0.505	0.173	0.121	0.086	0.052
	637.0W	0.991	6.87 %	2.562	0.005	0.172	0.031	0.008	0.016	0.005
				Limits	0.051	0.762	0.256	0.179	0.128	0.077
	803.9 W	0.995	4.97 %	3.222	0.003	0.154	0.040	0.016	0.011	0.007
				Limits	0.064	0.962	0.322	0.226	0.161	0.097
	973.8 W	0.997	3.13 %	3.901	0.004	0.110	0.049	0.024	0.015	0.003
				Limits	0.078	1.167	0.390	0.273	0.195	0.117
230 V	319.7 W	0.974	9.48 %	1.38	0.003	0.112	0.068	0.013	0.020	0.005
				Limits	0.028	0.403	0.138	0.097	0.069	0.041
	480.2 W	0.985	8.76 %	2.09	0.004	0.177	0.032	0.019	0.016	0.007
				Limits	0.042	0.619	0.209	0.147	0.105	0.063
	637.5 W	0.990	6.85 %	2.782	0.004	0.186	0.034	0.025	0.009	0.004
				Limits	0.056	0.827	0.278	0.195	0.139	0.083
	804.8 W	0.995	4.20 %	3.509	0.004	0.135	0.051	0.029	0.013	0.005
				Limits	0.070	1.047	0.351	0.246	0.175	0.105
	975.2 W	0.997	2.55 %	4.253	0.004	0.089	0.048	0.039	0.018	0.003
				Limits	0.085	1.272	0.425	0.298	0.213	0.128
180 V	320.7 W	0.979	8.00 %	1.789	0.003	0.134	0.049	0.011	0.003	0.005
				Limits	0.036	0.525	0.179	0.125	0.089	0.054
	484.1W	0.990	4,88 %	2.69	0.004	0.113	0.064	0.024	0.007	0.004
				Limits	0.054	0.801	0.270	0.018	0.135	0.081
	646.5 W	0.995	2.96 %	3.600	0.003	0.061	0.082	0.027	0.006	0.006
				Limits	0.072	1.074	0.360	0.252	0.180	0.180
	817.9 W	0.996	3.17 %	4.555	0.005	0.099	0.101	0.028	0.011	0.005
				Limits	0.091	1.361	0.405	0.318	0.228	0.137
120 V	157.3 W	0.968	10.99 %	1.357	0.007	0.146	0.023	0.013	0.013	0.012
				Limits	0.027	0.394	0.136	0.095	0.068	0.041
	327.6 W	0.991	5.81 %	2.741	0.005	0.155	0.036	0.013	0.008	0.005
				Limits	0.055	0.815	0.274	0.192	0.137	0.082
	496.8 W	0.997	2.22 %	4.153	0.004	0.076	0.045	0.026	0.019	0.016
				Limits	0.083	1.242	0.415	0.291	0.208	0.125
85 V	164.2 W	0.989	5.06 %	1.939	0.004	0.079	0.059	0.005	0.006	0.008
				Limits	0.039	0.575	0.194	0.136	0.097	0.058
	340.2 W	0.996	3.33 %	4.022	0.005	0.084	0.087	0.052	0.047	0.008
				Limits	0.080	1.202	0.402	0.282	0.201	0.121

Table 8.2: Experimental results in steady state with a switching frequency f_{sw} =72 kHz



(a) P_g = 482.2 W, PF = 0.974, $THDi$ = 12.36 %

(b) P_g =637.0 W, PF =0.991, $THDi$ =6.87 %

(c) P_g =803.9 W, PF =0.995, $THDi$ =4.97 %

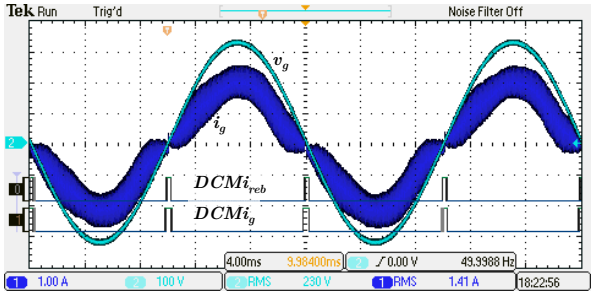
(d) P_g =973.8 W, PF =0.997, $THDi$ =3.13 %

Figure 8.4: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =250 V_{rms} - 50 Hz, at 72 kHz switching frequency for different power levels.

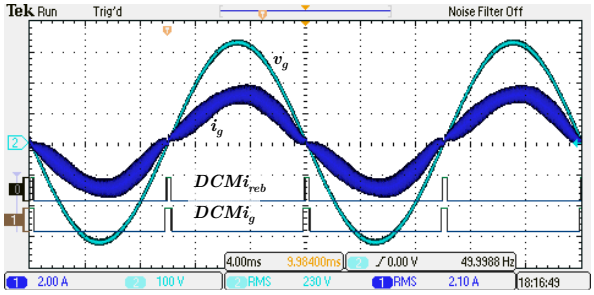
480 W and 970 W) in steady state, when the DCM times are matched (i_g with sinusoidal shape). These delays are function of the MOSFET gate resistor value and the, drain current and the MOSFET parasitic elements. These values are measured, every switching period, with the circuit shown in Fig. 5.4. These measured values are used in the digital controller to compensate the PFC algorithm as it has been presented in Section 5.2 . The drive signal delays are measured in the switching period $j-1$, to be applied in the compensation in the switching period j.

Figure 8.10 shows the experimental PF values measured at 640 W for different values of the delays used in the compensation algorithm $\triangle t_{on}^{meas}$, constant over the half line cycle $\triangle t_{on}^{meas}[j] = \triangle t_{on}^{meas}\ \forall\, j$. The experimental results, compared with the results presented in Table 8.2, shows in what extend this assumption causes an important current distortion with PF values always lower than 0.98 . Input voltage and current waveforms of two situations are shown in Fig. 8.11, that corresponds to $\triangle t_{on}^{meas}$ =100 ns (Fig. 8.11a) and 220 ns (Fig. 8.11b) cases. These results demonstrate that feedforward compensation with the continuous measurement of the switching delays is needed, and constant switching delays consideration does not assure sinusoidal input current [154].

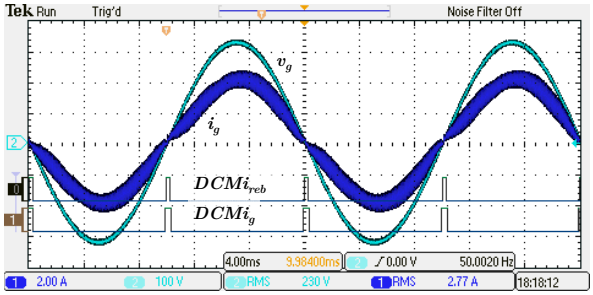
Figure 8.12 shows the main waveforms of the DCM condition detection circuit for the real input current, with $R_{ds1} = R_a = 1.2\ M\Omega$ and $R_{ds2} = R_b = 9.31\ k\Omega$. The digital signal, $DCMi_g$ changes to '1' when the first DCM oscillation in the drain-to-source voltage occurs. It can be seen how experimental and theoretical waveforms (Fig. 5.6) are in good agreement.



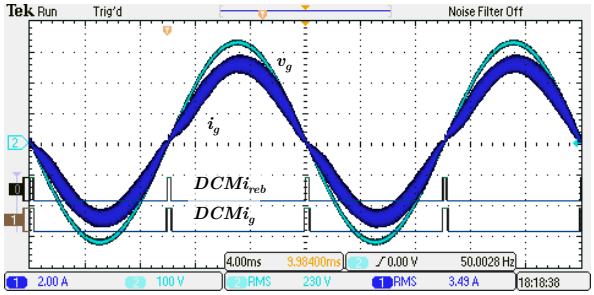
(a) P_g =319.7 W, PF =0.974, $THDi$ =9.48 %



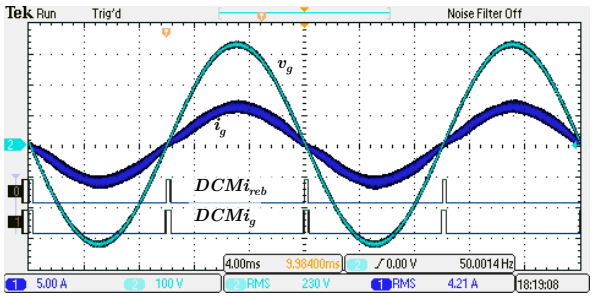
(b) P_g =480.2 W, PF =0.985, $THDi$ =8.76 %



(c) P_g =637.5 W, PF =0.990, $THDi$ =6.85 %

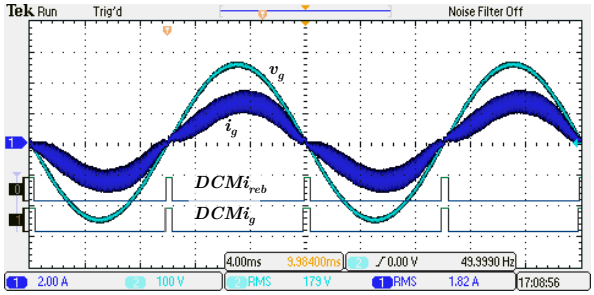


(d) P_g =804.8 W, PF =0.995, $THDi$ =4.20 %

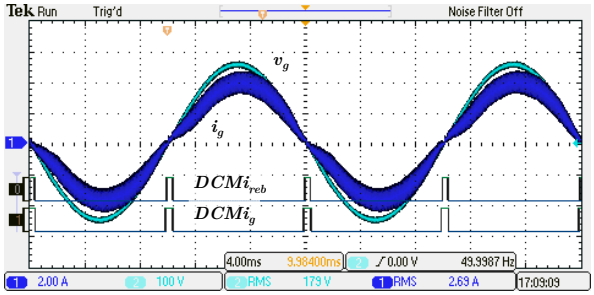


(e) P_g =975.2 W, PF =0.997, $THDi$ =2.55 %

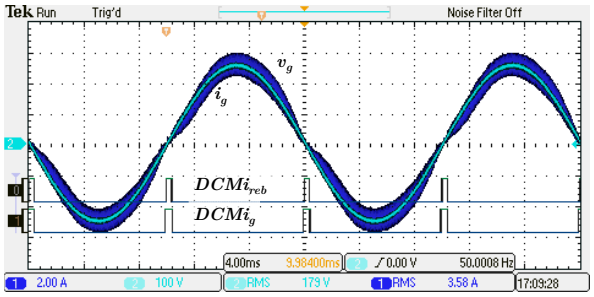
Figure 8.5: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =230 V_{rms} - 50 Hz, at 72 kHz switching frequency for different power levels.



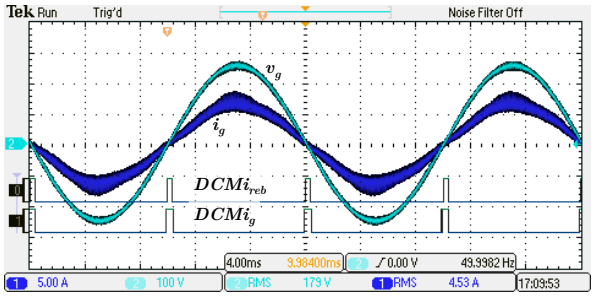
(a) P_g =320.7 W, PF =0.979, $THDi$ =8.00 %



(b) P_g =484.1 W, PF =0.990, $THDi$ =4.88 %

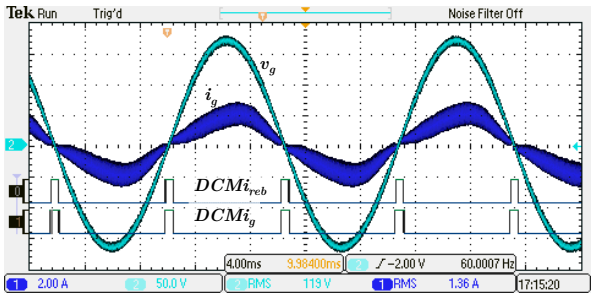


(c) P_g =646.5 W, PF =0.995, $THDi$ =2.96 %

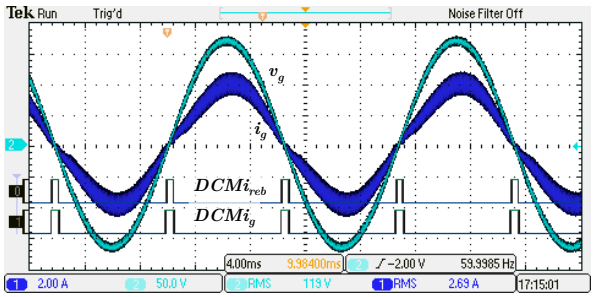


(d) P_g =817.9 W, PF =0.996, $THDi$ =3.17 %

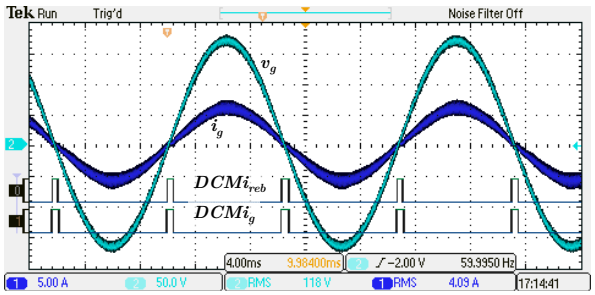
Figure 8.6: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =180 V_{rms} - 50 Hz, at 72 kHz switching frequency for different power levels.



(a) P_g =157.3 W, PF =0.968, $THDi$ =10.99 %

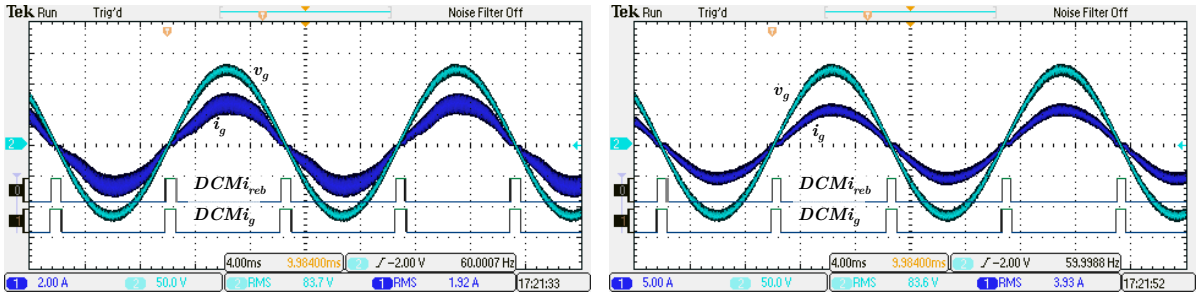


(b) P_g =327.6 W, PF =0.991, $THDi$ =5.81 %



(c) P_g =496.8 W, PF =0.997, $THDi$ =2.22 %

Figure 8.7: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =120 V_{rms} - 60 Hz, at 72 kHz switching frequency for different power levels.



(a) P_g =164.2 W, PF =0.989, $THDi$ =5.06 %

(b) P_g =340.2 W, PF =0.996, $THDi$ =3.33 %

Figure 8.8: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =85 V_{rms}, at 72 kHz switching frequency for different power levels.

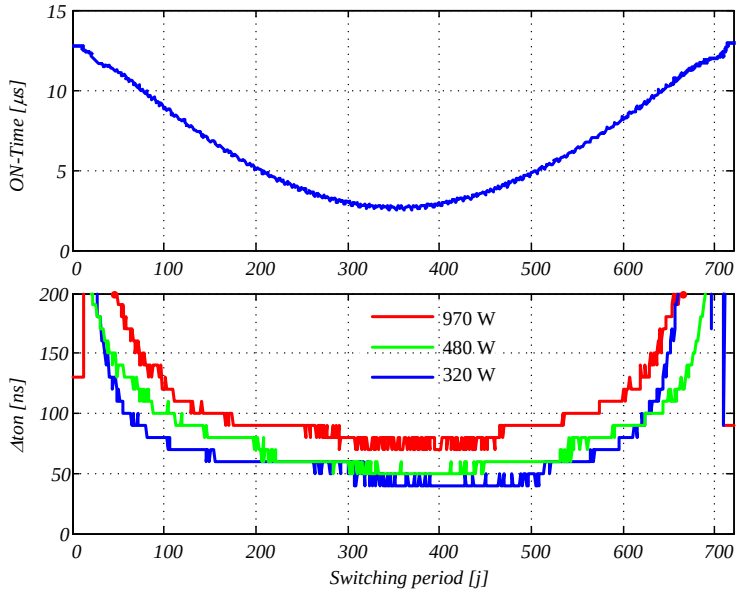


Figure 8.9: Experimental results: Value of the duty cycle modification ($\triangle t_{on}$) due to the drive signal delays over the half line cycle.

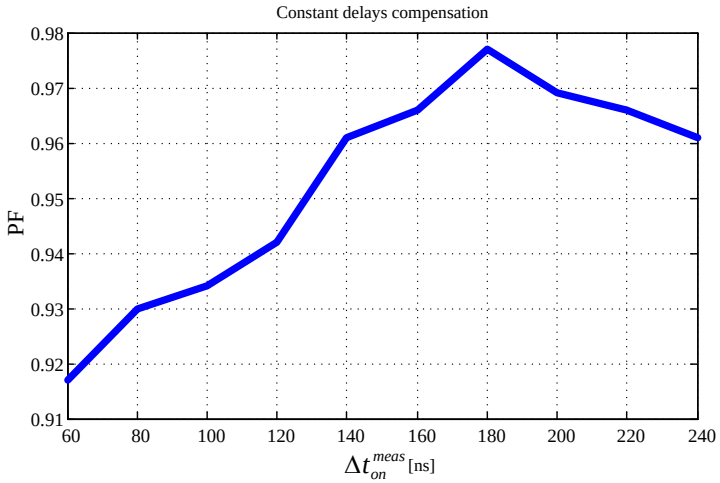
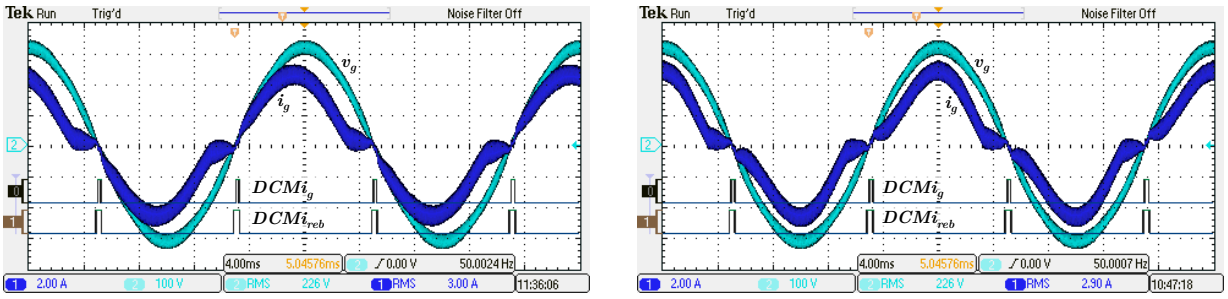


Figure 8.10: Power factor value for different delays used in the feedforward compensation when they are considered constant over the half line cycle.



(a) (b)

Figure 8.11: Input current and voltage waveforms if the feedforward is done considering constant drive signal delays. (a) $\triangle t_{on}^{meas}$ =100 ns and (b) $\triangle t_{on}^{meas}$ =220 ns

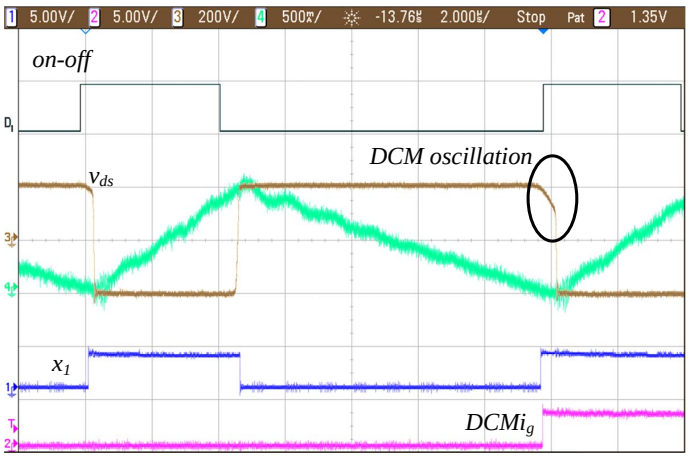


Figure 8.12: Experimental results for the DCM condition detection circuit for the real input current.

To demonstrate the universality of the controller with feedback control, a second inductor (L_2) has been built, and the experimental results are achieved without modifying any parameter of the digital controller (the DCM time feedback loop sets the new value of the signal v_{dig}). The two inductors used in these experimental validation are shown in Fig. 8.13. The first inductor has been built with a RM12-3C90 core, resulting in the inductance $L = 1\,mH$ and a measured parasitic resistor in series $R_L = 0.25\,\Omega$. The second inductor (L_2) has been built with a soft saturation Kool mμ core 77071. In this case, the inductance $L_2 = 1.5\,mH$ with $R_{L2} = 0.35\,\Omega$ at zero current level. The experimental results in steady-state operation are shown in Fig. 8.14 for two different input voltages (85 V_{rms}– 60 Hz and 230 V_{rms} – 50 Hz), output power and the inductance L_2. It can be observed that a sinusoidal input current is achieved and DCM times are matched. Power factor and Total harmonic distortion of the input current ($THDi$) values are listed in Table 8.3 for wide input voltage (from 85 V_{rms} – 60 Hz to 230 V_{rms} – 50 Hz) and output power ranges.

Measured $THDi$ are a little higher with L_2 than with L at high power load, despite $L_2 > L$. This is caused by the current dependent inductance of the inductor built with a soft saturation core [150, 151]. The aim of using this inductance in the proposed controller is to show the behavior of the controller under two different conditions. The use of L_2 on one hand introduces a non-linear behavior (addressed in Section 3.3.3) that produces higher current distortion as the current increases, and on the other hand, keeps the CCM operation for a higher load range. Despite this aspect, the experimental results present high power factor values for all the tested conditions. It must be remarked that the digital controller has not been modified to operate under these different conditions, showing the universality of the approach presented in this work, with a switching frequency and inductance value similar to the traditional and commercial analog PFC designs.

The same steady state results are presented with the switching frequency settled at 96 kHz and 144 kHz, with the same devices addressed before. All the results have been obtained

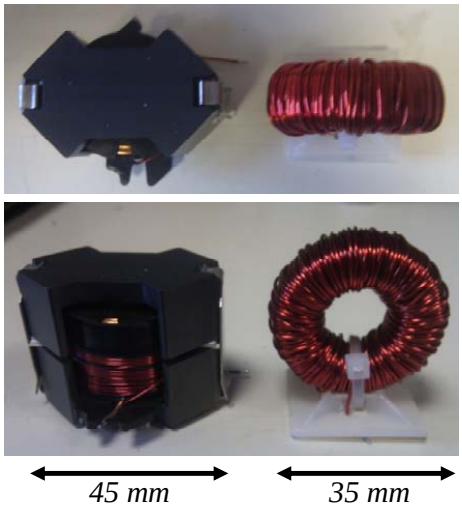
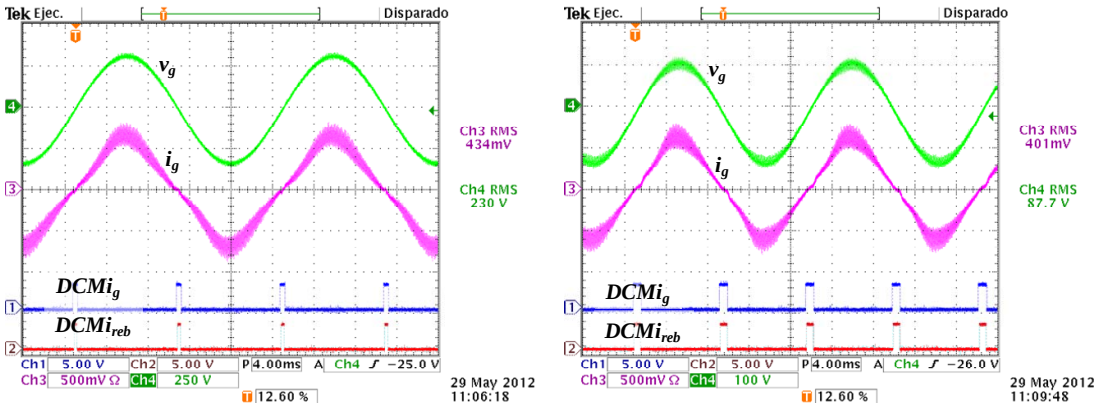


Figure 8.13: Inductors used in the experimental results. Left: $L = 1\,mH$ (RM12-3C90 core with $R_L = 0.25\,\Omega$). Right: $L_2 = 1.5\,mH$ (soft saturation Kool mμ core with $R_{L2} = 0.35\,\Omega$).



(a) (b)

Figure 8.14: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). $V_o = 400\,V_{dc}$ and $L_2 = 1.5mH$ ($R_{L2} = 0.35\,\Omega$). (a): $V_g = 230\,V_{rms}(50Hz)$, $P_g = 970\,W$. (b): $V_g = 85\,V_{rms}(60Hz)$, $P_g = 320\,W$.

Experimental results with $L_2 = 1.5\,mH$			
V_g	P_g	PF	$THDi$
250	460 W	0.975	9.0 %
	645 W	0.991	8.5 %
	800 W	0.993	9.5 %
	970 W	0.993	10.5 %
230	460 W	0.984	8.1 %
	640 W	0.988	9.1 %
	800 W	0.992	9.8 %
	970 W	0.993	10.5 %
180	323 W	0.980	5.4 %
	485 W	0.989	7.1 %
	650 W	0.992	8.6 %
	820 W	0.991	10.5 %
120	497 W	0.996	9.8 %
	323 W	0.988	9.8 %
	497 W	0.996	9.8 %
85	161 W	0.989	5.0 %
	336 W	0.993	9.0 %

Table 8.3: Power Factor and $THDi$ values under different conditions.

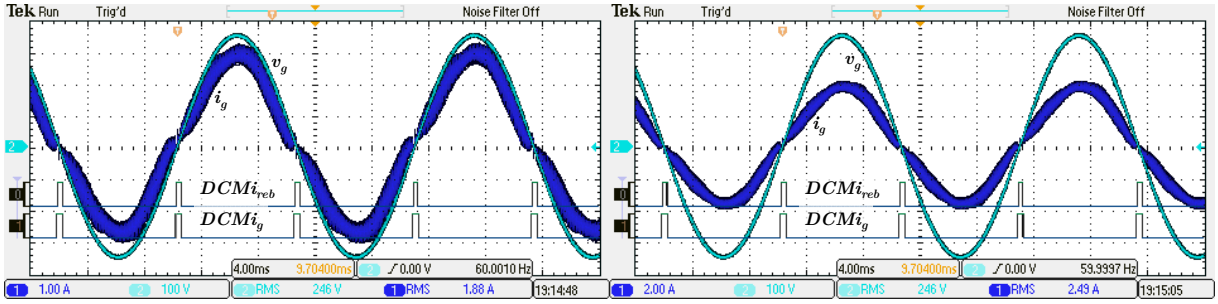
with the initial mentioned inductance L =1 mH ($R_L = 0.25\,\Omega$). It must be remarked that only the switching frequency has been modified, not controller coefficients, that are the same for all the conditions. Figures 8.15, 8.16, 8.17, 8.18 and 8.19 show the waveforms captured at 250, 230, 180, 120 and 85 V_{rms} input voltage, respectively; at different power levels with the digital controller tuned at 96 kHz, that corresponds with the measured data presented in Table 8.4.

And the steady state results obtained which a switching frequency of 144 kHz are enumerated in Table 8.5 for the same conditions presented before. The waveforms captured in those conditions are shown in Fig. 8.20, 8.21, 8.22, 8.23 and 8.24.

8.3 Time evolution under different conditions

In Chapters 4 and 5, a digital compensation of all the current estimation error that can occur in the sensorless controller for Boost PFC rectifiers has been presented. Among all the causes of current estimation error, the influence of the parasitic elements is the only one that depends on the current/power level. The DCM times feedback loop is needed to assure the correct behavior under different conditions. To illustrate the behavior of the proposed digital compensation, the time evolution of the PF and $THDi$ values are plotted in the time domain. A Voltech PM1000+ Power Analyzer is used to capture these data, with a sample period of 1 second.

Figure 8.25 shows the time evolution of these variables under different load steps, with an European Grid input voltage and a constant switching frequency of 144 kHz. The evolution



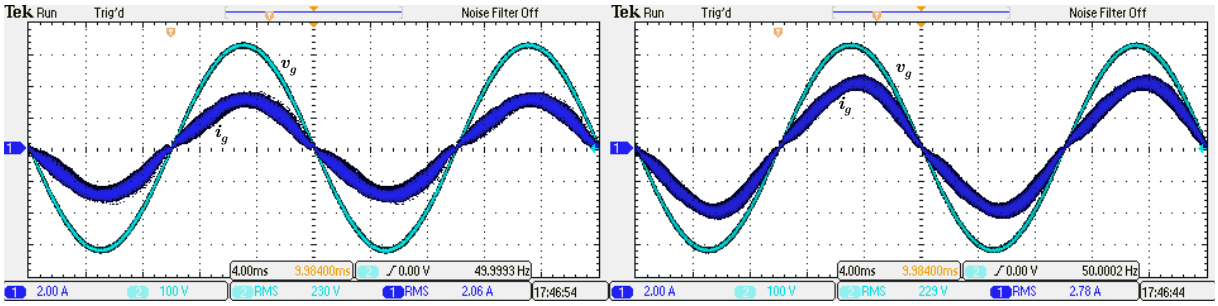
(a) P_g =481.9 W, PF =0.992, $THDi$ =5.86 %

(b) P_g =639.6 W, PF =0.995, $THDi$ =5.45 %

(c) P_g =806.9 W, PF =0.997, $THDi$ =2.99 %

(d) P_g =976.3 W, PF =0.998, $THDi$ =2.68 %

Figure 8.15: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =250 V_{rms} - 50 Hz, at 96 kHz switching frequency for different power levels.



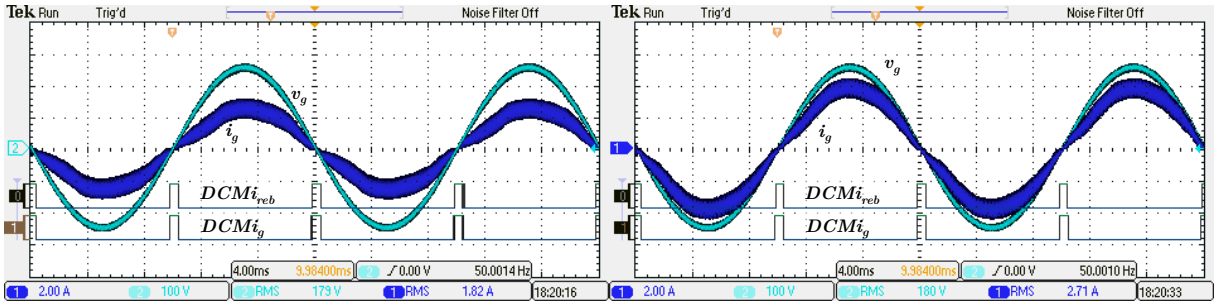
(a) P_g =480.6 W, PF =0.991, $THDi$ =6.17 %

(b) P_g =637.8 W, PF =0.993, $THDi$ =6.90 %

(c) P_g =803.9 W, PF =0.996, $THDi$ =4.57 %

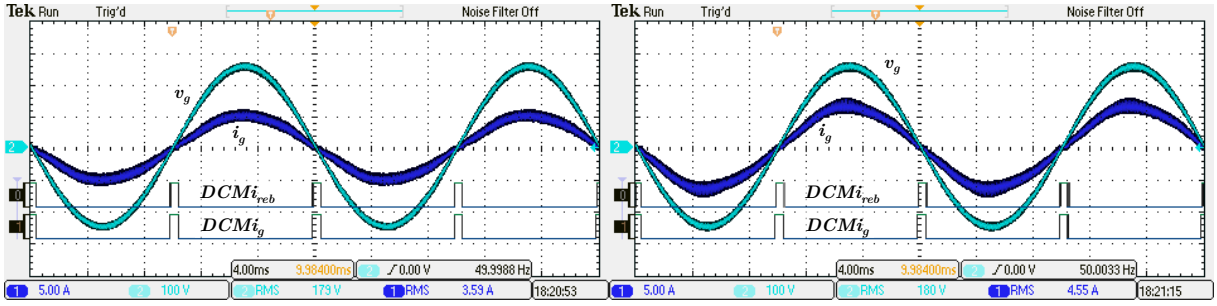
(d) P_g =977.1 W, PF =0.998, $THDi$ =2.55 %

Figure 8.16: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =230 V_{rms} - 50 Hz, at 96 kHz switching frequency for different power levels.



(a) P_g =324.6 W, PF =0.989, $THDi$ =4.85 %

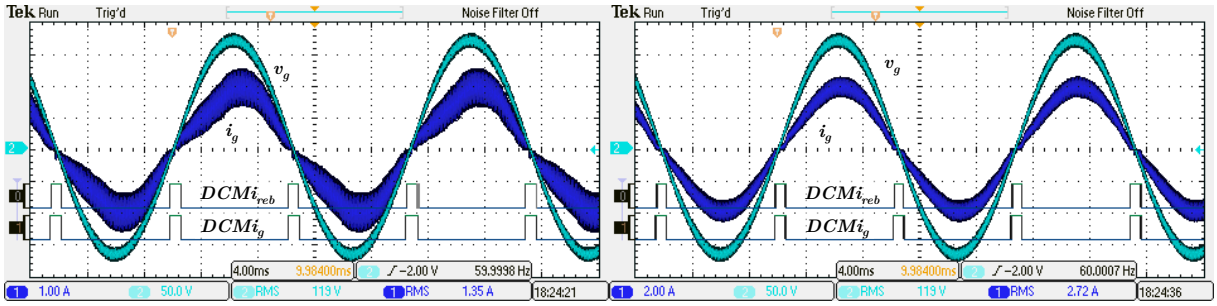
(b) P_g =488.3 W, PF =0.995, $THDi$ =3.02 %



(c) P_g =651.4 W, PF =0.997, $THDi$ =2.27 %

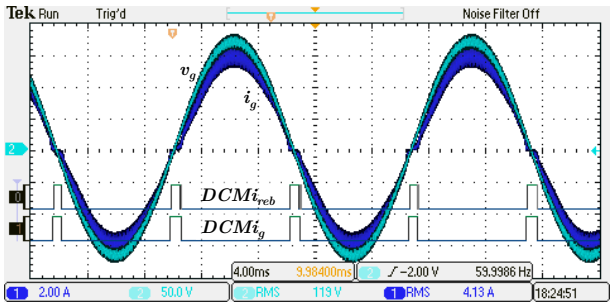
(d) P_g =822.9 W, PF =0.998, $THDi$ =2.92 %

Figure 8.17: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =180 V_{rms} - 50 Hz, at 96 kHz switching frequency for different power levels.



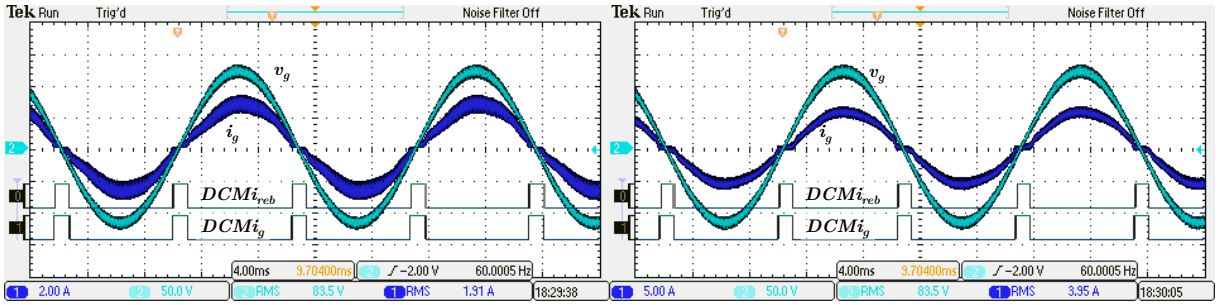
(a) P_g =162.2 W, PF =0.979, $THDi$ =9.29 %

(b) P_g =329.4 W, PF =0.994,$THDi$ =4.26 %



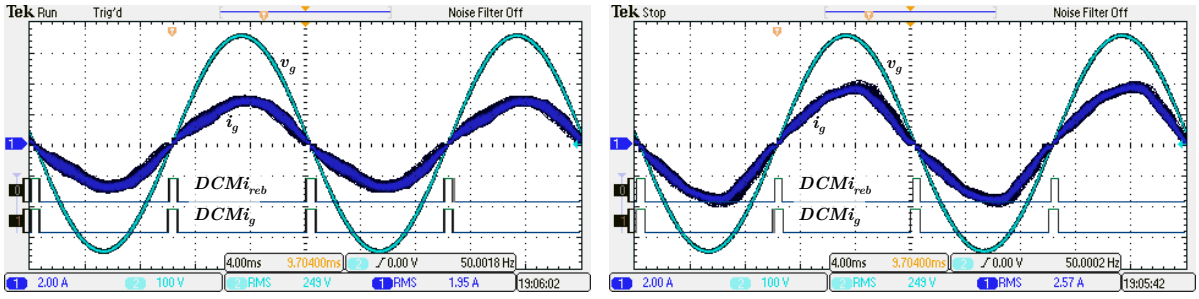
(c) P_g =500.0 W, PF =0.996, $THDi$ =2.43 %

Figure 8.18: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =120 V_{rms} - 60 Hz, at 96 kHz switching frequency for different power levels.

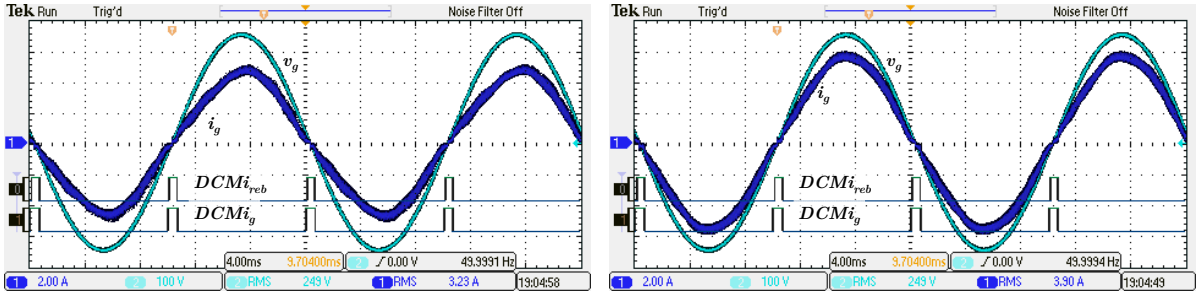


(a) P_g =165.1 W, PF =0.991, $THDi$ =5.62 % (b) P_g =340.7 W, PF =0.994, $THDi$ =4.80 %

Figure 8.19: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =85 V_{rms}, at 96 kHz switching frequency for different power levels.



(a) P_g =480.5 W, PF =0.992, $THDi$ =7.57 % (b) P_g =638.8 W, PF =0.994, $THDi$ =6.99 %

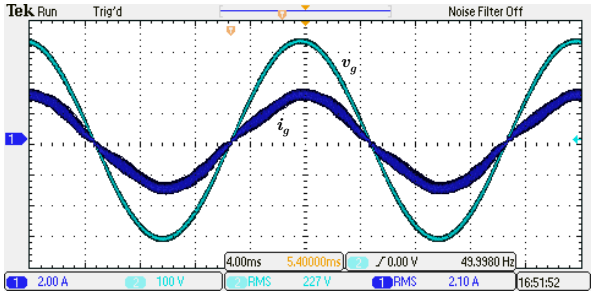


(c) P_g =806.7 W, PF =0.997, $THDi$ =5.55 % (d) P_g =978.4 W, PF =0.999, $THDi$ =3.07 %

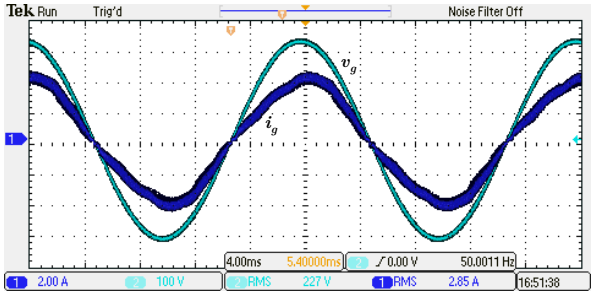
Figure 8.20: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =250 V_{rms} - 50 Hz, at 144 kHz switching frequency for different power levels.

				Current Harmonics (A)						
V_g	P_g	PF	$THDi$	I_1	I_2	I_3	I_5	I_7	I_9	I_{11}
250 V	481.9 W	0.992	5.86 %	1.919	0.006	0.114	0.037	0.007	0.019	0.021
				Limits	0.038	0.517	0.192	0.134	0.096	0.058
	639.6 W	0.995	5.45 %	2.560	0.006	0.133	0.031	0.020	0.005	0.013
				Limits	0.051	0.764	0.256	0.179	0.128	0.077
	806.9 W	0.997	2.99 %	3.231	0.007	0.091	0.044	0.023	0.017	0.009
				Limits	0.065	0.966	0.323	0.226	0.162	0.097
	976.3 W	0.998	2.68 %	3.908	0.007	0.094	0.052	0.031	0.022	0.021
				Limits	0.078	1.170	0.391	0.274	0.195	0.117
230 V	480.6 W	0.991	6.17 %	2.586	0.007	0.156	0.038	0.013	0.005	0.014
				Limits	0.052	0.769	0.259	0.181	0.129	0.078
	637.8 W	0.993	6.90 %	2.784	0.006	0.189	0.023	0.023	0.011	0.012
				Limits	0.056	0.829	0.278	0.195	0.139	0.084
	803.9 W	0.996	4.57 %	3.513	0.007	0.129	0.059	0.020	0.010	0.011
				Limits	0.070	1.049	0.351	0.246	0.176	0.105
	977.1 W	0.998	2.55 %	4.251	0.010	0.078	0.063	0.032	0.007	0.011
				Limits	0.085	1.273	0.425	0.298	0.213	0.128
180 V	324.6 W	0.989	4,85 %	1.813	0.009	0.050	0.068	0.005	0.013	0.006
				Limits	0.036	0.538	0.181	0.127	0.091	0.054
	488.3 W	0.995	3.02 %	2.717	0.010	0.047	0.062	0.014	0.06	0.003
				Limits	0.054	0.811	0.272	0.190	0.136	0.081
	651.4 W	0.997	2.27 %	3.629	0.007	0.038	0.064	0.024	0.008	0.006
				Limits	0.073	1.085	0.363	0.254	0.181	0.109
	822.9 W	0.998	2.92 %	4.584	0.014	0.105	0.079	0.033	0.017	0.016
				Limits	0.092	1.373	0.458	0.321	0.229	0.138
120 V	162.2 W	0.979	9.29 %	1.366	0.009	0.124	0.008	0.013	0.014	0.008
				Limits	0.027	0.401	0.137	0.096	0.068	0.041
	329.4 W	0.994	4.26 %	2.764	0.009	0.111	0.034	0.017	0.013	0.016
				Limits	0.055	0.824	0.276	0.193	0.138	0.083
	500.0 W	0.996	2.43 %	4.178	0.011	0.067	0.065	0.046	0.040	0.037
				Limits	0.084	1.248	0.418	0.292	0.209	0.125
85 V	165.1 W	0.991	5.62 %	1.953	0.006	0.097	0.044	0.016	0.023	0.028
				Limits	0.039	0.580	0.195	0.137	0.098	0.059
	340.7 W	0.994	4.80 %	4.046	0.005	0.104	0.137	0.090	0.085	0.073
				Limits	0.081	1.207	0.405	0.283	0.202	0.121

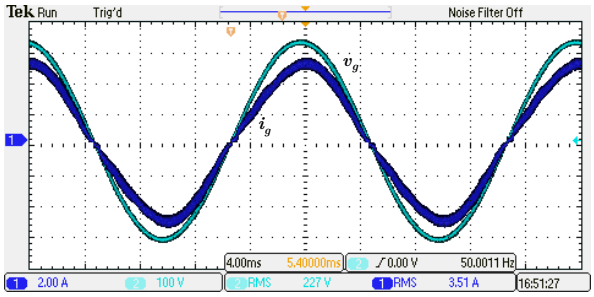
Table 8.4: Experimental results with a switching frequency of 96 kHz.



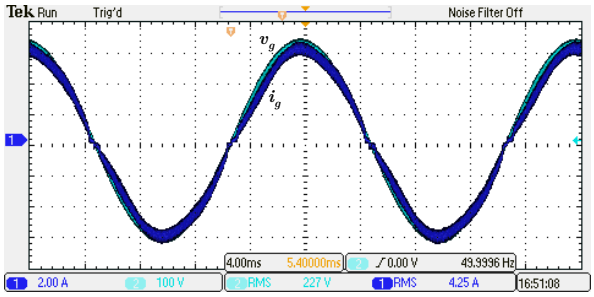
(a) P_g =483.1 W, PF =0.994, $THDi$ =6.20 %



(b) P_g =640.6 W, PF =0.994, $THDi$ =6.93 %

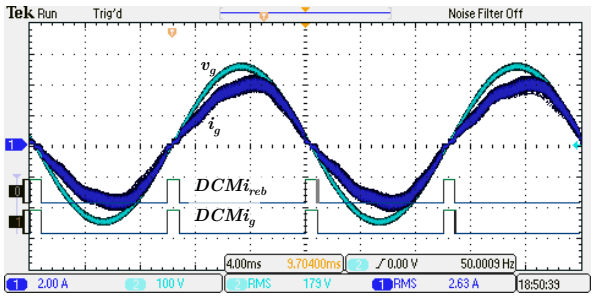


(c) P_g =807.2 W, PF =0.995, $THDi$ =5.48 %

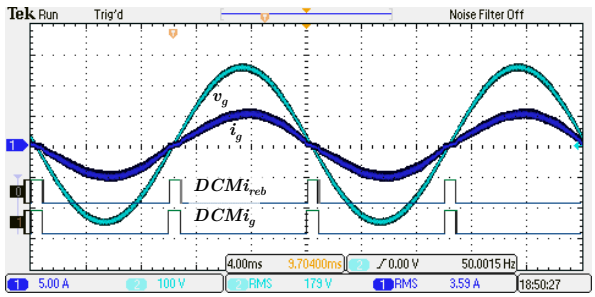


(d) P_g =978.8 W, PF =0.998, $THDi$ =2.78 %

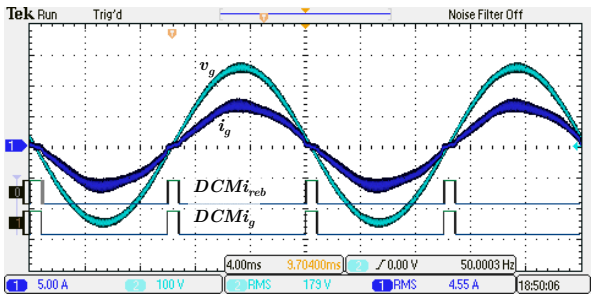
Figure 8.21: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =230 V_{rms} - 50 Hz, at 144 kHz switching frequency for different power levels.



(a) P_g =487.5 W, PF =0.993, $THDi$ =6.53 %

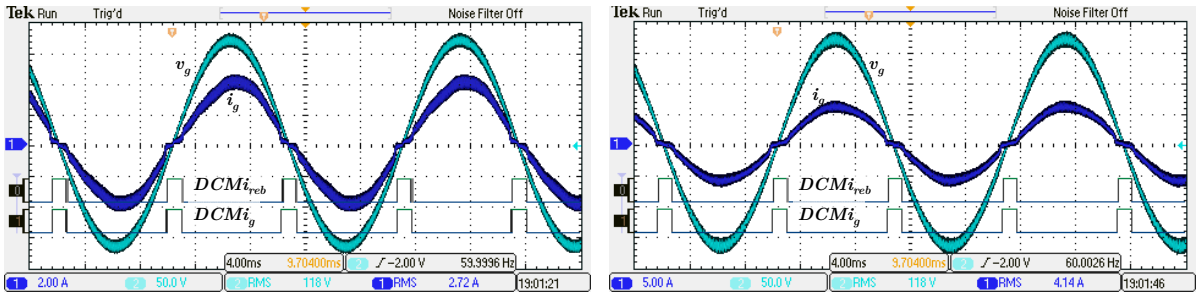


(b) P_g =648.4 W, PF =0.994, $THDi$ =4.91 %



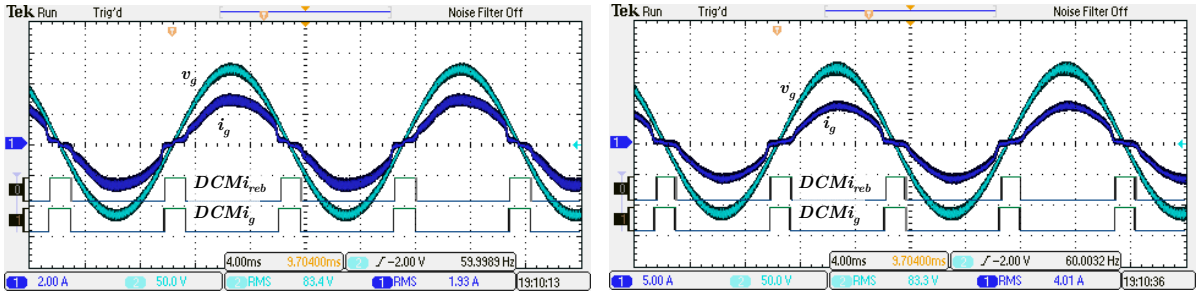
(c) P_g =821.8 W, PF =0.996, $THDi$ =3.50 %

Figure 8.22: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =180 V_{rms} - 50 Hz, at 144 kHz switching frequency for different power levels.



(a) P_g =331.5 W, PF =0.992, $THDi$ =6.61 % (b) P_g =503.9 W, PF =0.995, $THDi$ =5.18 %

Figure 8.23: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =120 V_{rms} - 60 Hz, at 144 kHz switching frequency for different power levels.



(a) P_g =167.4 W, PF =0.991, $THDi$ =7.83 % (b) P_g =346.6 W, PF =0.988, $THDi$ =11.13 %

Figure 8.24: Experimental results: input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). Waveforms under V_g =85 V_{rms}, at 144 kHz switching frequency for different power levels.

				Current Harmonics (A)						
V_g	P_g	PF	$THDi$	I_1	I_2	I_3	I_5	I_7	I_9	I_{11}
250 V	480.5 W	0.992	7.57 %	1.932	0.008	0.130	0.031	0.024	0.008	0.014
				Limits	0.039	0.575	0.193	0.135	0.097	0.058
	638.8 W	0.994	6.99 %	2.582	0.011	0.174	0.037	0.033	0.013	0.018
				Limits	0.052	0.770	0.258	0.181	0.129	0.077
	806.7 W	0.997	5.55 %	3.241	0.008	0.177	0.012	0.016	0.007	0.014
				Limits	0.065	0.969	0.324	0.227	0.162	0.097
	978.4 W	0.999	3.07 %	3.888	0.018	0.086	0.057	0.028	0.023	0.012
				Limits	0.078	1.165	0.389	0.272	0.194	0.117
230 V	483.1 W	0.994	6.20 %	2.117	0.003	0.119	0.048	0.026	0.014	0.018
				Limits	0.042	0.632	0.212	0.148	0.106	0.064
	640.6 W	0.994	6.93 %	2.805	0.005	0.189	0.031	0.023	0.020	0.021
				Limits	0.056	0.836	0.281	0.196	0.140	0.084
	807.2 W	0.995	5.48 %	3.544	0.005	0.192	0.018	0.022	0.011	0.008
				Limits	0.071	1.058	0.354	0.248	0.177	0.106
	978.8 W	0.998	2.78 %	4.294	0.004	0.056	0.096	0.038	0.017	0.015
				Limits	0.086	1.285	0.429	0.301	0.215	0.129
180 V	487.5 W	0.993	6.53 %	2.713	0.009	0.144	0.055	0.034	0.010	0.024
				Limits	0.054	0.808	0.271	0.190	0.136	0.081
	648.4 W	0.994	4.91 %	3.620	0.005	0.162	0.062	0.035	0.021	0.018
				Limits	0.072	1.080	0.362	0.253	0.181	0.109
	821.8 W	0.996	3.50 %	4.584	0.004	0.035	0.150	0.044	0.038	0.042
				Limits	0.092	1.370	0.458	0.321	0.229	0.138
120 V	331.5 W	0.992	6.61 %	2.776	0.005	0.166	0.056	0.061	0.042	0.038
				Limits	0.056	0.826	0.278	0.194	0.139	0.083
	503.9 W	0.995	5.18 %	4.223	0.004	0.131	0.142	0.104	0.097	0.081
				Limits	0.084	1.260	0.422	0.296	0.211	0.127
85 V	167.4 W	0.991	7.83 %	1.978	0.004	0.084	0.113	0.063	0.051	0.031
				Limits	0.040	0.588	0.198	0.138	0.099	0.059
	346.6 W	0.988	11.13 %	4.119	0.019	0.293	0.273	0.209	0.123	0.042
				Limits	0.082	1.221	0.412	0.288	0.206	0.124

Table 8.5: Experimental results at 144 kHz of switching frequency.

Results at 230 Vrms - 400 Hz sinusoidal grid									
V_g (V)	P_g (W)	PF	$THDi$ (%)	I_1 (A)	I_3 (A)	I_5 (A)	I_7 (A)	I_9 (A)	I_{11} (A)
224.8	969.4	0.996	1.49	4.32	0.05	0.02	0.03	0.02	0.02
225.7	804.2	0.995	1.66	3.57	0.05	0.02	0.02	0.02	0.02
226.7	631.5	0.992	2.24	2.72	0.06	0.03	0.02	0.01	0.01
225.7	482.1	0.990	3.52	2.13	0.06	0.03	0.02	0.01	0.01
225.7	321.3	0.982	4.35	1.41	0.05	0.03	0.02	0.02	0.01

Table 8.6: Experimental results at 230 V_{rms} - 400 Hz under high frequency line voltages.

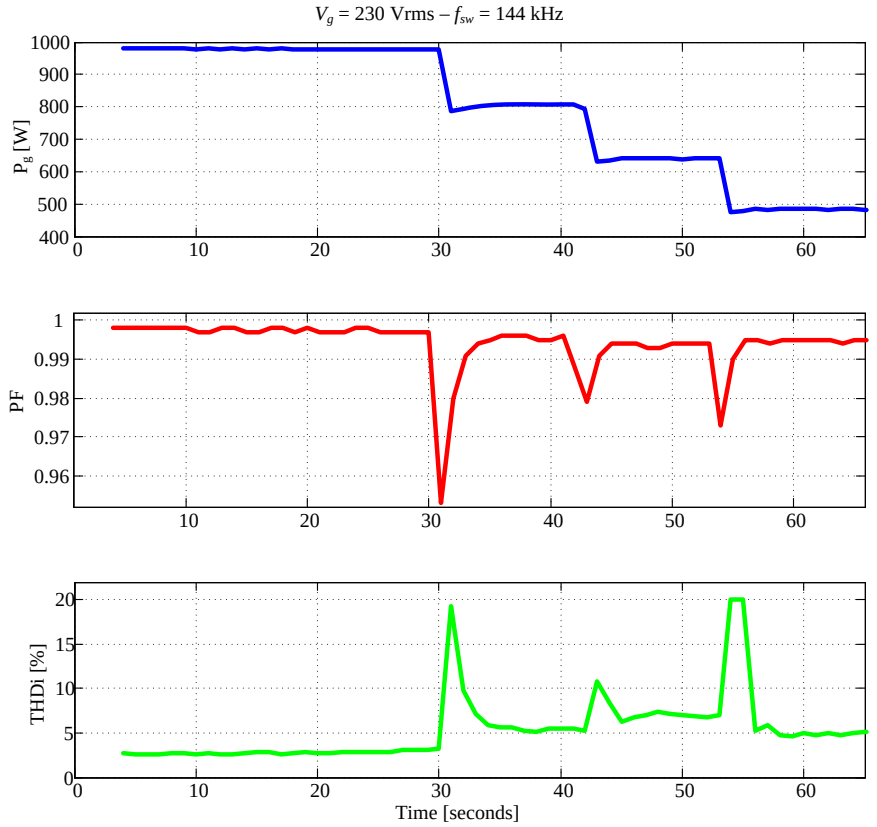
under different load steps-down is plotted in Fig. 8.25a, and in Fig. 8.25b for the step-up evolution. The PF value is high, above 0.990 in all the cases, in steady state as long as the DCM time feedback loop has set $v_{dig} = V_\beta/q$. Just at the load step, PF value decreases (no lower than 0.950 in any case), and starts to increase when the DCM time feedback acts. The time evolution of the $THDi$ value is similar to the PF, having a maximum value of the 20 % in the load steps, but always lower then the 10 % in steady state.

The DCM time feedback loop sets v_{dig} trying to compensate the current estimation error in all the different situations. To evaluate this approach, the converter controlled by the FPGA has been tested under different voltage, grid frequency, and load steps randomly applied.

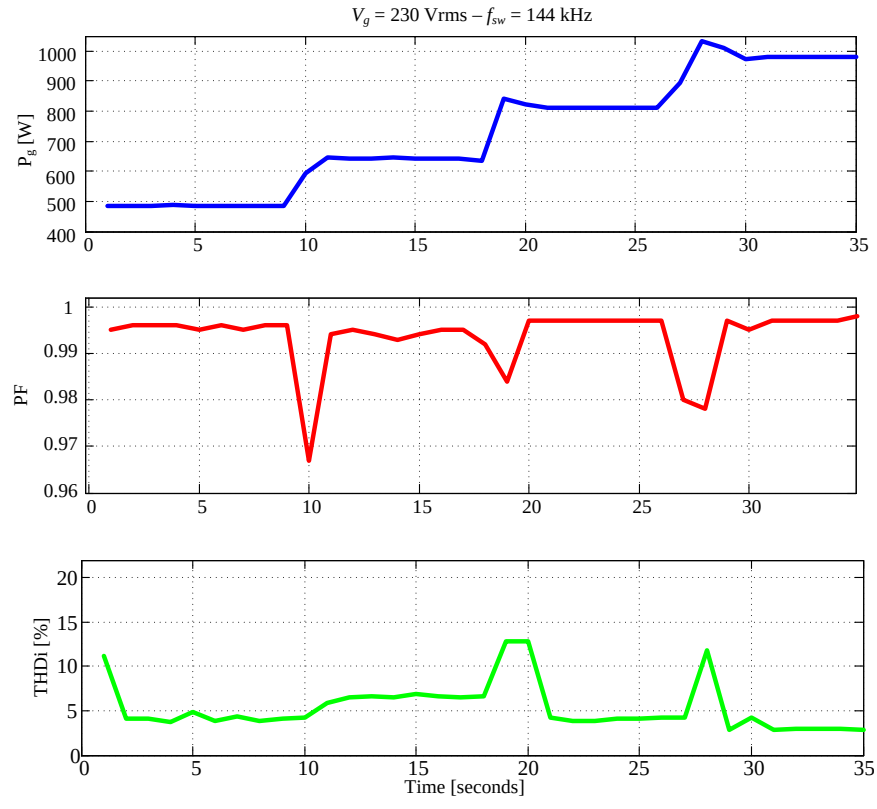
The results of this experiment are presented in Fig. 8.26. The variables V_g and f_u are modified manually in the 6813B AC power source of Agilent, used to supply the boost converter, and the power demanded from the grid P_g is changed with load steps. PF and $THDi$ are the "output" variables used to evaluate the behavior of the controller. It can be seen how every step in V_g, f_u or P_g decreases the PF value. The more aggressive the step is, the higher instantaneous change in the PF value occurs. At the same time, in parallel with the PF modification, the $THDi$ value increases. This current distortion is detected by the DCM time feedback loop that starts to compensate the DCM time mismatch, increasing the PF always with a higher value than 0.990. There are three points where the $THDi$ looks like an impulse but the PF keep high, that corresponds with grid frequency steps-up in which the measurement given by the power analyzer is no correct.

Among the different situations under high frequency grids plotted in Fig. 8.26, the current and voltage waveforms of two of them are presented in Fig. 8.27. Figure 8.27a corresponding to the second 116, and the values of the measurements are V_g =200.7 V, f_u =600 Hz, $THDi$ =1.88 %, PF =0.997, P_g =643.6 W. Figure 8.27b corresponds to the second 165 of the test, and the results are V_g =229.7 V, f_u =360 Hz, $THDi$ =2.15 %, PF =0.998, P_g =968.3 W. It can be seen how the higher is f_u, the lower $THDi$ value is obtained.

More detailed results under a 230 V_{rms} - 400 Hz input voltage at high power level are presented in Table 8.6, with a switching frequency of 96 kHz. The $THDi$ is lower than 2% at high power levels, and is better than the results obtained at 50-60 Hz. The current and voltage waveforms that correspond to the conditions represented in Table 8.6 are presented in Fig. 8.28.



(a)



(b)

Figure 8.25: Power factor and Total harmonic distortion value time evolution under different load steps. $V_o = 400\ V_{dc}$ $V_g = 230\ V_{rms}(50Hz)$, $f_{sw} = 144\ kHz$. (a) Load steps-down. (a) Load steps-up.

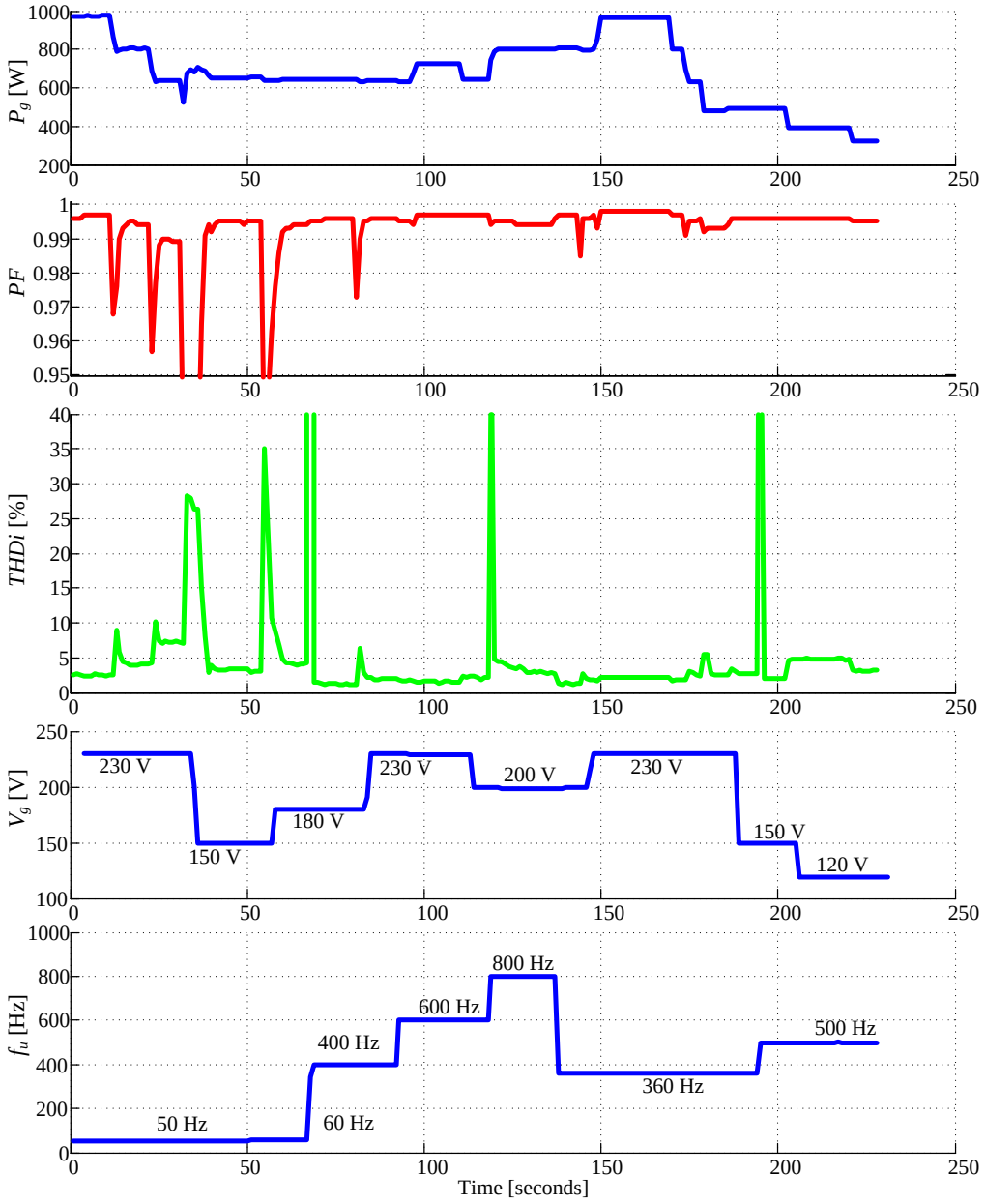
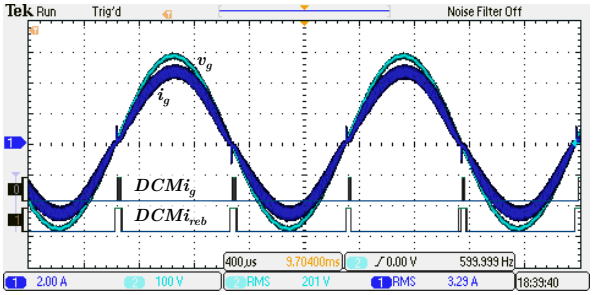
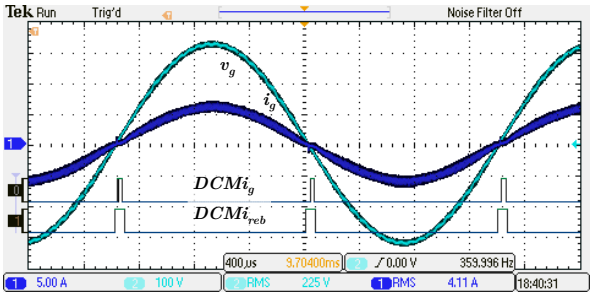


Figure 8.26: Time evolution of the different electrical variables with $V_o = 400V_{dc}$, $f_{sw} = 72kHz$ under different load, grid voltage and grid frequency arbitrary conditions.

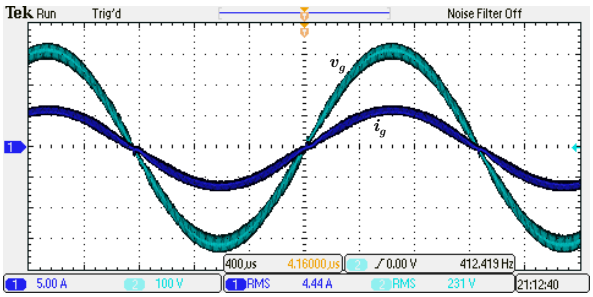


(a) V_g =200.7 V, f_u =600 Hz, $THDi$ =1.88 %, PF =0.997, P_g =643.6 W

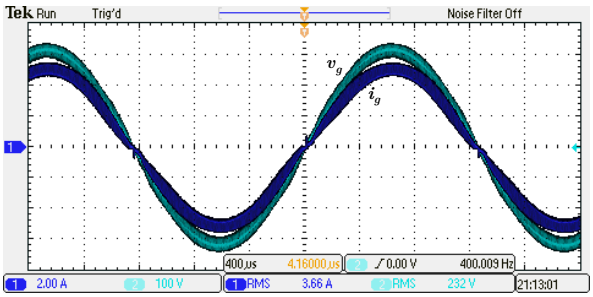


(b) V_g =229.7 V, f_u =360 Hz, $THDi$ =2.15 %, PF =0.998, P_g =968.3 W

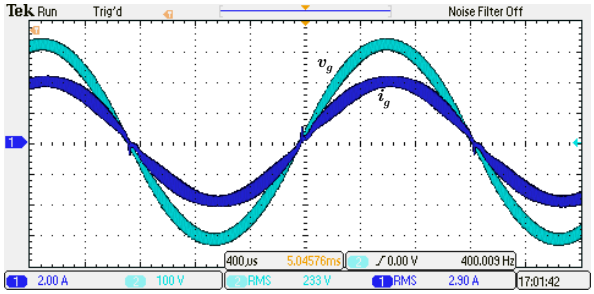
Figure 8.27: Experimental results under high-frequency grids of two instants of the results presented in Fig. 8.26. Input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$).



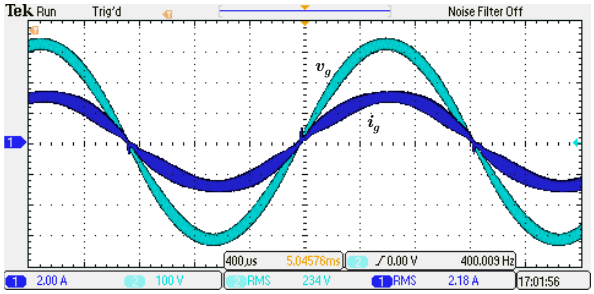
(a) V_g = 224.8 V, f_u = 400 Hz, $THDi$ = 1.49 %, PF = 0.996, P_g = 969.4 W



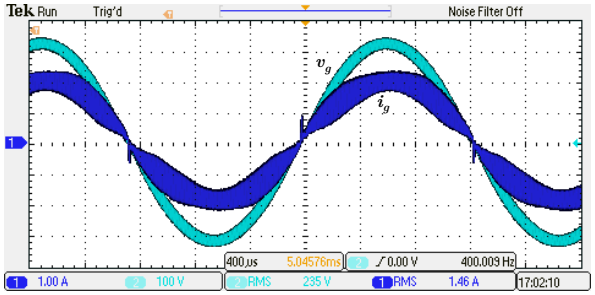
(b) V_g = 225.7 V, f_u = 400 Hz, $THDi$ =1.66 %, PF = 0.995, P_g = 804.2 W



(c) V_g = 226.7 V, f_u = 400Hz, $THDi$ = 2.24 %, PF = 0.992, P_g = 631.5 W



(d) V_g = 225.7 V, f_u = 400 Hz, $THDi$ = 3.52 %, PF = 0.990, P_g = 482.1 W



(e) V_g = 225.7 V, f_u = 400 Hz $THDi$ = 4.35 %, PF = 0.982, P_g = 321.3 W

Figure 8.28: Experimental results under high-frequency grids of two instants of the results presented in Fig. 8.26.

Pure Sinusoidal behavior under distorted voltage										
V_g (V)	P_g (W)	PF	$THDv$ (%)	$THDi$ (%)	I_1 (A)	I_3 (A)	I_5 (A)	I_7 (A)	I_9 (A)	I_{11} (A)
224.8	964.9	0.993	5.05	1.52	4.31	0.03	0.03	0.03	0.02	0.01
225.6	799.5	0.994	5.03	1.81	3.56	0.04	0.04	0.02	0.01	0.01
224.7	963.1	0.990	12.16	3.60	4.32	0.13	0.07	0.02	0.03	0.01
225.5	800.4	0.988	12.17	2.93	3.58	0.06	0.07	0.03	0.03	0.02
Resistance behavior (traditional PFC controller approach)										
V_g (V)	P_g (W)	PF	$THDv$ (%)	$THDi$ (%)	I_1 (A)	I_3 (A)	I_5 (A)	I_7 (A)	I_9 (A)	I_{11} (A)
224.7	966.7	0.996	4.93	4.38	4.30	0.12	0.14	0.03	0.03	0.04
225.6	800.6	0.995	4.92	4.64	3.55	0.11	0.12	0.03	0.02	0.03
224.7	965.1	0.995	11.95	11.25	4.28	0.41	0.16	0.08	0.02	0.01
225.5	800.9	0.995	11.95	11.25	3.53	0.37	0.14	0.07	0.02	0.01

Table 8.7: Experimental results at 230 V_{rms} - 400 Hz under distorted line voltages.

8.4 Operation under distorted voltage. Resistance or pure sinusoidal current behavior

The modification of the NLC controller to demand a totally sinusoidal input current despite an input voltage harmonic distortion has been addressed in Chapter 7. With this, the user can decide what type of behavior is preferred depending on the application, standard or specifications that must be fulfilled by the front-end stage.

To experimentally validate this proposed approach, the boost converter has been tested under a 230 V_{rms} - 400 Hz input voltage, with a 5 % and 12 % of harmonic distortion, for two different power levels (around 965 W and 800 W), and a switching frequency of 96 kHz. These four situations have been tested with the proposed controller approach (pure sinusoidal controller), and with the traditional PFC controller approach (resistance behavior), and the results are resumed in Table 8.7. To supply the front-end stage with a distorted voltage, a 345-AMX AC power source of Pacific is used in which different templates for distorted voltages are predefined.

Comparing the results presented in Table 8.7, it can be seen how the higher power factor values are obtained with the resistance behavior, with a $THDi$ value similar to the $THDv$ of the input voltage; obtaining a power factor value similar to the values obtained under sinusoidal grids. On the other hand, with the new proposal, the current harmonics decrease (above all 3^{th} and 5^{th} harmonic), and therefore the $THDi$ value, despite the voltage distortion.

The current and voltage waveforms of the different situations, enumerated in Table 8.7, are shown in Fig. 8.29 and 8.30 for the pure sinusoidal behavior and the traditional PFC approach of resistance emulator, respectively. The v_g waveform given by the AC power source is similar to the real grid waveform, with a trapezoidal shape, caused by the 5^{th} harmonic with a phase lag of 180 degrees, and the 3^{th} and 7^{th} harmonic in phase with the fundamental harmonic component.

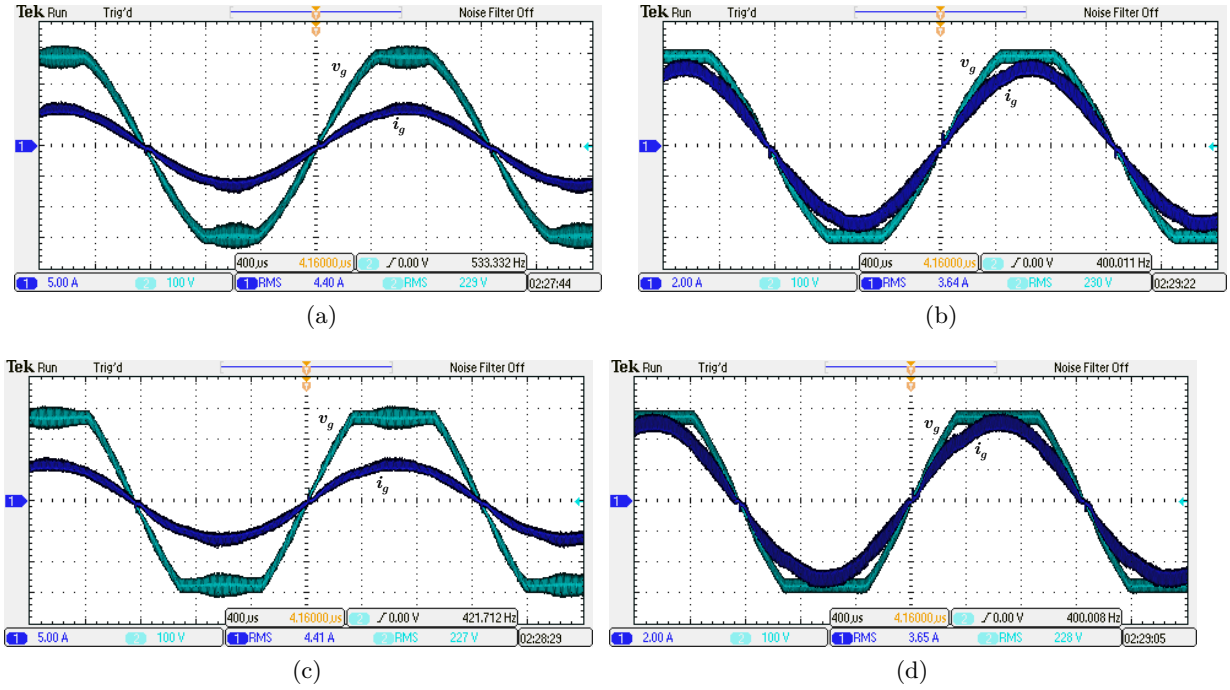


Figure 8.29: Pure sinusoidal behavior under different power levels and input voltage distortions. Input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$). $V_g = 230\,V$, $f_{sw} = 96\,kHz$. With $THDv$ =5 % at (a) P_g =964.9 W and (b) P_g =799.5 W. With $THDv$ =12 % at (c) P_g =963.1 W and (d) P_g =800.4 W.

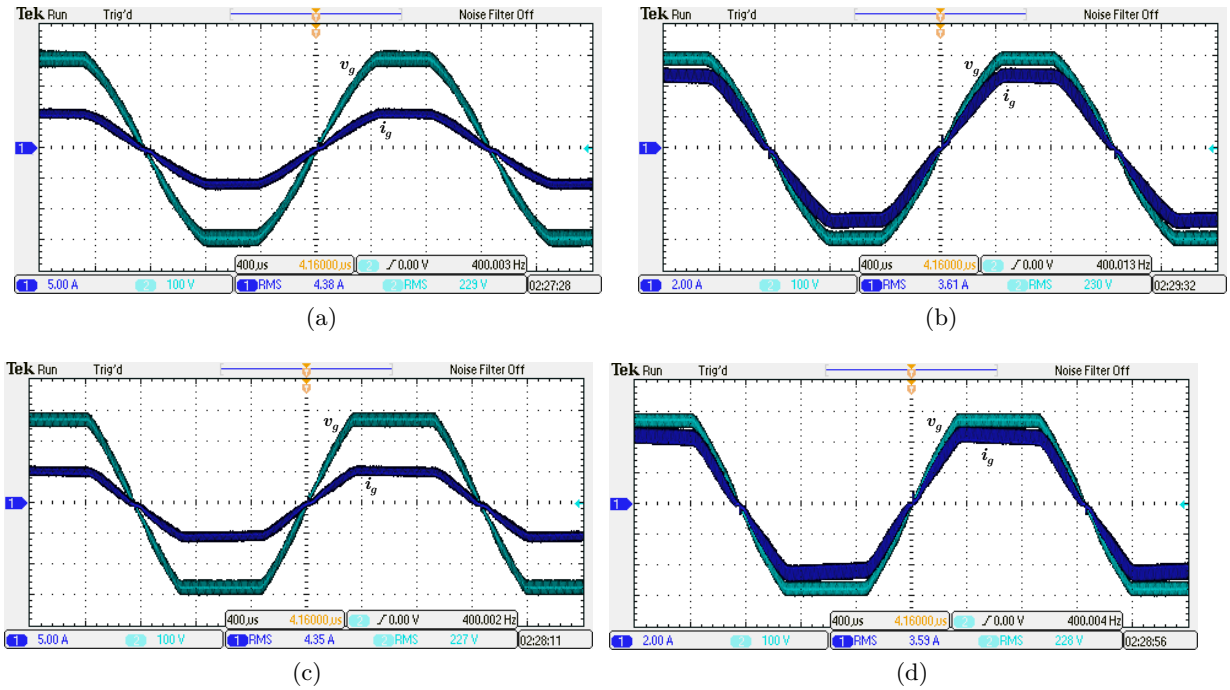


Figure 8.30: Resistance behavior under different power levels and input voltage distortions. Input voltage (v_g) and current (i_g) along with the DCM signal of the rebuilt input current ($DCMi_{reb}$) and the real input current ($DCMi_g$).$V_g = 230\,V$, $f_{sw} = 96\,kHz$. With $THDv$ =5 % at (a) P_g =966.7 W and (b) P_g =800.6 W. With $THDv$ =12 % at (c) P_g =965.1 W and (d) P_g =800.9 W.

8.5 Chapter conclusion

Experimental results under different situations are presented in this Chapter. Universal input voltage range at different power levels, for 72, 98 and 144 kHz has been presented. Power factor correction is achieved in all the cases despite not measuring the input current

One important aspect that must be emphasized is that despite the fact that the digital controller has not been modified in this experimental validation, the power factor correction is achieved in very different conditions (e.g. 230 V_{rms} - 50 Hz and 120 V_{rms} - 500 Hz), illustrating the "universality" of the proposed controller. This aspect is the most relevant contribution of this work, representing a step-forward in comparison with other works in the same topic, achieving the initial goal presented in Section 2.8.

It is important to remark the behavior of the proposed controller under high-frequency grids, used in airborne applications. Grid frequencies around 400 Hz are almost one order of magnitude higher than the typical 50-60 Hz grids, so the error accumulated every switching period over the half line cycle (for the same conditions and components) is divided by 10, leading to a lower current distortion (i.e. 3 mA of error per switching period, represents a current estimation error at the end of the switching period of 3 A in a 50 Hz grid, and 0.375 A in a 400 Hz grid).

Results under distorted grids, with the proposed pure sinusoidal current behavior are presented, and compared with the traditional resistance behavior. Current harmonics decrease with the proposal despite the fact that the power factor value also decreases. In this case, the user selects the desired behavior.

Chapter 9

Example of application: Digital PFC controllers for HID lamps electronic ballast applications

In this Chapter, the digital controller presented in this Thesis is used in an application controlling a Boost PFC rectifier connected to electronic ballasts for high intensity discharge (HID) lamps. Furthermore, in parallel with the control without current sensor, an additional performance derived from the potential capabilities of the digital controllers is included.

Low frequency utility voltage fluctuations cause a perceptible variation in the light emitted by lamps, unpleasant for the human eye and known as flicker effect. An novel control technique for PFC stages analyzes the input voltage, detects the fluctuations only in the range of human flicker sensitivity and modifies the parameters of the PFC output voltage controller to avoid the propagation of the utility fluctuations to the dc bus, and then to the ballast, eliminating the lamp light variation. The controller is implemented in a Field Programmable Gate Array (FPGA). A constant lamp luminance is achieved with this digital controller, with no dependence on the next ballast stage is needed.

9.1 Introduction

High Intensity Discharge (HID) lamps are of interest from a research and commercial point of view. Key properties include higher energy efficiency, compact size, good color rendering, whiter light (higher color temperature), and longer lifetime [164–169]. Typical applications range from car headlamps, greenhouse lighting, interior lighting, industrial sector and urban lighting applications. Since the urban lighting consumption represents a non-negligible part

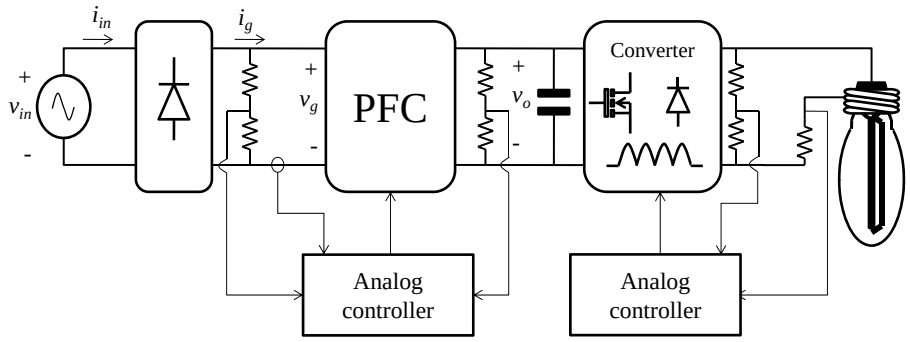


Figure 9.1: Two power stages ballast circuit with a analog PFC and inverter controllers.

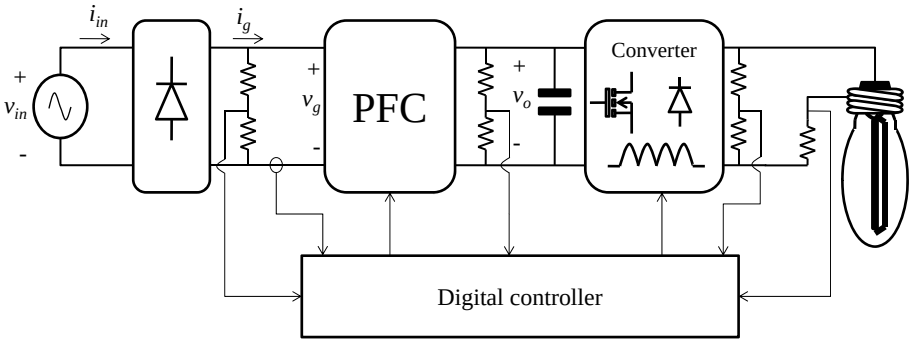


Figure 9.2: Two power stages ballast circuit with digital controllers integrated in a single device.

of the total energy amount consumed on Earth, improvements of the supply and efficiency are investigated.

To cope with all these challenges, designers can rely on more and more mature digital electronics technologies, which now come along with friendly software development tools. Nowadays, it is becoming more usually to find digital control in electronic ballast that provides higher performance [164–166]. In Fig. 9.1 a typical system of two power stages applies in electronic ballast is shown: power factor correction (PFC) [1] and inverter. On the other hand, in Fig. 9.2 the same system is depicted with a digital controller.

Light emitted by HID lamps is very sensitive to voltage supply fluctuations, producing an effect on the human visual perception, known as flicker [170–172]. Flicker is a very uncomfortable effect, which would cause a lot of human physiological effects; so it is addressed as a safety and health at work issue. These fluctuations can be caused by the connection and disconnection of important loads (high-power motors, PFC bank capacitors, etc...), compressors, resistive welding machines or arc furnaces. Flicker frequency can be perceived by the eye-brain set, when it is below a range of the frequencies that extends from 0.5 to 25 Hz [171]; and the maximum flicker perception is established at around 10 Hz.

In two-stage electronic ballast, where the inverter operates in open loop, the PFC outer loop and its output bulk capacitor, C, are the elements that attenuate the propagation of the utility voltage fluctuation to the dc bus and then contribute to reduce the light variation in HID lamps [171, 173, 174]. Increasing the PFC output capacitance is a simple solution to

reduce human flicker sensitivity. The output capacitor filters out the utility voltage fluctuations at the expense of increasing its size and weight. But the power supply manufacturers and research groups are looking for reducing this capacitance and even avoiding the use of electrolytic capacitors [66, 175, 176]. Lamp light variation is avoided in [169] with a wide bandwidth controller in the inverter stage. In [177], two control algorithms are presented for Distribution STATic synchronous COMpensator (DSTATCOM) for voltage fluctuation mitigation with electric arc furnace loads. Previous works like in [178] present a technique to monitor voltage fluctuations in the power system with a least-squares-Kalman optimization technique for fundamental frequency voltage phasor estimation. In [173], an input instantaneous voltage detection algorithm, under ideal utility mains, is presented. A previous version of the controller presented in this paper, appears in [174].

The proposed digital compensation of the voltage fluctuation does not modify the original PFC controller if input voltage low frequency fluctuations are not detected. When these fluctuations appear, the proposed controller changes the voltage loop dynamic response to minimize the dc voltage ripple at the fluctuation frequency assuring a constant light luminance in the lamp and avoiding the optical flicker perception. No extra cost and no extra analog components are introduced whenever the FPGA is large enough to include the additional digital block. To clearly show the performance achieved, a practical application with a 150 W HPS (High Pressure Sodium) lamp supplied by an open loop resonant inverter as second stage (Fig. 9.1 and Fig. 9.2) is presented.

The objectives of this Chapter are: 1) to use a digital sensorless controller technique for the PFC stage, presented in this Thesis, in a real ballast. 2) To develop a universal voltage fluctuation detection method that fits the standard definition human perception range. 3) To use the lowest PFC output capacitance C by extending the capabilities of the digital output voltage loop, and 4) to minimize the flicker perception for the human eye caused by the utility disturbances.

9.2 Outer voltage loop in the digital PFC controller

In steady-state operation, the PFC output voltage loop has a low bandwidth (around 10 Hz) so not to interfere with the inner loop that keeps the current shape proportional to the input voltage to comply with the IEC 61000-3-2 for class C equipment [1]. The action of the low bandwidth cannot reject the low-frequency fluctuations and they are propagated through the PFC and inverter stages, perturbing the lamp current and voltage, as is depicted in Fig. 9.3. The current fluctuation causes the lamp light variation, and then the flicker effect.

In order to attenuate this flicker effect, traditionally the capacitance of the output bulk capacitor (C) in the PFC stage is increased over the required to limit the amplitude of the voltage ripple at twice the line frequency. On the other hand, the electrolytic capacitor is a typical bottleneck to extend the useful life of the ballast system.

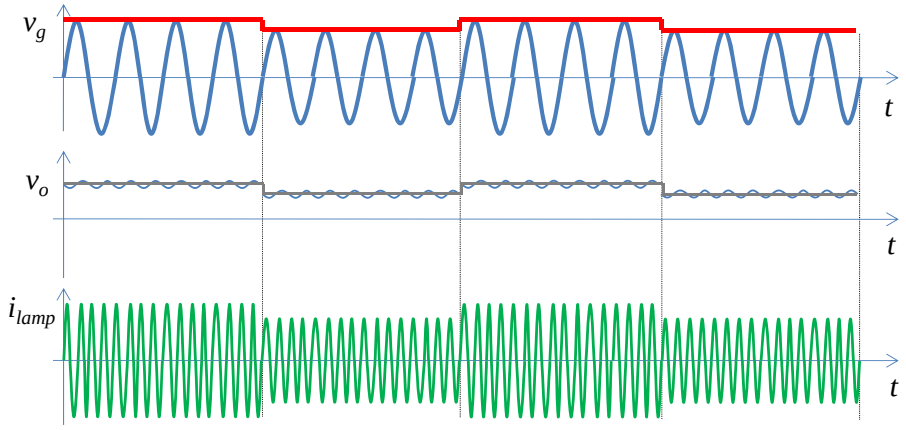
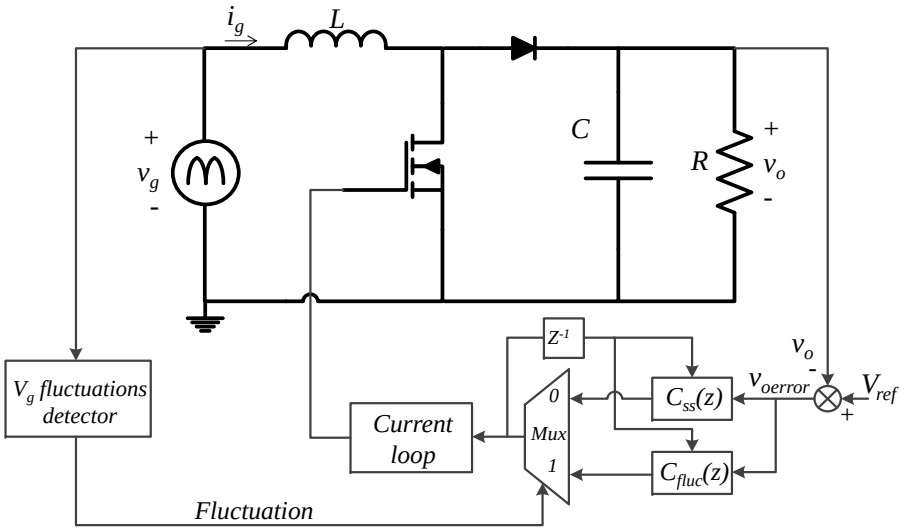
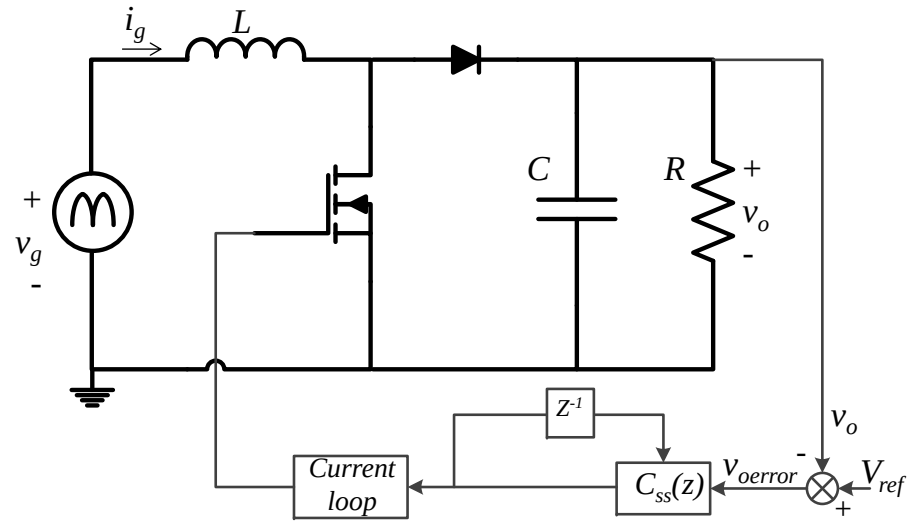


Figure 9.3: Waveforms under voltage fluctuations situation: Utility voltage, vg, PFC stage output voltage, v_o, and lamp current, i_{lamp}.



(a)



(b)

Figure 9.4: PFC stage and digital controller implementation. (a) Traditional digital voltage control loop. (b) Digital control loop proposed.

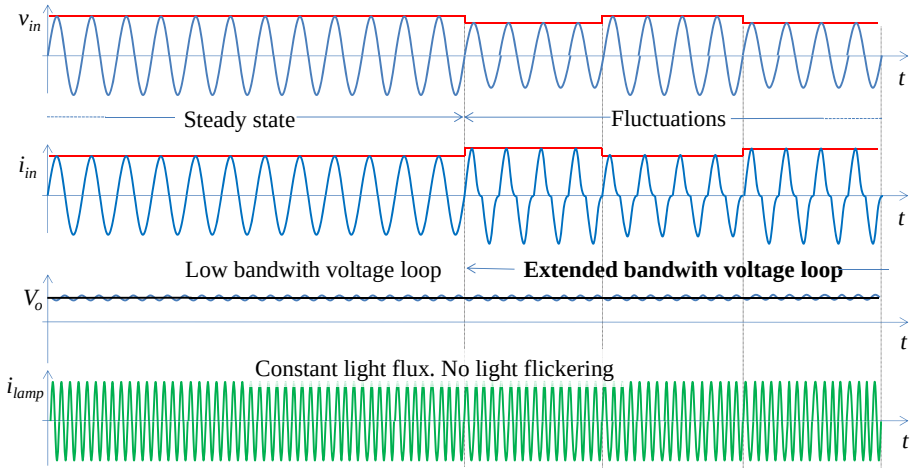


Figure 9.5: Sketches of the utility voltage, utility current, dc voltage and lamp current changing the voltage loop: Low bandwidth loop during steady state and extended bandwidth loop under utility voltage fluctuation.

A traditional digital voltage loop is shown in Fig. 9.4a, where a low bandwidth compensator, $C_{ss}(z)$ is implemented to assure that the output voltage that supplies the second stage follows the reference (V_{ref}). The block diagram of the proposed digital controller is presented in Fig. 9.4b. Under steady-state situation, without utility fluctuations, a low bandwidth compensator, $C_{ss}(z)$ is applied. When utility disturbances appear, an utility voltage fluctuations detector, that is presented in Section 9.3, activates the compensator $C_{fluc}(z)$ in order to extend the bandwidth of the PFC outer loop, avoiding their propagation to the lamp at the expense of increasing the utility current distortion. With this capability, a low C value can be utilized [173, 174].

Figure 9.5 shows the target behavior of the proposed control. During steady state, the output voltage loop has a low bandwidth and a current shape proportional to the input voltage and also has an extended bandwidth loop in the utility voltage fluctuations situation with current distortion. Standard IEC 61000-3-2 class C [1] is not applied in presence of these utility transients. A constant PFC stage output voltage (v_o) is achieved despite input voltage low frequency fluctuations. With this, constant lamp current (i_{lamp}), and then constant lamp light luminance are also achieved.

9.3 Input voltage fluctuations detection algorithm

A utility mains voltage distorted with a low-frequency fluctuation is shown in Fig. 9.6. Δv defines the depth and T_f the fluctuation period.

The value of utility peak voltage ($v_{g,peak}$) is obtained, cycle by cycle, with a digital peak detector of the digital input voltage value (v_g^*). With this value, the steady-state utility peak voltage is calculated and three different voltage ranges are defined as is shown in Fig. 9.7. The algorithm defines the non-fluctuation band (called "In" in Fig. 9.7), with the steady-state utility peak voltage, $v_{g,peak}$ $\pm 2\%$. When the utility peak voltage is outside this band, i.e.

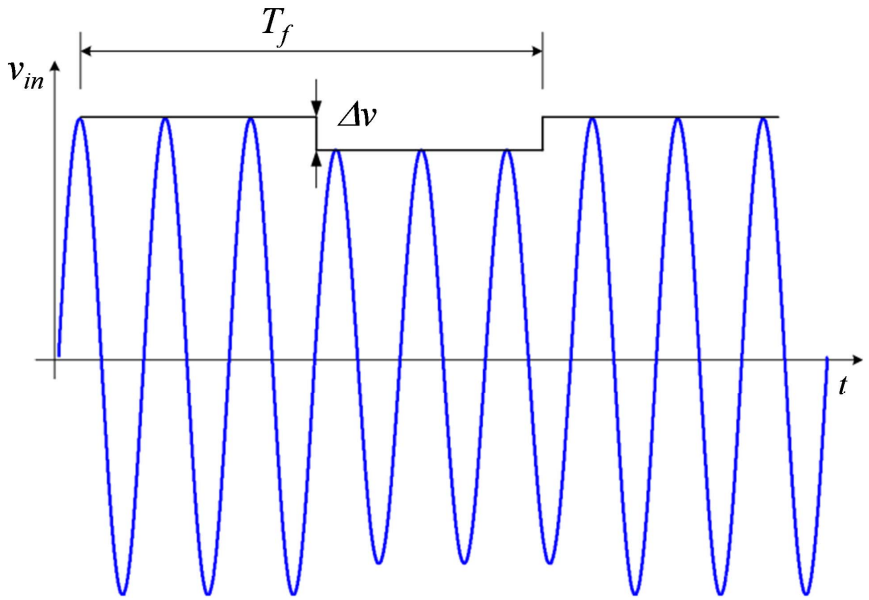


Figure 9.6: Low frequency voltage fluctuation.

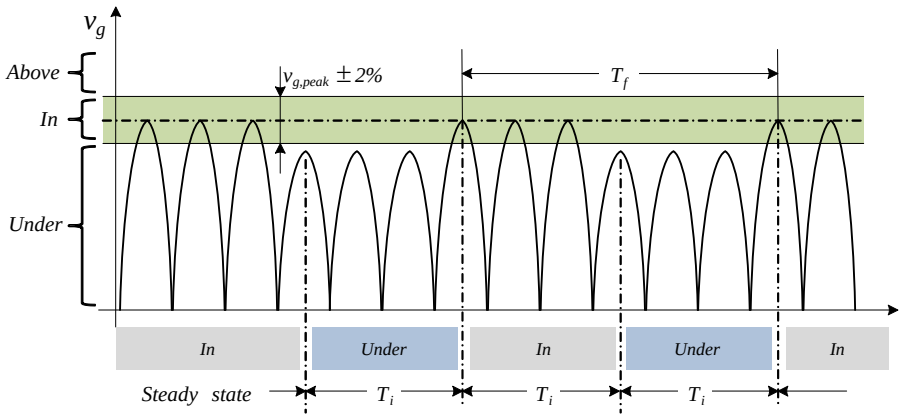


Figure 9.7: Voltage range defined to detect the utility voltage fluctuations.

"Above" or "Below" in Fig. 9.7, the algorithm determines whether there is a fluctuation in the most sensitive frequency range of the human eye, between 0.5 to 25 Hz. If the fluctuation has a period T_f, it can be approximated that $T_f/2$ is the time in each voltage band. When the first change in the peak value is detected, the algorithm measures the time (T_i) that the peak voltage is maintained in each band. If T_i is between 0.02 s and 1 s (half period of a 25 and 0.5 Hz fluctuation, respectively), it is considered that there is a utility voltage fluctuation. The precise fluctuation frequency is only measured if it is in the 0.5 to 25 Hz range where it produces an unpleasant optical flicker perception. The input voltage fluctuation detection algorithm flowchart is shown in Fig. 9.8. The signal "Fluctuation" is set to "1" under flicker situation, and therefore the time during the wide bandwidth voltage loop has to be applied ($T_{wide-loop}$) is determined.

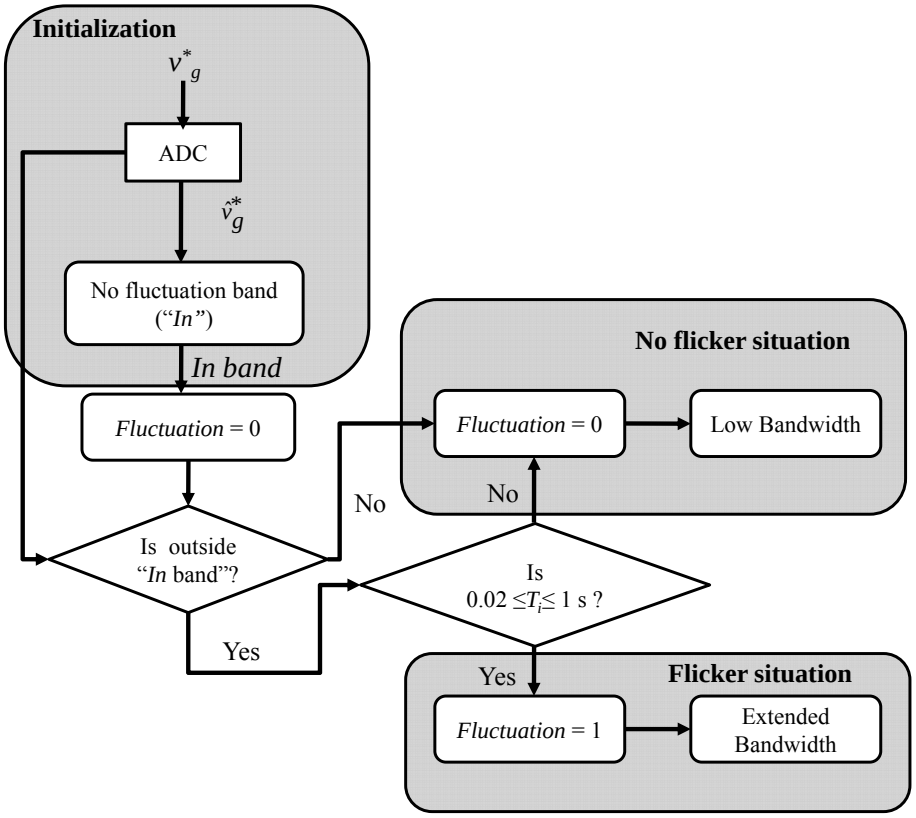


Figure 9.8: Input voltage fluctuation detection algorithm flowchart.

9.4 Experimental results

Laboratory experiments that illustrate the performance of the digital controller have been carried out with an electronic ballast for a 150 W HPS lamp (LUCALOX). Fig. 9.9 shows a block diagram of the laboratory test setup. A boost converter has been used as PFC stage. Values of the components are: L= 3.2 mH, V_{in} = 230 V (50 Hz), f_{sw} = 73 kHz, V_o = 420 V and P_o= 150 W. The value of the output bulk capacitor is 68 µF. A LCC half-bridge resonant inverter (RI) is used as second stage. It provides the required ballast action at reduced cost and behaves as an input voltage-dependent power source.

The LCC resonant circuit is designed to have zero resonant current phase lag at the end of the lamp lifetime, and it works in a frequency window free of acoustic resonance, which is a valid solution for 150 W HPS lamps [179]. This inverter operates in open loop, so it is a system without capability for compensation of input voltage disturbances, being a good example to illustrate the performance of the proposed digital controller. ZVS is guaranteed in the resonant inverter along with a minimum reactive component in the resonant tank considering the whole life span of the lamp. Using the design sequence described in [179], the RI design is defined by $Z_p = R_{lamp}/Q_p$= 170 Ω, L_r = 115 µH, C_p = 5.7 nF and C_s = 330 nF. In order to measure the behavior of the system with the proposed digital control, an APDS-9007 ambient light photo sensor is used. This photo sensor has a spectral response close to the standard photopic observer. The photo sensor is placed in front of the lamp to

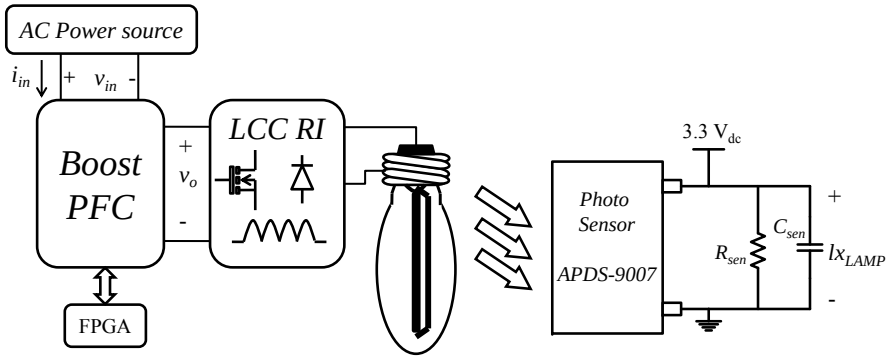


Figure 9.9: Block diagram of the laboratory test setup.

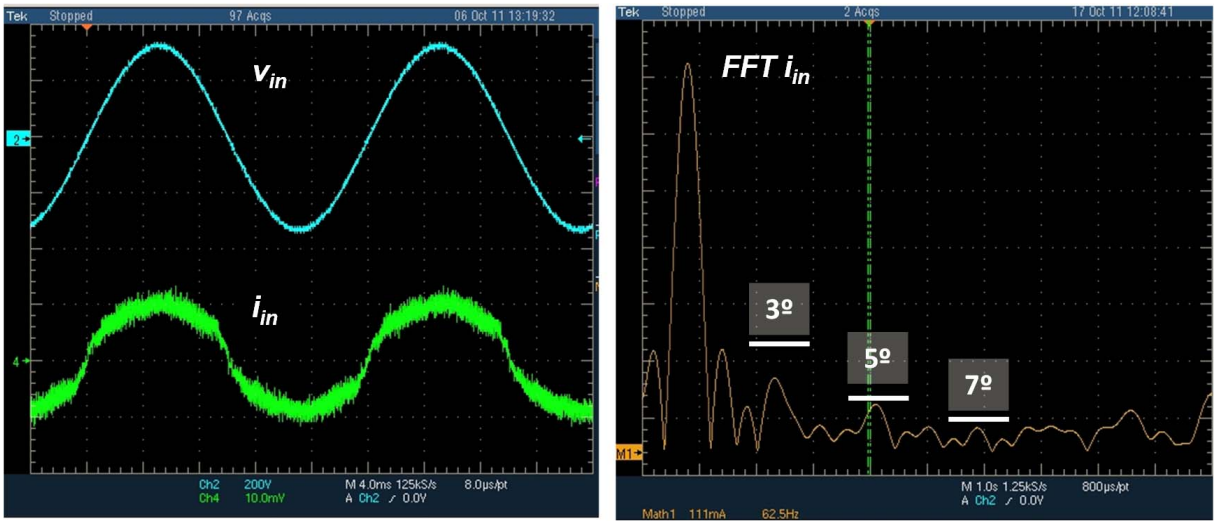


Figure 9.10: PFC stage input waveforms and power. Low bandwidth outer loop. (a) Input voltage v_{in}, and input current i_{in}. $V_{in} = 230\ V_{rms}$, 50 Hz. Ch2 input voltage, 200 V/div, Ch4 input current, 10 mV/A and 10 mV/div. (b) Input current Fast Fourier Transform (FFT i_{in}) and IEC 61000-3-2 class C limits with $I_1 = 0.680$ A and $PF = 0.991$. Math1. Vertical scale 111 mA/div, horizontal scale 62.5 Hz/div.

get an output voltage proportional to the brightness of the lamp light, according to what human eye perceives). This output voltage is called lx_{LAMP} (Fig. 9.9). An Agilent 6813B AC programmable power source is used to supply the HID lamp power supply.

Figure 9.10 shows the PFC stage input current (i_{in}) and the input voltage (v_{in}) waveforms in steady state situation. Despite not measuring the input current, power factor correction is successfully achieved. The value of the power factor measurement is 0.991 with an input power (P_g) of 168 W. Then, in Fig. 9.10 the Fast Fourier Transform (FFT) on the input current in comparison with the IEC 61000-3-2 class C limits is shown. In this case, all current harmonics are below the limits recommended by the standard. Figure 9.11 shows the PFC stage input current (i_{in}) and the input voltage (v_{in}) waveforms during utility fluctuation with the wide bandwidth outer loop. In this case, the value of the power factor is 0.91. The input current is distorted because of the faster dynamic response. In Fig. 9.11 it is shown how the harmonic content of the input current do not comply with the IEC 61000-3-2 class C limits. The phase margin and the crossover frequency are 73º and 0.61 Hz for the reduced bandwidth

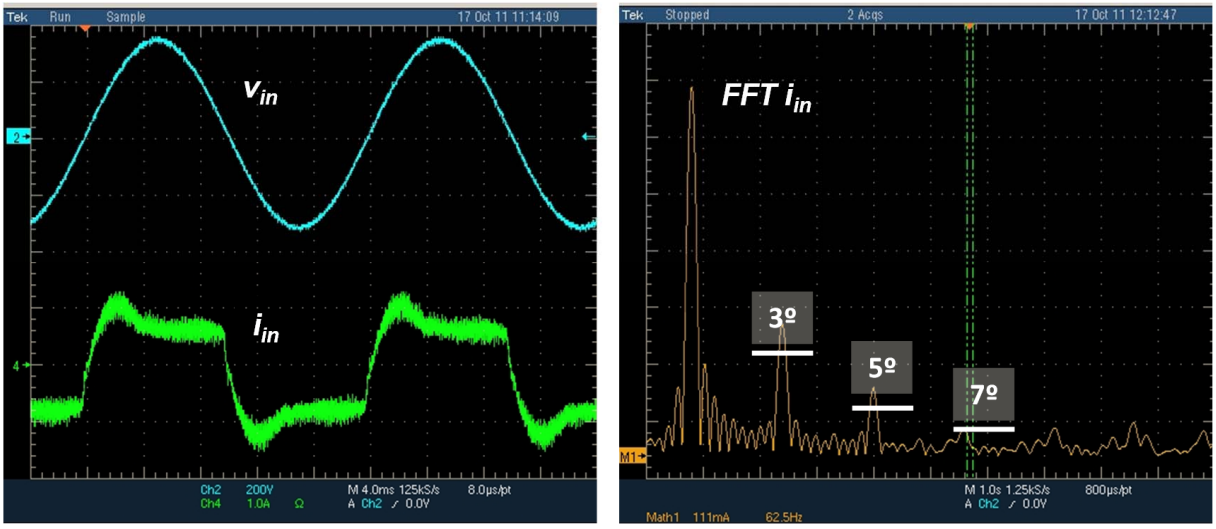


Figure 9.11: PFC stage input waveforms and power. Wide bandwidth outer loop. (a) Input voltage v_{in}, and input current i_{in}. V_{in} = 230 V_{rms}, 50 Hz. Ch2 input voltage, 200 V/div, Ch4 input current, 10 A/div. (b) Input current Fast Fourier Transform (FFT i_{in}) and IEC 61000-3-2 class C limits with I_1 = 0.680 A and PF = 0.91. Math1. Vertical scale 111 mA/div, horizontal scale 62.5 Hz/div.

voltage loop (9.10), and 78.8º and 149 Hz for the wide bandwidth loop (Fig. 9.11). Output voltage reference is the same for both controllers; in this case 420 Vdc. Fig. 9.12 shows the Bode diagrams of the extended bandwidth (blue) and the reduced bandwidth (green) outer loops.

The PFC stage dc output voltage (v_o), the lamp light lux level measured by the photo sensor (lx_{LAMP}) and the input voltage (v_{in}) to the PFC stage under a 10% fluctuation (ΔV) in the input voltage (programmed in the AC power source) are shown in Fig. 9.13a when the PFC uses the slow PFC outer loop and in Fig. 9.13b when the PFC uses the fast PFC outer loop to compensate the fluctuation. Fluctuation frequency has been set close to the maximum level of human eye flicker perception, i.e. 10 Hz. Figures 9.13a and 9.13b shows the same input voltage and the differences on lx_{LAMP} and v_o waveforms between applying or not the extended bandwidth outer loop. In Fig. 9.13a, the lx_{LAMP} signal has a fluctuation of 10 Hz (added to the output voltage 100 Hz fluctuation, imperceptible by the human eye). On the other hand, in Fig. 9.13b this fluctuation is highly attenuated, because the wide bandwidth voltage loop is applied. In this case, lamp light variation and flicker perception disappear. Figures 9.14 and 9.15 show the behavior of the input voltage fluctuation detection algorithm. Figure 9.14 shows the signal "Fluctuation" under different utility voltage conditions. At first, a 230 V_{rms} (325 V peak) utility voltage is applied. After 27 seconds, a step down of 30 V_{rms} is applied; and then, after 30 seconds, 210 V_{rms} (297 V peak) input voltage is applied. In this situation, a 10 % and 10 Hz fluctuation is imposed (210 – 189 V_{rms}). The algorithm determinates the steady-state peak voltage and defines the ±2% "In" band. When the fluctuation is detected, the signal "Fluctuation" turns to "1". The extended bandwidth voltage loop is applied during the time $T_{wide-loop}$.

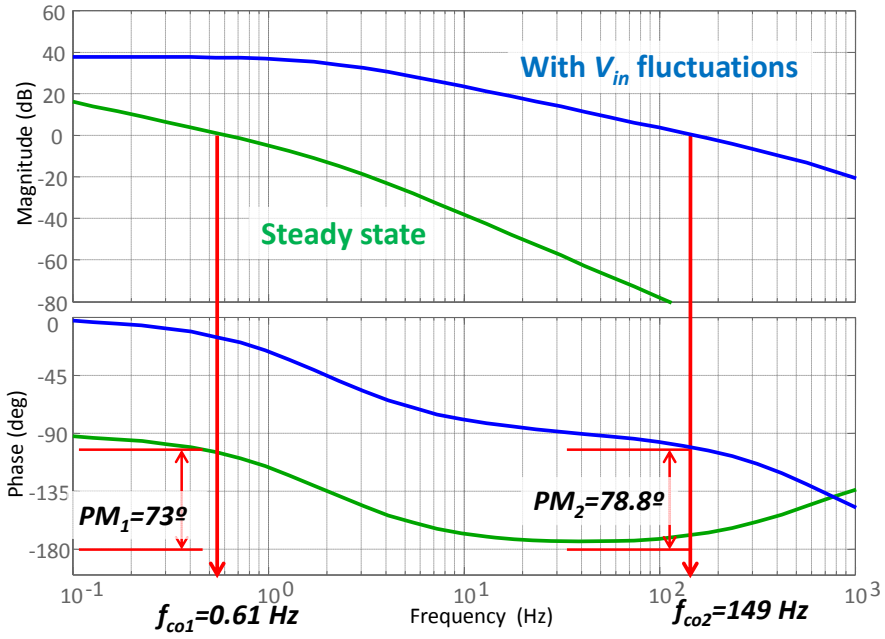


Figure 9.12: Bode plots for the different voltage loops. Green: Bode plot for steady-state conditions with reduced bandwidth. Blue: Bode plot for transient state during input voltage fluctuation with wide bandwidth.

Figure 9.15 shows the result of the algorithm behavior at the end of the fluctuation. It can be seen that a period of 1 second is necessary to determinate that the fluctuation has finished. The experimental prototype of the PFC boost converter and the control circuit used to verify the proposal. One of the HPS lamp used in the experimental results is shown in Fig. 9.16.

9.5 Chapter conclusion

A digital controller for power factor correction applied to HID lamp electronic ballast has been proposed. This controller, implemented in a FPGA, achieves a power factor correction according to the IEC 61000-3-2 class C limits and rejects input voltage disturbances to avoid the flicker effect. Any current sensor is needed to determine the input ballast current and achieve a sinusoidal current shape. This current is estimated from input and output PFC stage voltages measurements. Avoiding the current measurement can be a significant advantage with respect to analog controllers. A voltage fluctuations detection algorithm is used to avoid the fluctuations propagation to the lamp. The algorithm measures the steady-state utility peak voltage and detects low frequency voltage fluctuations in the most sensitive frequency range of the human eye. The digital controller changes the PFC stage voltage loop speed depending of the disturbances detected, reducing the optical flicker perception. The proposed digital controller is a valid solution although higher bandwidth (149 Hz) voltage loop distorts the input current. This is acceptable under transient conditions. A two stage ballast system (Boost PFC + Resonant Inverter) that supplies a 150 W HPS lamp has been subjected to low frequency utility fluctuations. These fluctuations have been programmed with an AC

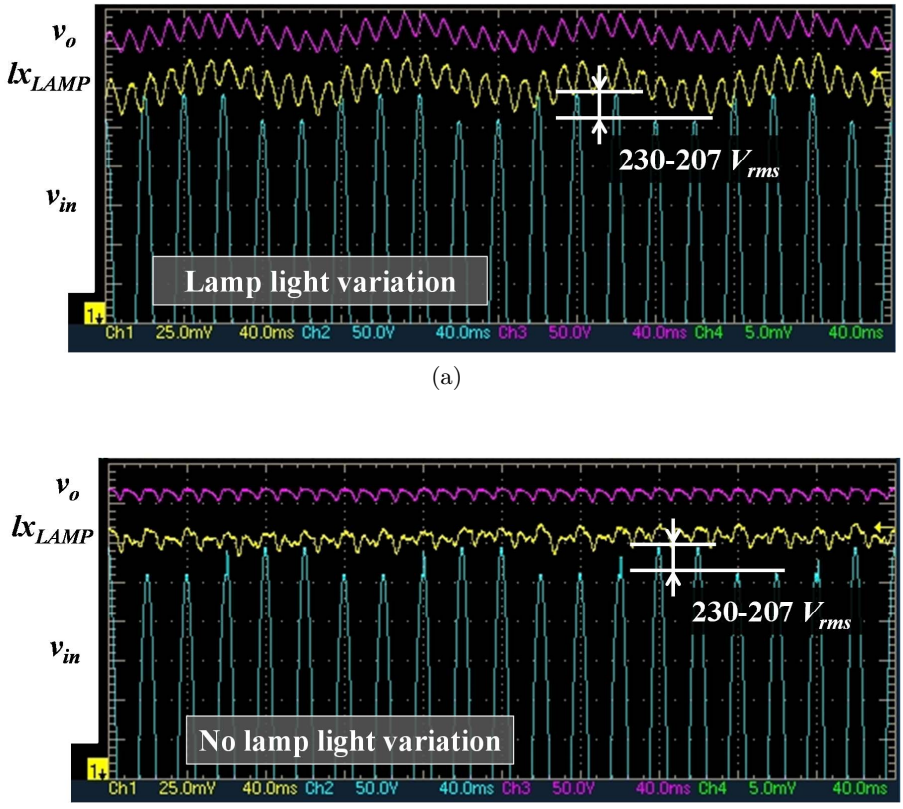


Figure 9.13: The PFC stage output voltage (v_o), the lamp light lux level measured by the photo sensor (lx_{LAMP}) and input voltage (v_{in}) under 10% V_{inRMS} and 10 Hz fluctuation. V_{in} = 230–207 V_{rms}, 50Hz, V_o = 420 Vdc, P_g = 150 W and C=68 µF output capacitor. (a) With a reduced voltage loop bandwidth and (b) With a wide voltage loop bandwidth. Ch2 input voltage, 50 V/div, Ch1 lamp light flux. Ch3 output voltage 50 V/div. Time scale: 40 ms/div.

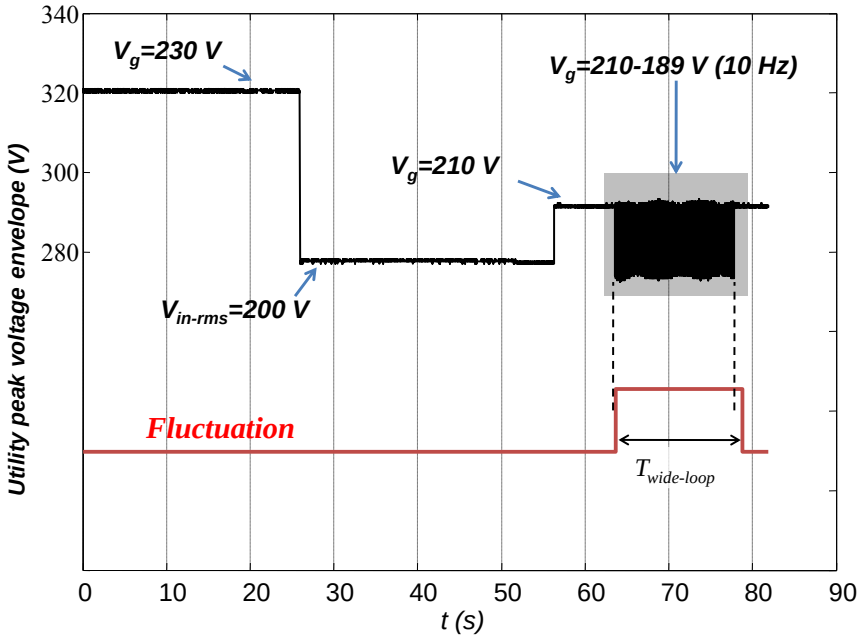


Figure 9.14: Behavior of the input voltage fluctuation algorithm under different utility voltage conditions. Utility peak voltage envelope (blue) and "Fluctuation" signal that indicates if a fluctuation is detected (red).

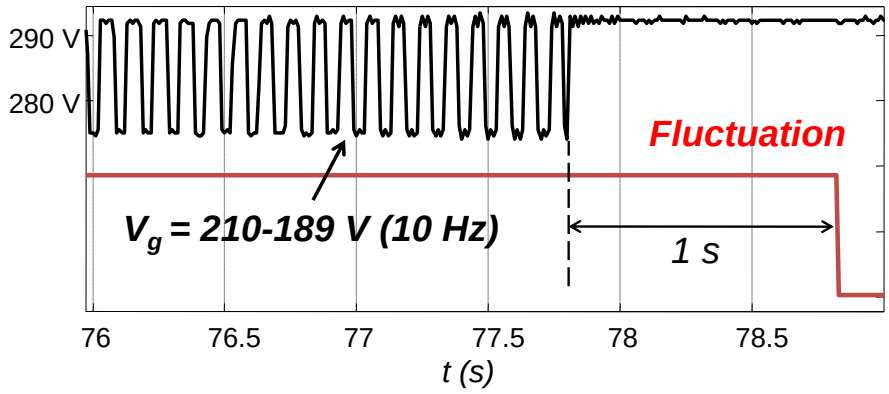


Figure 9.15: Time necessary by the algorithm to determinate the steady state condition at the end of the utility voltage fluctuation.

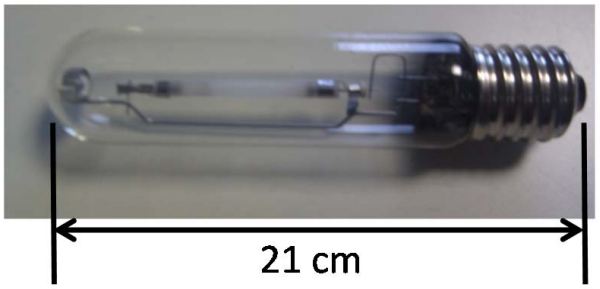


Figure 9.16: Lucalox 150 W HPS lamp used to verify the proposal.

power electronic source in order to produce a light variation close to the maximum level of human eye flicker perception, emulating an industrial environment under grid disturbances. A constant light luminance in the lamp is achieved despite frequency utility mains fluctuations and without extra analog components. Moreover, the size of the PFC output capacitor is reduced, decreasing the volume and cost, and increasing the lifetime of the converter.

Chapter 10

Conclusions

A universal current sensorless controller for Boost PFC stages operating in CCM has been presented in this Thesis. The input current is digitally rebuilt in a digital device, and is used in the PFC current loop, substituting the traditional current measurement in the PFC rectifiers. Making the most of the digital control capabilities, this traditional current sensing analog circuit is substituted by a simpler circuit (two resistor dividers and a comparator) which detects DCM condition in the input current by translating the pulsated drain-to-source voltage into a digital signal. With this circuit, an indirect measurement of the current distortion is obtained by comparing the actual DCM time in the converter, and the DCM time in the digitally rebuilt input current.

The effect of the different causes of error in the input current estimation for sensorless PFC Boost digital controllers operating in CCM has been analyzed. In this case, the current estimation is carried out by measuring the input, output and MOSFET drain-to-source voltages. The error between the estimated and actual DCM periods close to the zero crossing of the input voltage is a key variable to accurately correct the error in the estimation of the input current and the consequent distortion.

An auxiliary circuit detects indirectly DCM condition in the input current comparing drain-to-source voltage with the output voltage during the MOSFET OFF-time. The single digital signal acquired from the MOSFET drain-to-source voltage drop is used by both, the feedforward and feedback compensator.

The feedforward one represents a coarse compensation of current estimation errors due to time delays. And the new DCM time feedback loop generates a constant digital signal to compensate current estimation errors, modifying the output voltage measurement used to estimate the input current, and minimizes this DCM time error. This feedback loop sets the value of the digital signal when the converter operates in a wide load or voltage range with a high resolution.

With this approach, an universal Boost PFC digital controller is achieved without current measurement, so in the point of view of the designer the complexity of the PFC controller decreases. With this feedback loop, parasitic element values do not need to be measured, and are compensated for automatically, representing a step-forward in comparison with the previous works about sensorless PFC controllers. Experimental results show a boost PFC converter under different load and input voltage conditions achieving high power factor with reliable performance.

10.1 Summary of contributions

(1) Use of a digital estimation of the input current in a Boost PFC Stage in CCM in the inner current loop:

In a common approach, digital Boost PFC controllers sense the input/inductor current to control it, and assure a current shape proportional to the input voltage. Recent developments of Sensorless PFC controllers for Boost converters uses a stored duty cycle command to control the input current, or present new control approaches. Although the estimation of the inductor current is a well-known technique for DC-DC converters, in this work it is used in the PFC inner loop to control the input current.

(2) Study of the current estimation errors due to different causes:

Small errors in the measurement of the variables used in the current estimation cause a current estimation error every switching period, accumulated over the half line cycle. All the sinks of error are studied deeply, and modeled by different mathematical expressions in this Thesis. This aspect is important to evaluate the waveshape of the current error, that cause the input current distortion and low power factor value.

(3) Feedforward compensation of the switching signal delays:

One cause of the estimation error is the mismatch between the $on - off$ signal duty cycle generated by the NLC control applied to the rebuilt current which drives the MOSFET, and the effective duty cycle in the boost inductor due to the switching delays. These delays are measured with the digital circuit every switching period and used to compensate the PFC controller. The resolution of this compensation is limited by clock period of the digital device, resulting in a coarse fast compensation that not assuring the total compensation of the current estimation error originated by the switching delay.

(4) Auxiliary circuit to detect the DCM in the Boost converter measuring the drain-to-source voltage:

The difference between the DCM time of the actual current in the boost converter an the DCM time in the digitally estimated current is caused due to the input current distortion. So it represents a indirect measurement of the current estimation error. To detect the DCM in the boost converter without current sensor a new circuit that compares the drain-to-source voltage with the output voltage during the OFF-state has been presented.

(5) DCM time feedback high resolution compensation of the current distortion:

In parallel with the feedforward compensation, the mismatch between the DCM time of the actual and the estimated current is compensated by a slow feedback loop that assures near zero current estimation accumulated error at the end of the half line cycle with high resolution. This resolution is obtained in the digital device, i. e. no extra analog components are needed. A DC and AC small signal analysis is this feedback loop has been presented, defining the limits of stability. This DCM time feedback loop is slower that the output voltage loop.

(6) Low THDi demanded power under grid distortion:

Added to the sensorless approach, an additional functionality is presented in this work. A modification in the nonlinear-carrier controller, used in this work, is presented in Chapter 7 to demand a sinusoidal input current despite the input voltage distortion. With this controller used to control front-end stages, the system does not contribute in the voltage distortion. In application in which the requirements of current harmonics are critical, this approach fulfill them under distorted grids. This is not possible with the traditional PFC controllers with a resistance emulator behavior.

10.2 Future works

The most attractive work line is the possibility of develop a commercial integrated circuit with the ideas and approaches presented in this Thesis. In the point of view of the research, the future works lines that would be interesting to follow, after the work done during this Thesis, are:

- To extend the Sensorless PFC controller with current rebuilding to another converter topologies. One of the most interesting is the SEPIC converter, in which high power can be managed with an output voltage lower than the input voltage.
- To extend the digital controller to bridgeless or bidirectional Boost PFC rectifiers, in which the input diode rectifier is substituted by different individual switches.

- To modify the sensorless approach to three-phase systems.
- To extend the low THDi controller to Up-Down topologies, with or without current sensing.
- To extend the approach to 3 phase bidirectional rectifiers and converters.

In all of these ideas and future application, one of the mainstream aspects that must be consider is the modification of the DCM time feedback loop. The DCM condition is different depending on the converter topology.

Chapter 11

Published papers

11.1 Journals

- Miguel Rodríguez, **Víctor M. López**, Francisco J. Azcondo, Javier Sebastián, Dragan Maksimovic, *"Average Inductor Current Sensor for Digitally Controlled Switched-Mode Power Supplies*," in IEEE Transactions on Power Electronics, vol. 27, no. 8, pp. 3795-3896, Aug. 2012.

- Francisco J. Azcondo, Ángel De Castro, **Víctor M. López**, Óscar Garcia, "*Power Factor Correction Without Current Sensor Based on Digital Current Rebuilding*," in IEEE Transactions on Power Electronics, vol. 25, no. 6, pp. 1527-1536, Jun. 2010.

- Alberto Sánchez, Ángel de Castro, **Víctor M. López**, Francisco J. Azcondo, Javier Garrido, *"Single ADC Digital PFC Controller using Pre-calculated Duty Cycles,*" in IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 996-1005, Feb. 2014.

- **Víctor M. López**, Francisco J. Azcondo, Ángel De Castro, Regan Zane, "*Universal digital controller for Boost CCM power factor correction stages based on current rebuilding concept*," in IEEE Transactions on Power Electronics, *IEEE Early Access Articles.*

11.1.1 In review

- F. Javier Diaz, **Víctor M. López**, Francisco J. Azcondo, "*Digital PFC controllers for HID lamps electronic ballast applications*," in IET Power Electronics. *Minor revision.*

11.2 International Conferences

- **Víctor M. López**, Francisco J. Azcondo, Ángel De Castro, *"Current error compensation for current-sensorless power factor corrector stage in continuous conduction mode*," in

IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL), pp. 1-8, Kyoto, Japan, June 2012.

- F. Javier Díaz, **Víctor M. López**, Francisco J. Azcondo, Rosario Casanueva, Christian Brañas, *"Anti-flicker digital PFC controller for HID lamp electronic ballast*," in 37th Annual Conference on IEEE Industrial Electronics Society (IECON), pp. 2901-2906, Melbourne, VIC, Australia, Nov. 2011.

- F. Javier Díaz, **Víctor M. López**, Francisco J. Azcondo, Rosario Casanueva, Christian Brañas, *"New specification for the PFC controller in HID lamps electronic ballast,"* in 36th Annual Conference on IEEE Industrial Electronics Society (IECON), pp. 2595-2600, Glendale, AZ, USA, Nov. 2010.

- **Víctor M. López**, Francisco J. Azcondo, Ángel De Castro, "*High-resolution error compensation in continuous conduction mode power factor correction stage without current sensor*," in 15th International Power Electronics and Motion Control Conference (EPE/PEMC), pp. LS3c.2-1 - LS3c.2-8, Novi Sad, Serbia, Sept. 2012.

- **Víctor M. López**, Francisco J. Azcondo, Ángel De Castro, "*Autotuning digital controller for current sensorless power factor corrector stage in continuous conduction mode*," in IEEE 12th Workshop on Control and Modeling for Power Electronics (COMPEL), pp. 1-8, Bouder, CO, USA, June 2010.

- **Víctor M. López**, Francisco J. Azcondo, "*Low THDi front-end stage under non-sinusoidal voltage*," in IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL), pp. 1-6, Salt Lake City, UT, USA, June 2013.

- **Víctor M. López**, Francisco J. Azcondo, "*Modeling of a High resolution DCM times feedback loop for Sensorless Boost PFC stages,*" in IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL), pp. 1-8, Salt Lake City, UT, USA, June 2013.

- **Víctor M. López**, F. Javier Díaz, Francisco J. Azcondo, Ángel De Castro, "*Current Sensorless SEPIC PFC Stage for HID Lamps Ballast with Lamp Control Performances*," in International Exhibition & Conference for Power Electronics, Intelligent Motion and Power Quality (PCIM), pp. 1115-1131, Nuremberg, Germany, May 2011.

- **Víctor M. López**, F. Javier Díaz, Francisco J. Azcondo, Ángel De Castro, "*Current sensorless power factor corrector applied to electronic ballast for HID lamps*," in International Exhibition & Conference for Power Electronics, Intelligent Motion and Power Quality (PCIM), pp. 1184-1190, Nuremberg, Germany, May 2010.

11.3 Spanish Conferences

- **Víctor M. López**, Francisco J. Azcondo, Ángel De Castro, "*Corrección de Factor de Potencia basado en Estimación Digital de la Intensidad de Entrada,*" in Seminario Anual de Automática y Electrónica Industrial e Instrumentación (SAAEI), Bilbao, Spain, July 2010.

- **Víctor M. López**, Francisco J. Azcondo, F. Javier Díaz, "*Nuevas especificaciones para el controlador CFP utilizado en balastos electrónicos para lámparas de alta intensidad de descarga,*" in Seminario Anual de Automática y Electrónica Industrial e Instrumentación (SAAEI), Badajoz, Spain, July 2011.

- **Víctor M. López**, Francisco J. Azcondo, A. de Castro, Regan Zane, "*Controlador de CFP Universal para Boost en MCC sin sensado de corriente,*" in Seminario Anual de Automática y Electrónica Industrial e Instrumentación (SAAEI), Madrid, Spain, July 2013.

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[2] K. K. Sum, "Valley-fill power factor correction circuit," United States of America Patent 6,141,230, Oct. 31, 2000, 2000.

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Appendix A

Definition of the rebuilt input current RMS value I_{reb}

This appendix shows the procedure to set the value of α used in Chapter 6. It has been addressed in that Chapter, that this parameter α is used to define the linear relation between the RMS values of i_g, i_{reb} and the current estimation error i_{error}.

A.1 Linearization of the expression

The instantaneous value of the input current i_g, has been defined as:

$$i_g = i_{reb} + i_{error} \tag{A.1}$$

where i_{reb} and i_{error} are the rebuilt current used in the current loop and the current estimation error, defined by

$$i_{reb} = I_{reb}\sqrt{2}sin\left(\omega t\right) \tag{A.2}$$

and (6.5), that is copy in (A.3),

$$i_{error} = \xi\left(qv_{dig} - V_{\beta}\right)\left[1 - cos\left(\omega t\right)\right] \tag{A.3}$$

respectively. Defining $M_g = V_{g,peak}/V_o$ and $K = 2Lf_{sw}/R$, then ξ represents a constant value under a given operation conditions, defined by (6.6) as

$$\xi = \frac{M_g f_{sw}}{\pi K R f_u} \tag{A.4}$$

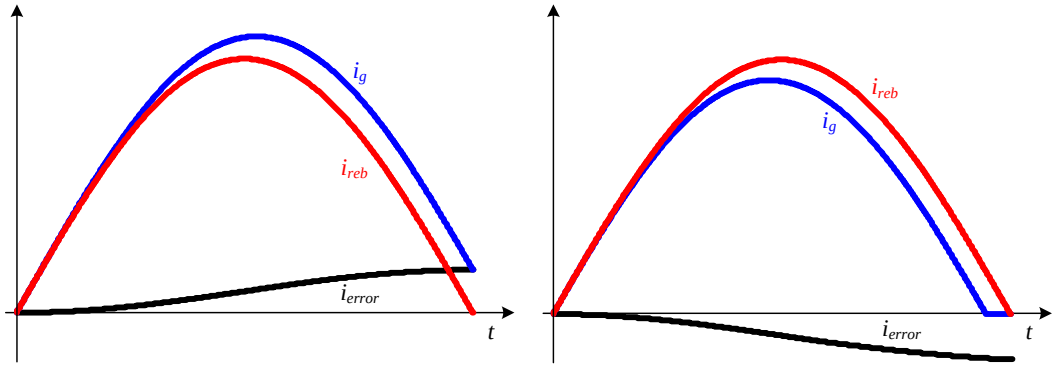

Figure A.1: System waveforms for a given I_{reb} and $qv_{dig} - V_\beta$ values. Left: $qv_{dig} > V_\beta$ and right: $qv_{dig} < V_\beta$.

and V_β is defined by (4.25)

$$V_\beta = \frac{V_{ref}\left(R_{on} + R_L\right) + V_D R_e - V_g\left(R_{on} - R_D\right)}{R_e - \left(R_{on} + R_L\right)} \tag{A.5}$$

To model the system, it is needed to define the portion of the half line cycle in with i_g is operating in the DCM. As it has been mentioned in Chapter 6. From the power balance of the large signal model, the RMS value of the real current I_g, is given by:

$$I_g = \frac{V_o^2}{RV_g} \tag{A.6}$$

So the RMS value of the real current is known, being unknown the instantaneous value of i_g, and the RMS value of rebuilt input current I_{reb}. The variable needed to develop the model presented in Chapter 6 is I_{reb}. Computing the RMS values of i_g, according to (A.1):

$$I_g = \frac{V_o^2}{RV_g} = \sqrt{\frac{1}{T_u}\int_0^{T_u} \left(i_{reb} + i_{error}\right)^2 dt} \tag{A.7}$$

Substituting (A.2) and (A.3), in (A.7):

$$\frac{V_o^2}{RV_g} = \sqrt{\frac{1}{T_u}\int_0^{T_u} \left[I_{reb}\sqrt{2}sin\left(\omega t\right) + \xi\left(qv_{dig} - V_\beta\right)\left[1 - cos\left(\omega t\right)\right]\right]^2 dt} \tag{A.8}$$

Computing and linearizing this expression to obtain the value of I_{reb} is not practical and useful. To obtain a linear approximation of I_{reb} as a function of the known values I_g and $\xi\left(qv_{dig} - V_\beta\right)$, the Curve Fitting Toolbox [180] has been used. To do that, a sinusoidal i_{reb} waveform is created for several values of I_{reb}, according to (A.2). And different i_{error} waveforms are added to i_{reb}, for different values of qv_{dig} obtaining the corresponding i_g waveform. Two different examples are plotted in Fig. (A.1). With a positive i_{error} (obtained with $qv_{dig} > V_\beta$), the real input current is higher than i_{reb}, and vice-verse. It must be considered, that i_g can not be negative, so in the case $i_{error} > i_{reb}$, i_g keeps zero value (i.e. DCM condition).

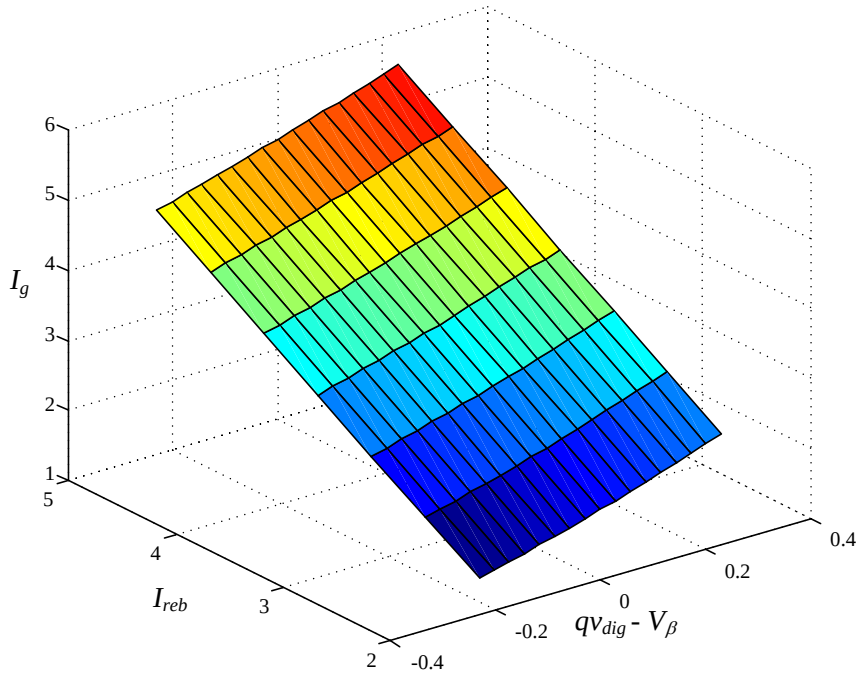

Figure A.2: Surface of I_g values obtained for different combinations of given I_{reb} and $qv_{dig} - V_\beta$ values.

Figure A.2 plots the surface of the different I_g values obtained under several I_{reb} and $qv_{dig} - V_\beta$ combination values. In this case $I_{reb} \epsilon [2, 5]$ and $qv_{dig} - V_\beta \epsilon [-0.3, 0.3]$, and it can be seen how the surface is similar to a plane, approximated as:

$$I_g = \gamma I_{reb} + \alpha\xi \left(qv_{dig} - V_\beta\right) \tag{A.9}$$

being γ and α the coefficient of the expression that defined mentioned plane. With this I_{reb} and $qv_{dig} - V_\beta$ values vectors are inputs in the Curve fitting toolbox, which sets the values of the coefficients as: $\gamma = 1$ and $\alpha = 0.9$. Figure (A.3) compare the I_g values obtained by the real converter and defined by (A.7), and its linear approximation defined by (A.9), labeled by $I_{g,lin}$ in the figure, for the values of $I_{reb} \epsilon [2, 5]$ and $qv_{dig} - V_\beta \epsilon [-0.3, 0.3]$ presented previously. It can been seen the good agreement between the two curves around the operation point ($qv_{dig} - V_\beta = 0$). According to that, for a demanded power level $P_o = V_o^2/R$, a RMS value of the input voltage V_g, and the v_{dig} value given by the DCM time feedback controller it yields with the I_{reb} value:

$$I_{reb} = I_g - 0.9\xi \left(qv_{dig} - V_\beta\right) = \frac{V_o^2}{RV_g} - \xi \left(qv_{dig} - V_\beta\right) \tag{A.10}$$

that corresponds with the expression (6.11), used in Chapter (6), to model the system.

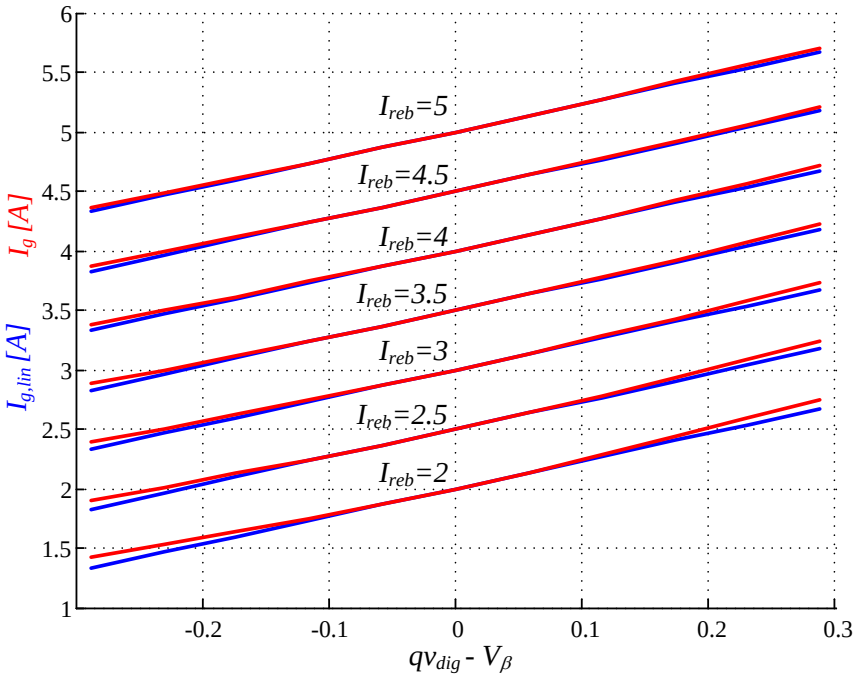

Figure A.3: Comparison of I_g values obtained by (A.7) (represented in red), and by the linear approximation defined by (A.9), labeled as $I_{g,lin}$ and plotted in blue.