4–12- and 25–34-GHz Cryogenic mHEMT MMIC Low-Noise Amplifiers

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***Abstract*—In this paper, monolithic microwave integrated circuit (MMIC) broadband low-noise amplifiers (LNAs) for cryogenic applications based on a 100-nm metamorphic high-electron mobility transistor (mHEMT) technology in combination with grounded coplanar waveguide are reported. A three-stage LNA, operating in 4–12 GHz and cooled to 15 K exhibits an associated gain of 31.5 dB ± 1.8 dB and average noise temperature of 5.3 K ($\mathrm{NF} = 0.079$ dB) with a low power dissipation of 8 mW. Additionally another three-stage LNA 25–34 GHz cooled to 15 K has demonstrated a flat gain of 24.2 dB ± 0.4 dB with 15.2 K ($\mathrm{NF} = 0.22$ dB), average noise temperature, with a very low power dissipation of 2.8 mW on chip. The mHEMT-based LNA MMICs have demonstrated excellent noise characteristics at cryogenic temperatures for their use in radio-astronomy applications.**

***Index Terms*—Cryogenic low-noise amplifier (LNA), metamorphic high electron-mobility transistor (mHEMT), monolithic microwave integrated circuit (MMIC).**

I. Introduction

A NEW generation of focal plane arrays, with a large number of pixels, enhance the mapping efficiency of some of the existent radio telescopes. This need of a large number of receivers has been the initial motivation for the development of monolithic microwave integrated circuits (MMICs) especially designed to obtain good cryogenic performance. Cryogenic low-noise amplifiers (LNAs) working at 4–15-K ambient temperature are the key component in the front-ends of all those ultra-low-noise cryogenic receivers used for radio astronomy and deep-space communications. For such a large number of LNAs, MMICs enable simple, small size, and low-cost production. These LNAs should be designed to obtain the lowest possible noise. Moreover, some of the radio-astronomy applications also require a very wide instantaneous bandwidth in order to increase the sensitivity of continuum observations. In that case, gain fluctuations of the amplifier may play a role since they can degrade the sensitivity.

To date, InP pseudomorphic high electron-mobility (pHEMT) MMIC LNAs have demonstrated outstanding noise at cryogenic temperatures [1]–[6]. However, recently metamorphic high electron-mobility transistor (mHEMT)-based LNAs have also been reported with good performances [7]–[10]. The advantages of mHEMT technology are lower costs, better robustness, and availability of larger GaAs wafers for production compared to InP substrate materials. The potential of the 100-nm mHEMT technology for MMIC applications at cryogenic temperatures is evaluated in this paper. We report the results obtained in two designs for the 4–12- and 25–34-GHz bands.

The 4–12-GHz band is of great interest since it is typically used in the IF of millimeter- and submillimeter-wave cryogenic receivers. The mixing element in this type of receiver is a superconducting–insulating–superconducting (SIS) junction, a superconducting hot-electron bolometer (HEB), or a Schottky-barrier diode, cryogenically cooled to 4 K.

The 25–34-GHz band is very important in very long baseline interferometry (VLBI) for astronomy and geodesy observation (see VLBI 2010 [11]), as well as for the down link of modern deep-space missions [12].

After a description of the technology in Section II, the device modeling with ambient and cryogenic measurements is shown in Section III. Circuit designs are discussed in Section IV, and their characterization at room and cryogenic temperatures is described in Section V.

II. mHEMT Technology

For ultra-low-noise applications, high electron-mobility transistors (HEMTs) based on InGaAs/InAlAs heterostructures with high In-content in the electron transport channel are the most appropriate devices [13]. These heterostructures can be grown either directly on InP wafers or by using a metamorphic buffer to adapt the lattice constant on GaAs substrates. Major advantages of the metamorphic approach are cost and quality of the GaAs wafers. Furthermore, the material is less brittle compared to InP.

The InAlAs/InGaAs epi-structure is grown by molecular beam epitaxy (MBE) on 4-in semi-insulating GaAs substrates. For the metamorphic buffer, a 1-μm-thick linear

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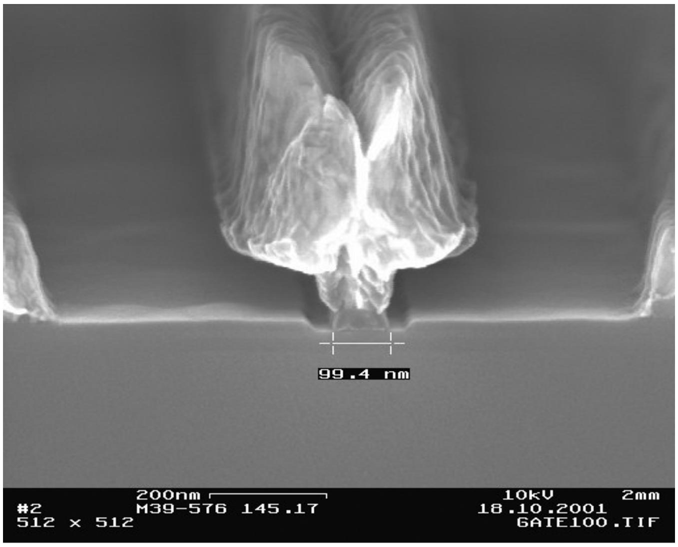

Fig. 1. SEM cross section of a 100-nm mHEMT.

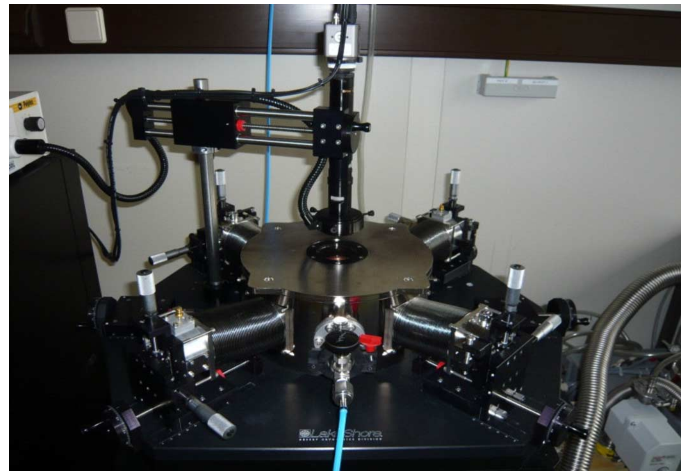

Fig. 2. Cryogenic probe station.

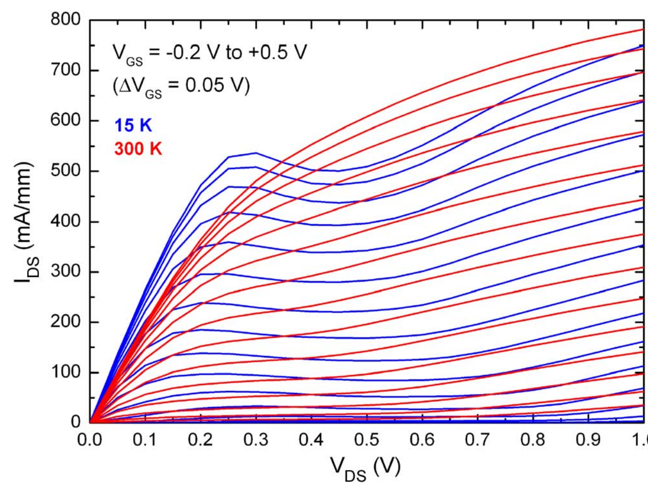

Fig. 3. *I–V* characteristics for a 4 × 15 μm mHEMT device at 15 K (blue in online version) and at 300 K (red in online version) for several gate voltages.

InxAl$_{0.48}$Ga$_{0.52-x}$As $(x = 0 \rightarrow 0.52)$ transition is used. The electrons are confined in a In$_{0.65}$Ga$_{0.35}$As/In$_{0.53}$Ga$_{0.47}$As split channel to increase the breakdown voltage. The low-energy electrons are confined in the In$_{0.65}$Ga$_{0.35}$As layer with high electron mobility. In addition, the high-energy electrons are distributed over both layers, which reduces impact ionization. The split channel is confined by In$_{0.52}$Al$_{0.48}$As barriers. The upper barrier layer includes a silicon δ doping. The layer sequence is capped with a highly doped In$_{0.53}$Ga$_{0.47}$As layer to reduce the ohmic contact and source resistance. A wet chemically mesa etch process is used for device isolation. The InGaAs channel layer is under-etched to avoid contact between the conducting InGaAs channel material and the gate metallization crossing the mesa edge in order to avoid gate leakage currents. Electron beam evaporated GeAu layers are used for the ohmic contacts, which are alloyed at 300 °C on a nitrogen purged hot plate. The 100-nm T gate is defined by 100-kV electron-beam lithography using a three-layer resist (PMMA). The gate recess is etched with a succinic-acid-based solution. Great care is taken to achieve homogeneous lateral etching across the 4-in wafer. An undersized lateral recess width would degrade the breakdown voltage of the device, whereas an oversized lateral recess would increase the source resistance [14]. A Pt Ti Pt–Au layer sequence is used for the gate metallization.

The active devices feature T-shaped 100-nm gates with an indium content of 65% in the main channel. A cross section of a realized 100-nm transistor is shown in Fig. 1. These devices also typically have a f_T of 220 GHz and a $f_{\max}$ of 300 GHz. A two-finger device with 0.06-mm total gate width is used for process monitoring. Typical values are a maximum transconductance of 1400 mS/mm with a drain bias of 1 V and a two-terminal reverse breakdown greater than 4 V at ambient temperature.

The transmission lines used in the MMICs are grounded coplanar waveguides with two metallization levels and 3-μm Au thickness. The process further includes 50-Ω/sq NiCr thin-film resistors, 225 pF/mm^2 metal–insulator–metal (MIM) capacitors, via-holes, and CVD SiN passivation.

The wafers are thinned down to a final thickness of 50 μm. The 100-nm gate-length HEMT devices exhibited more than 90% yield for the fabricated wafers.

III. Device Modeling

The design of cryogenic LNAs requires a small-signal HEMT model with noise parameters; therefore, it was developed first [15]. The S-parameters of the device, both at ambient temperature 300 and 15 K, were measured on a wafer using a thru-reflect line (TRL) calibration, in the cryogenic probe station shown in Fig. 2. From these measurements, parasitic elements and intrinsic capacitances were determined. The noise parameters of the transistors were modeled following the approach of Pospieszalski [16]. Cryogenic models were improved based on the data from numerous runs.

DC measurements were carried out at 300 and 15 K on a representative device with gate length of 100 nm and gate width of 4 × 15 μm. The output *I–V* characteristics are shown in Fig. 3. The device exhibits good pinch-off characteristics. The kink effect appears at around 15 K $V_{\rm DS} = 0.3$ V.

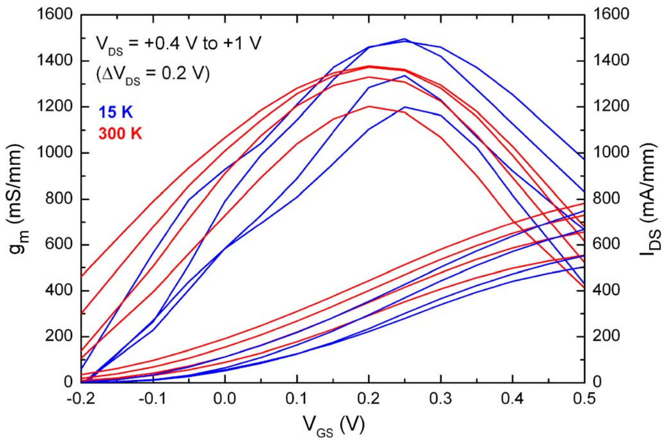

Fig. 4. Transconductance (g_m) and $I_{\rm DS} - V_{\rm GS}$ characteristics for a 4×15 μm mHEMT device at 15 and 300 K for several drain voltages.

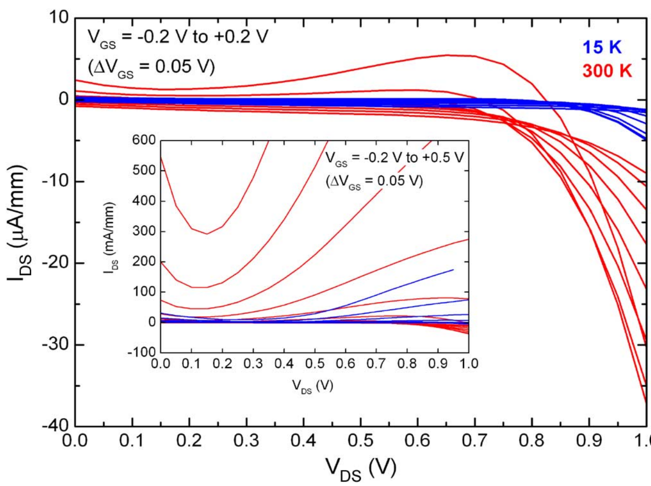

Fig. 5. Gate current–voltage characteristics for a 4×15 μm mHEMT device at 15 and at 300 K for several gate voltages.

The transconductance and $I_{\rm DS} - V_{\rm GS}$ characteristics for the same device are plotted in Fig. 4. The device exhibits a maximum transconductance of 1500 mS/mm with $V_{\rm DS} = 0.6$ V at 15 K and 1400 mS/mm with $V_{\rm DS} = 1$ V at 300 K.

The gate leakage current is an important parameter related to the noise behavior of the device. Measured $I_{\rm GS} - V_{\rm GS}$ characteristics are shown in Fig. 5. The gate leakage at 15 K is lower than at 300 K, in the range of a few nanoamperes for $V_{\rm GS}$ from -0.2 to 0.2 V and $V_{\rm DS}$ from 0.1 to 0.9 V.

The device S-parameters were also measured on wafer at both ambient temperature 300 and 15 K up to 50 GHz. Measurement results can be found in [15] and [17].

IV. Amplifiers Design

To demonstrate the potential of the mHEMT technology at cryogenic temperatures, two MMIC LNAs were designed and manufactured. The two single-ended LNAs cover the frequency range from 4 to 12 GHz (IF for millimeter-wave receivers) and from 25- to 34-GHz VLBI and deep-space bands), respectively.

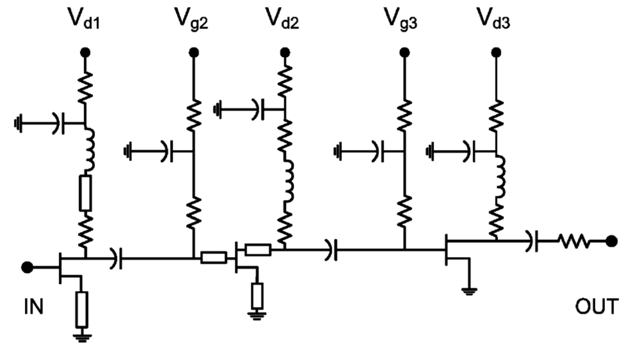

Fig. 6. Schematic diagram of the 4–12-GHz MMIC LNA.

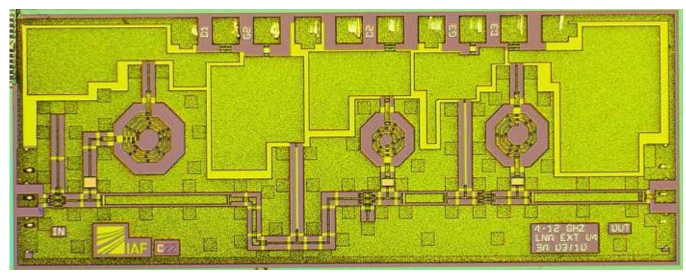

Fig. 7. Photograph of the manufactured 4–12-GHz MMIC LNA. The chip size is 2.5 mm × 1 mm.

A. LNA 4–12 GHz

A simplified schematic of the three-stage 4–12-GHz LNA is shown in Fig. 6. The LNA has three stages, which include 4×30 μm transistors. A photograph of the three-stage 4–12-GHz LNA is shown in Fig. 7. The chip size is 2.5 mm × 1 mm.

The first stage is mainly optimized for minimum noise figure, while the second stage is matched partially for noise, and the third stage fully for gain. Gain flatness and input and output reflection coefficients were also taken into account during the design optimization. Grounded coplanar-waveguide lines are used for matching networks and interconnections. Bias is brought to the transistors through resistors and stubs capacitively shorted with RF bypass MIM capacitors. The resistors act as damping elements suppressing the excess out-of-band gain and stabilizing the amplifier.

Matching the first transistor for minimum noise requires a high impedance of about 100 Ω real part with low losses. An external matching network, on a low-loss substrate, allows more flexibility to match the optimum noise impedance to the source impedance at these frequencies. Therefore, an external microstrip input matching network has been designed as shown Fig. 8, which is fabricated on a 0.254-mm CLTE-XT Arlon substrate with lower losses than GaAs, and the inductance is realized by one 1.6-mm-long bond wire.

This network allows to achieve broadband matching, to reduce the circuit noise figure, and to tune the amplifier. The first gate is biased through the RF input, and this is done through the external input matching network.

In order to characterize its performance, the MMIC was assembled in a gold-plated brass module with SMA coaxial connectors, shown in Fig. 9.

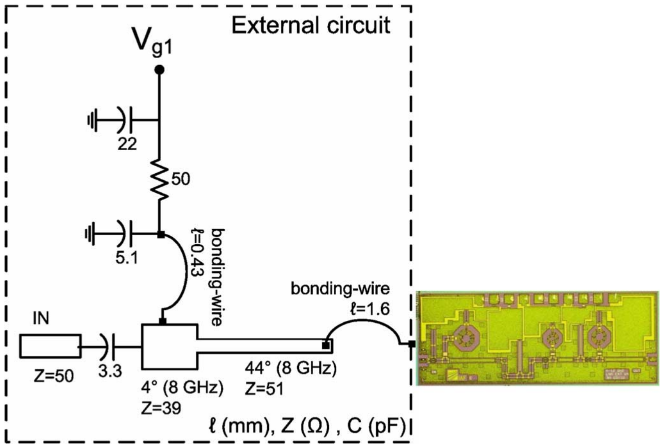

Fig. 8. Schematic diagram of a 4–12-GHz MMIC LNA with the external input matching network.

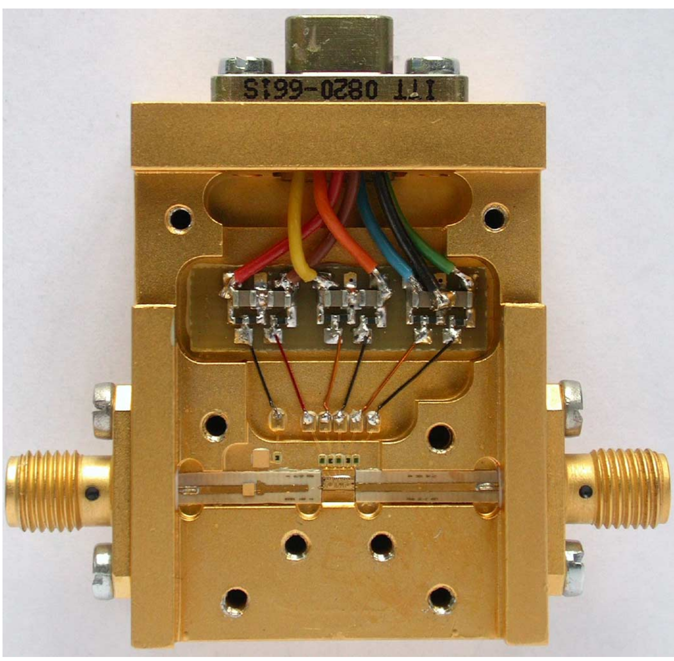

Fig. 9. Packaged module of the 4–12-GHz LNA. The box dimensions are 31.3 mm × 40 mm × 15 mm.

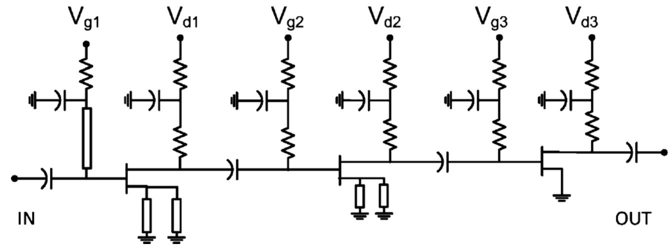

Fig. 10. Schematic diagram of the 25–34-GHz MMIC LNA.

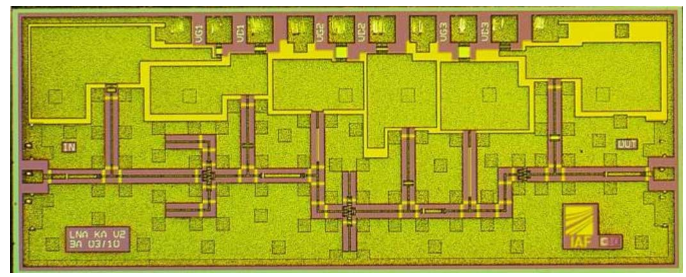

Fig. 11. Photograph of the manufactured 25–34-GHz MMIC LNA. The chip size is 2.5 mm × 1 mm.

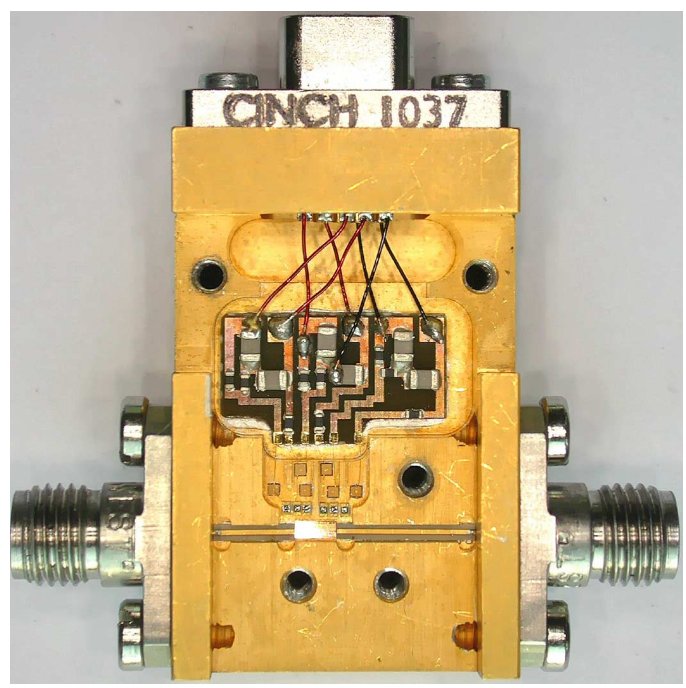

Fig. 12. Packaged module of the 25–34-GHz LNA. The dimensions of the box are 20.6 mm × 32.5 mm × 12 mm.

B. LNA 25–34 GHz

As is shown in Fig. 10, the MMIC LNA consists of three stages; each one employs a 4 × 15 μm transistor, with a source inductive stub in the two first stages. Grounded coplanar-waveguide lines are used for matching networks and interconnection. To accomplish wideband matching, lossy matching networks are used both for interstage matching and for biasing the drains.

A photograph of the three-stage LNA is shown in Fig. 11. The chip size is 2.5 mm × 1 mm.

The LNA MMIC was assembled in a gold-plated aluminium module with 2.92-mm coaxial connectors, shown in Fig. 12. Gold-plated microstrip lines on a 0.127-mm CLTE-XT Arlon dielectric substrate were used at the input and output of the MMIC.

V. Experimental Results

S-parameters, noise temperature, and gain fluctuations were tested at 300- and 15-K temperatures. The chips were first tested on-wafer and then the packaged LNAs were measured at 300 and 15 K. The characterization at cryogenic temperatures of the modules was carried out in a closed-cycle helium cryostat, partially shown in Fig. 13.

For both amplifiers, two units were packaged and tested at cryogenic temperatures in order to verify the measurements. Test results demonstrated very good repeatability, and therefore that the process is sufficiently stable. Moreover, the amplifiers

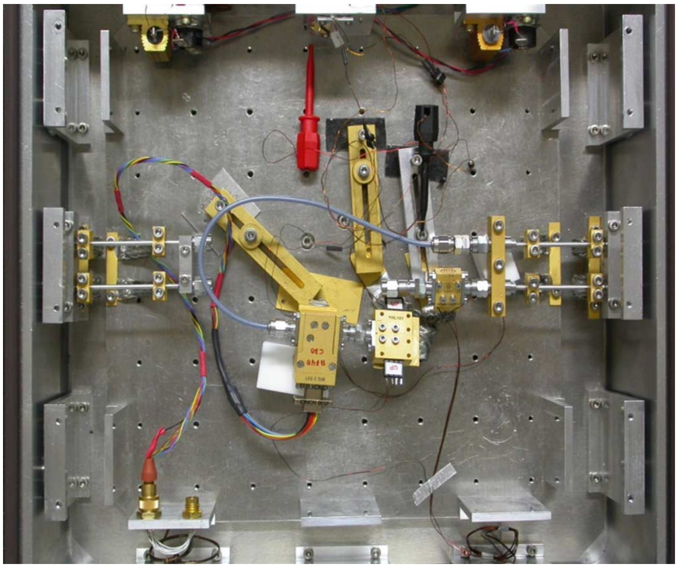

Fig. 13. Amplifier inside the vacuum chamber of the cryostat test system.

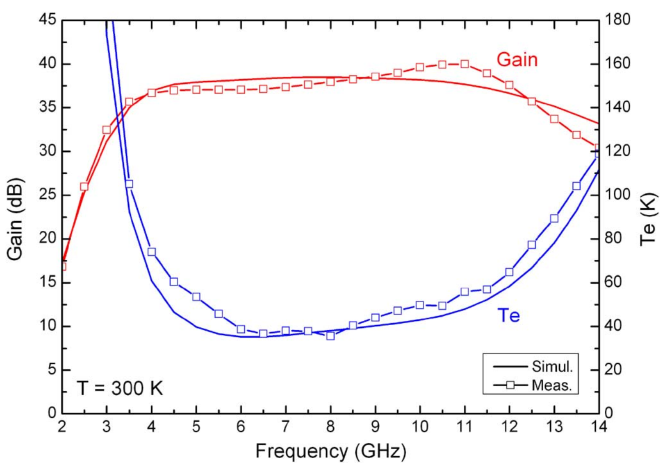

Fig. 14. Measured and simulated gain and noise temperature of the LNA 4–12 GHz at 300 K.

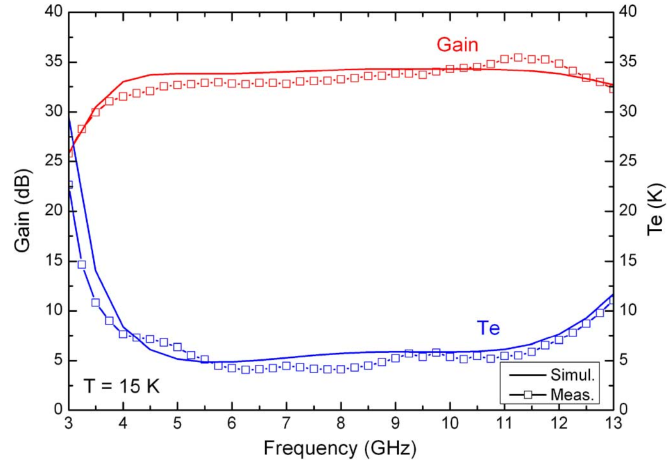

Fig. 15. Measured and simulated gain and noise temperature of the LNA 4–12 GHz at 15 K.

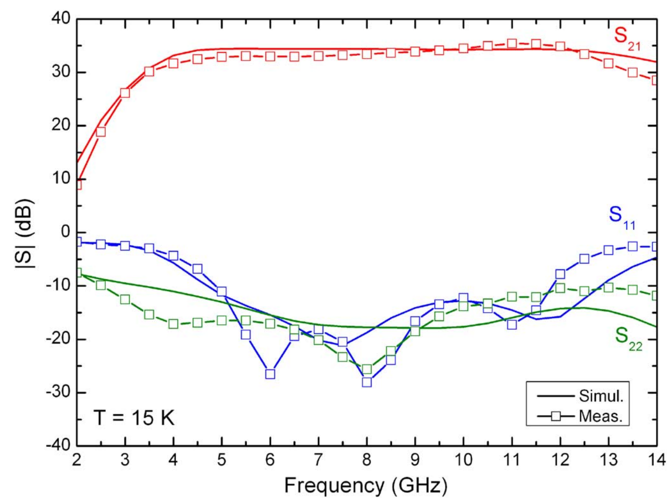

Fig. 16. Measured and simulated S-parameters of the LNA 4–12 GHz at 15 K.

were unconditionally stable at both room and cryogenic temperatures, which was checked from the S-parameter measurement.

A. LNA 4–12 GHz

The 4–12-GHz amplifier was tested at room temperature and it exhibited the gain and noise temperature depicted in Fig. 14. The measured gain was 38 dB with ripple of 1.6 dB in the 4–12-GHz frequency band and with average noise of 47.8 K. The on-chip power consumption for this optimum noise bias was 90.2 mW; $Vd = 1.5$ V, $Id = 60$ mA (166 mA/mm). The minimum noise was 35 K with an associated gain of 37.7 dB at 7.75 GHz.

At 15 K, the cold attenuator method was used to measure the LNA module noise performance, where the incoming noise power is generated by a commercial noise source. A cooled 15-dB attenuator provides a well-defined cold-temperature noise reference at the input of the LNA and reduces the change of reflection coefficient between the on- and off-states of the noise source. In this way, the measurement uncertainty of the noise temperature is reduced to ± 1.4 K.

The measured and simulated gain and noise temperature at 15 K from 3 to 13 GHz are shown in Fig. 15. The simulation comprises the MMIC LNA, as well as the external microstrip network and coaxial connectors. From 4 to 12 GHz, the amplifier achieves 31.5-dB gain with ± 1.8-dB flatness. The average noise temperature is 5.3 K from 4 to 12 GHz. The measurement was made with a drain voltage $Vd = 0.53$ V and a total drain current of 15 mA (41.6 mA/mm). The dc power dissipation is 8 mW on-chip. The minimum noise temperature is 4 K at 6.25 GHz with 30 dB of gain.

The LNA S-parameters at cryogenic temperature (15 K) were also measured referred to the input and output ports of the packaged amplifier for the same bias conditions as in the measurement achieving the best noise performance, shown in Fig. 16. Input and output return losses are greater than 5 and 14 dB in the band, respectively (the input reflection loss (IRL) is greater than 12 dB from 5 to 12 GHz).

B. LNA 25–34 GHz

After testing the S-parameters of the chip on-wafer at room temperature, it was also tested in the cryogenic probes station at 15 K. The S-parameters at 15 K are shown in Fig. 17. With

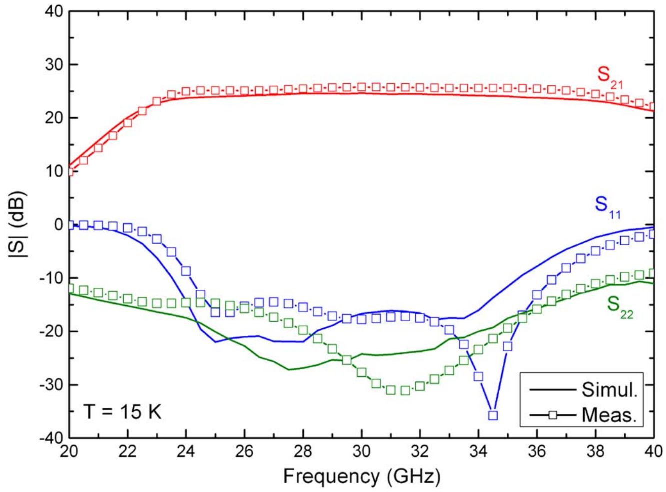

Fig. 17. S-parameters on-wafer of the LNA 25–34 GHz at 15 K.

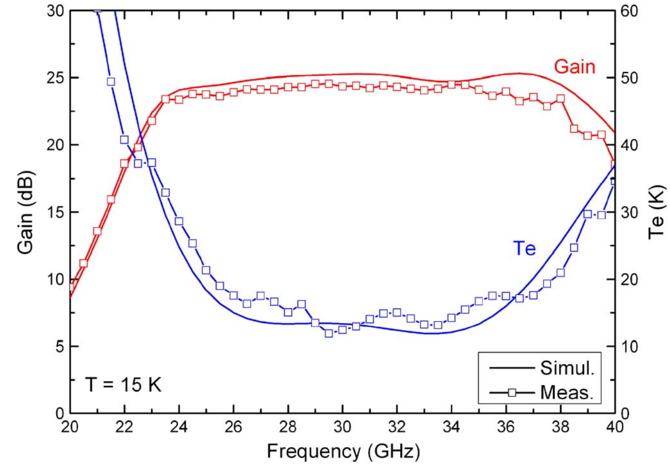

Fig. 19. Measured and simulated gain and noise temperature of the packaged LNA 25–34 GHz at 15 K.

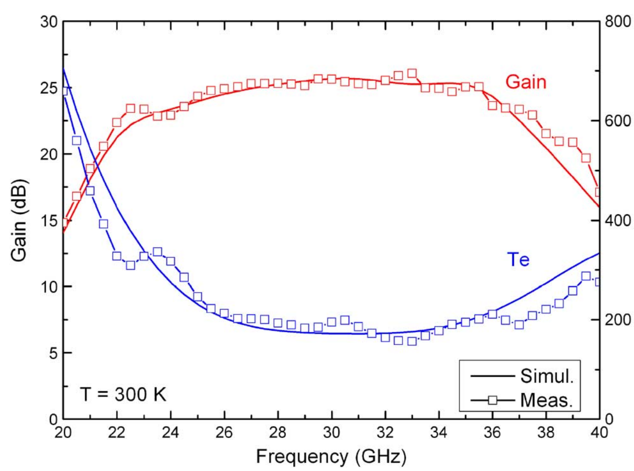

Fig. 18. Measured and simulated gain and noise temperature of the packaged LNA 25–34 GHz at 300 K.

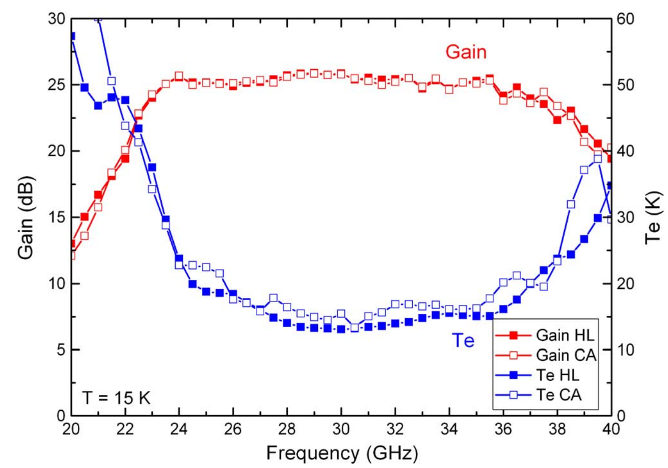

Fig. 20. Measured gain and noise temperature of the packaged LNA 25–34 GHz at 15 K, using the cold attenuator (CA) method with a diode as noise source, and the hot/cold method (HL) with a 50-Ω load at the input of the amplifier.

a power dissipation of 3.6 mW, $Vd = 0.4$ V and a total current of 9.0 mA (50 mA/mm), the gain was 24.3 dB with a ripple of only 0.3 dB. Input and output return losses were greater than 15 and 20 dB in the band, respectively.

The amplifier was then measured in the module with coaxial connectors at 300 K. The gain and noise temperature are depicted in Fig. 18.

The measured gain was 25.2 dB with ripple of 0.8 dB in the 25–34-GHz frequency band. The average noise in the band was 190 K with a power dissipation of 17.3 mW on chip; $Vd = 0.68$ V, $Id = 25.5$ mA (141 mA/mm). The minimum noise temperature was 183 K at 29 GHz, with an associated gain of 25 dB.

Next, the noise performance was measured with the amplifier cooled to cryogenic temperature. The measured and simulated gain and noise temperature from 20 to 40 GHz at 15 K are shown in Fig. 19. The simulation includes the amplifier with bonding wires, microstrip lines, and coaxial connectors. The gain and noise were tested using the cold attenuator method. The measured gain was 24.2 dB with a ripple of 0.4 dB in the 25–34-GHz frequency band and the average noise in the band was 15.2 K. The minimum noise temperature was 11.8 K with an associated gain of 24.5 dB at 29.5 GHz. The power consumption was 2.8 mW on chip; $Vd = 0.37$ V and $Id = 7.5$ mA (42 mA/mm).

An identical LNA from the same wafer was also assembled and tested at cryogenic temperature using two different methods in order to verify the measurements of noise and gain. The methods were: 1) the cold attenuator method with a diode noise source and 2) the hot/cold method with a 50-Ω load at the input of the amplifier [18]. The results obtained in gain and noise temperature for both methods are shown in Fig. 20. The gain was the same, 25.3 $\pm$ 0.6 dB and the average temperature 16.6 K with the cold-attenuator method, and 14.9 K with the hot/cold method, showing a difference in the average temperature of only 1.7 K. In addition, the hot/cold method showed a smoother response of the noise temperature versus frequency.

One of the possible applications of this amplifier is in the front end of cosmic microwave background (CMB) radiation receivers [19], [20]. The very wide band of those receivers combined with the extreme low noise makes the problem of gain fluctuations more prominent. The gain fluctuation of the LNA

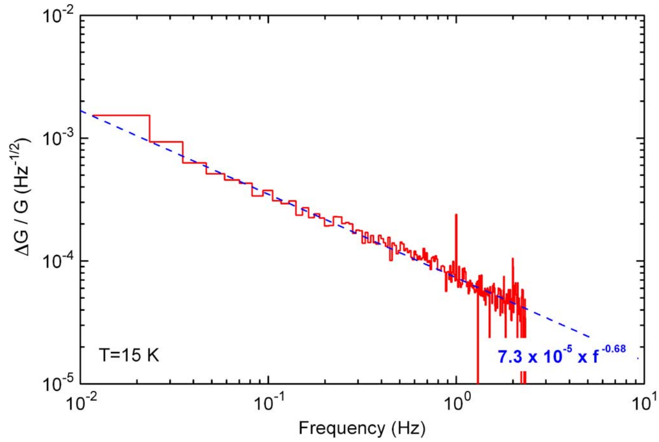

Fig. 21. Normalized gain fluctuation spectrum of the LNA 25–34 GHz at 15 K. The dashed line indicates the noise floor of the measurement system.

TABLE I
COMPARISON OF WIDE-BANDWIDTH LNA AT CRYOGENIC TEMPERATURE

Ref.	Process	Type	Freq (GHz)	Gain (dB)	Te @ Tamb (K)	Pdis (mW)
[1]	0.1 μm InP HEMT	3-stages MMIC	1-11	33.4±0.3	3.9 @ 4.1	24
[2]	0.1 μm InP HEMT	3-stages MMIC	4-12	37	3.9 @ 12	9.2
[6]	0.13 μm InP HEMT	3-stages MMIC	0.5-13	38	4.4 @ 12	16.5
[8]	0.1μm mHEMT	3-stages MMIC	4-12	26±1.2	8.1 @ 15	12
This Work	0.1μm mHEMT	3-stages MMIC	4-12	31.5±1.8	5.3 @ 15	8
[3]	0.1μm InP HEMT	3-stages MMIC	26-40	23±1.1	15.5 @ 12	5.95
		2 cascaded 3-stages MMIC	26-40	41±2.4	11.4 @ 12	--
[4]	InP HEMT	Hybrid	27-37(*)	28±7	14.5 @ 12	--
[5]	InP HEMT	4-stages MMIC	26-36	42	20.0 @ 15	--
This Work	0.1μm mHEMT	3-stages MMIC	25-34	24.2±0.4	15.2 @ 15	2.8

(*) Narrowband design with $Te = 9$ K and Gain $= 30$ dB at 32 GHz when cooled at 12 K.

25–34 GHz operating cryogenically was measured as described in [21]. The spectrum of normalized gain fluctuation (SNGF) measured is shown in Fig. 21. The SNFG is usually modeled by an expression of the form [21]

$$S(f) = \beta \cdot \left(\frac{1\ \mathrm{Hz}}{f}\right)^{\alpha} \tag{1}$$

where $S(f)$ is the unilateral spectral density (i.e., SNGF) with units $\mathrm{Hz}^{-(1/2)}$. In cryogenic LNAs, the parameter α is usually close to 0.5. The best fit to the data shown in Fig. 21 is obtained with $\beta = 7.3\ 10^{-5}\ \mathrm{Hz}^{-(1/2)}$ and $\alpha = 0.674$.

These results would meet the stringent specifications of Atacama Large Millimeter/Sub-millimeter Array (ALMA)[1] or HERSCHEL [22], achieving SNFG values at 1 Hz lower than those obtained for cryogenic InP amplifiers [23].

A comparison of the two LNAs with other reported wideband MMIC LNAs, working in the same frequency ranges at cryogenic temperature, is given in Table I. Almost all data found in the literature refer to InP-based devices. Both presented LNAs offer very low-noise performance with ultra-low-power dissipation at cryogenic temperatures.

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VI. CONCLUSION

Ultra-low-noise MMIC LNAs that can operate cryogenically cooled are required for radio-astronomy applications. We reported the fabrication and characterization of two MMIC LNAs based on 100-nm mHEMT technology. These very low-noise and wide instantaneous bandwidth amplifiers have been developed in order to demonstrate the excellent performance of this mHEMT technology at cryogenic temperatures. Their performance has been characterized in terms of small-signal gain and equivalent noise temperature under cryogenic operating conditions (15 K). A three-stage LNA demonstrated a small-signal gain of 31.5 dB and average noise temperature of 5.3 K from 4 to 12 GHz when cooled at 15 K with only 8.0-mW power consumption.

The 25–34-GHz MMIC LNA exhibited a gain of 24.2 dB and average noise temperature of 15.2 K with 2.8-mW power consumption. Both LNAs offer very low-noise performance with very low-power dissipation at cryogenic temperatures. The presented results demonstrate the high potential of mHEMT technology for cryogenically cooled very sensitive wideband receivers.

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