Current-Sensorless Power Factor Correction with Predictive Controllers

Felipe López,Víctor M. López-Martín,Francisco J. Azcondo, *Senior Member, IEEE,*
Luca Corradini, *Senior Member, IEEE,* and Alberto Pigazo, *Senior Member, IEEE*

***Abstract*—Power Factor Correction (PFC) converters are widely employed for AC/DC conversion to fulfil the applicable standards while ensuring high efficiency. Current-sensorless controllers in PFCs simplify the interaction between power and control circuits, improving noise immunity. This manuscript reviews the state-of-the-art in line current control techniques, identifying relevant contributions that incorporate predictive algorithms, and those that eliminate the current sensor. Furthermore, it evaluates two approaches for current-sensorless PFC. The first is applicable to converters with diode-bridge and includes a high-resolution digital control loop to cancel the estimation errors. The second, valid for bridgeless PFCs, is a new current sensorless control, which includes a fast compensation of the prediction errors with a third-harmonic dependent function generated from a Phase Locked Loop (PLL). This compensation modifies the duty cycle sequence obtained from the controller, ensuring the matching of the line current with the reference obtained from the line voltage. The two evaluated approaches are investigated via computer simulations and experimentally.**

***Index Terms*—Power factor correction, bridgeless, digital control, current sensor, PLL.**

I. Introduction

POWER Factor Correction (PFC) stages are widely employed as active front-end AC/DC converters in single-phase [1], [2] and three-phase [3], [4] grid-connected applications, achieving regulated output DC voltage and high efficiency, while close to unity input Power Factor (PF) [5] is ensured by the analog or digital line current controller. Therefore, the PFC stage usually behaves as a resistor emulator (R_{eq}) seen from the AC side, minimizing the current phase displacement and the harmonic content [6].

The applicable current control techniques classify the PFCs into four groups:

- *Group I*: Operation in Discontinuous Conduction Mode (DCM) or the boundary condition between the Continuous Conduction Mode (CCM) and DCM [7].
- *Group II*: Non-Linear Carrier (NLC) control of the line current, where the switching instants are identified by the comparison of the current with a carrier signal, hysteresis band or a sliding surface that imposes the proportionality between the peak, valley or average current and the input voltage in each switching period [8]–[13].
- *Group III*: Linear control of the average current. Noise immunity improves compared to the NLC technique at the expense of reducing the bandwidth of the current control. Predictive controllers are employed as inner current controllers in [14]–[17], achieving a wider operation range with current measurement.
- *Group IV*: Phasor-based control. The input voltage is assumed sinusoidal, so the modulation function that imposes the line current must be sinusoidal. Predictive controllers are frequently found in bidirectional grid-connected converters [18]. Those developed in a stationary complex reference frame (Clarke Transformation) do not require a PLL, i.e. the deadbeat current controller in [19] or the predictive direct power controller in [20]. Predictive controllers operating in the rotating reference frame (Park Transformation) can benefit from the PLL and generate a synchronously rotating frame to simplify the algorithm and the rejection of current/voltage harmonics. This is the case in [21], where the predictive controller directly generates the duty cycle sequence.

Usually, input current sensors, and the associated signal conditioning circuitry, lead to high cost [22] and complexity; resistive sensors may cause high local power losses (hot spot) and introduce switching noise along with the requirement of gain compensation in the control circuit.

PFCs in *Group I* behave intrinsically as, or nearly as, resistor emulators, so they do not need a current sensor, while controllers in *Groups II* to *IV* can be adapted to operate as predictive ones. They can even avoid current sensing, if the limitations of the current estimation are properly overcome, i.e. effect of nonlinearities and discontinuities, linearization errors and PFC parasitics, among others.

One of the first works about PFC rectifiers without any current sensor was [23], where the duty cycle command is a function of the input and output voltages, the error between the output voltage and the reference voltage and $\frac{\partial|\sin\theta|}{\partial\theta}$, in which θ represents the phase angle of the input voltage, v_g. Among all the references, [24] introduces a universal controller with

Manuscript received February 13, 2018; revised July 11, 2018; accepted January 12, 2019. This work was supported by the Spanish Ministry of Science and Innovation under Project TEC2014-52316-R ECOTREND - *Estimation and Optimal Control for Energy Conversion With Digital Devices*.

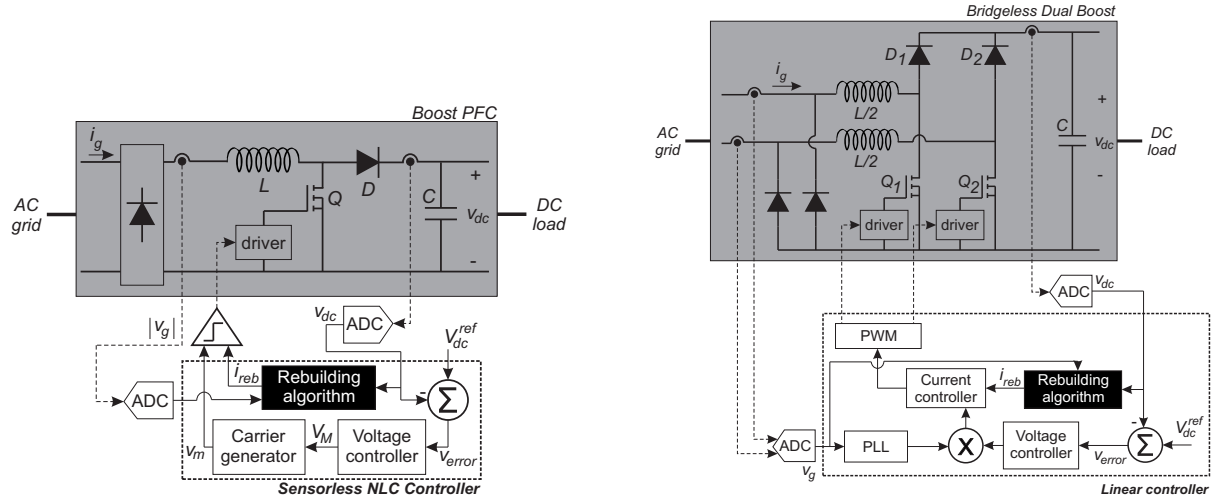
F. López is with the Department of Power Electronics at Norvento Enerxía Innovation Centre (CIne), 27003 Lugo, Spain (e-mail: felipe.lopez@gmail.com).

V. M. López-Martín is with the Department of Power Electronics, IK4-Ikerlan Technology Research Centre, 20500 Gipuzkoa, Spain (e-mail: vmlopez@ikerlan.es).

F. J. Azcondo is with the Department of Electronics Technology, Systems and Automation Engineering, University of Cantabria, 39005 Santander, Spain (e-mail: azcondof@unican.es).

L. Corradini is with the Department Information Engineering, University of Padova, 35131 Padova, Italy (e-mail: luca.corradini@dei.unipd.it).

A. Pigazo is with the Department Computer Systems and Electronics, University of Cantabria, 39005 Santander, Spain (e-mail: pigazoa@unican.es).



(a) (b)

Fig. 1. General structure of the evaluated PFC controllers for a) diode-bridge and b) bridgeless topologies.

a wide range of operation in terms of power, voltage and frequency. Its control diagram is shown in Fig. 1.a. The most recent works proposing current sensorless solutions are [25]–[30].

In [25], only the AC line voltage is acquired and used to generate the switching signal for the MOSFET. Therefore, not only the DC output voltage sensor, but also the AC current sensor can be removed in the control system. A Kalman filter approach to estimate the input current is presented in [26]. Several works avoid the current loop using Single-Loop Current Sensorless Control (SLCSC) for single-phase Boost-type PFC rectifiers. This controller was first presented in [27] as Duty Phase Control (DPC) and presented as SLCSC in [28], where the duty cycle command is computed taking into consideration the parasitic elements. Its model and small-signal analysis is presented in [29]. It provides good behavior under sinusoidal input voltages. A modification of the controller is presented in [30], where the input voltage is measured and the SLCSC is extended to work under distorted input voltages.

A proposal achieving high power factor with a pre-calculated duty cycle for a line period under nominal conditions, which applies these preprogrammed values at the detected half-line zero crossings, is presented in [31]–[35]. In [31] no input voltage changes are considered, and the control responds to load changes. A predictive duty cycle is presented in [32], with a DSP implementation, where the duty cycle command of the next AC line period is computed from the measurement of the input and output voltages. This solution presents limitations under load changes and it is improved in [33] with the measurement of the input current. The pre-calculated duty cycle strategy is applied in [34] with no current acquisition. In [35], the control method is based on the previous experimental acquisitions of the duty cycle command for different load conditions using a current sensor.

The use of bridgeless topologies motivates more the adoption of control without a current sensor. Bridgeless PFCs increase their efficiency by removing the input diode bridge [36], [37]. Consequently, they are prone to suffering noise issues due to the output voltage ground floating relative to the AC line input. To address this issue, several solutions were proposed [37]–[41]. Among them, two of the most promising are: totem-pole bridgeless and dual boost with diode connection between the DC-link reference and the grid line. The former has lower THD_i, but the power MOSFETS do not share the same reference, while the second one requires two additional power diodes [37] (Fig. 1.b).

Apart from the EMI, one of the drawbacks associated with the bridgeless topologies is the difficulty of measuring the AC side variables (voltage and current), because they become differential measurements [37]. Therefore, the overall cost and complexity increases, not only because of the necessity of a differential/isolated current and voltage sensor, but also due to the signal conditioning and acquisition stage [42]–[47].

In [42], [43], the voltage across the boost inductor is continuously estimated based on the input and output voltages and the switching states. This voltage is integrated to obtain the estimated grid current. Similarly, [44] directly calculates the duty cycle based on the input and output voltages and the converter parameters. Finally, one solution within *Group IV* is presented in [48], where the quasi-steady-state analysis of the converter for input current estimation is considered.

The feasibility of current-sensorless predictive controllers in Boost type PFC operating in CCM is presented in this work, showing their advantages, and widening their applicability range. Two predictive approaches applicable to current-sensorless PFCs are evaluated in both linear and nonlinear controllers. New sensorless current control is presented, which includes fast compensation of the current estimation errors by introducing a Phase Locked Loop (PLL) and generating a third-harmonic-dependent function, modifying the duty cycle sequence generated by any controller whose input is the estimated current. This work is organized as follows: Section I has classified the current shaping techniques for PFC, identifying the relevant predictive controllers oriented to remove

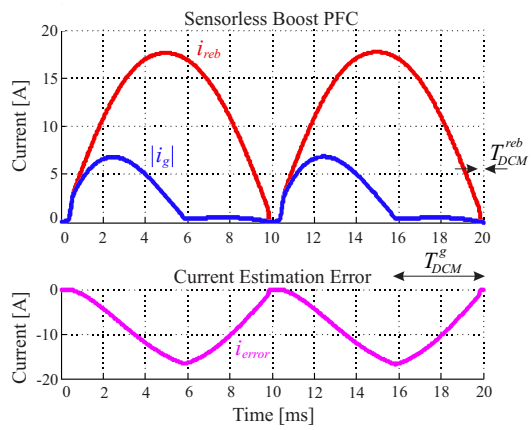


Fig. 2. Current waveforms under a current estimation error situation without any compensation of the estimation error.

sensors in PFC and has motivated the adoption of current sensorless techniques. Section II evaluates two compensation strategies for estimation errors; one for controllers based on the computation of the instantaneous current and another one for controllers that compute the duty cycle sequence. Sections III and IV provide the simulation and experimental results obtained with the proposed controllers and, finally, conclusions are provided.

II. Current-Sensorless Predictive Controllers in PFCs

A. High-resolution current-sensorless strategy in Group II and III PFC controllers

The proposed strategy is applied within a universal digital controller for Boost CCM power factor correction stages, such as the one shown in Fig. 1.a. It is based on the rebuilding concept in [24] and the current estimation is tuned by adopting predictive control strategies. This allows the compensation of the estimation errors, due to variations of the input voltage specifications and power conversion rate.

As introduced in [24], the current rebuilding concepts are based on the converter principles that define the inductor current as follows:

- During ON-state

$$\Delta i_g = \frac{v_g}{L} t_{on} = \frac{\lambda_{L,on}}{L} \tag{1}$$

- During OFF-state

$$\Delta i_g = \frac{v_g - v_{dc}}{L} \left(T_{sw} - t_{on}\right) = \frac{\lambda_{L,off}}{L} \tag{2}$$

where all the variables have been represented in Fig. 1.

The variable volt-seconds (λ_L, defined as $\lambda_{L,on}$ and $\lambda_{L,off}$ for the ON- and OFF- states, respectively) across the inductor is computed in each switching period T_{sw}. The current estimation error accumulated per switching period over the half line cycle is represented in Fig. 2, which is caused by errors in the input and output converter volt-second measurements (with v_g or v_{dc}, respectively) or by a variation in the inductor value, L. The digitally rebuilt input current i_{reb} is the variable

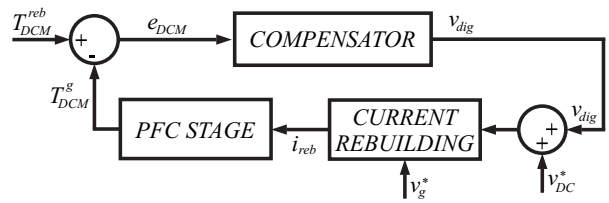


Fig. 3. Block diagram of the DCM time cost function cancellation circuit for predictive current sensorless Boost PFC operating in the CCM.

used in the current loop, and the real current i_g, has a large distortion due to the estimation error $i_{error} = i_g - i_{reb}$. In [24], all the different causes of estimation error are defined and explained in detail, but the implementation, resolution and dynamic response of a high-resolution digital control loop is presented in this manuscript, decreasing this error (i.e. current distortion) and keeping it below the design requirements. The block diagram of this concept is presented in Fig. 3.

The distortion causes a mismatch between the DCM times of both currents over the half line cycle, reducing the power factor (Fig. 2). These times are labeled as T_{DCM}^{g} for the real current, and T_{DCM}^{reb} for the rebuilt current. The digital controller captures these DCM times, as is described in [49], [50], and measures and compares T_{DCM}^{g} and T_{DCM}^{reb} (Fig. 3). The DCM time error function e_{DCM} is computed and minimized with a horizon equal to the half-line cycle. Variable v_{dig} allows vs_L to be compensated, adjusting the DCM times. The DCM time error e_{DCM} is the input of an integral compensator, which internally adjusts the value of the signal v_{dig} until the DCM times match, i.e. $e_{DCM} = 0$.

This feedback loop achieves the close-to-universal digital controller for sensorless Boost CCM power factor correction stages based on current rebuilding concept, which are also robust under variations in the passive element values (inductor or capacitor).

In a PFC operating in CCM, the DCM condition appears close to the AC line zero crossings, where the duty cycle is ideally $d = 1$, but in the real implementation d is saturated before it reaches unity. Therefore, under d saturation condition, T_{DCM}^{reb} is constant at different power levels, and it is used as the DCM time reference. The compensator modifies the value of v_{dig} used in the digital current estimator. With the i_{reb} value, the duty cycle command is obtained and applied to the power stage.

This feedback loop is able to compensate for all the sources of error that appear in this approach, where the current estimation error over the half line cycle is given by the time integration of the volt-seconds estimation error

$$\begin{aligned} i_{error}(t) &= \frac{1}{L}\int_{t-\frac{\pi}{\omega}}^{t} \left(q v_{dig}(\tau) - V_\beta(\tau)\right)\left(1 - d(\tau)\right) d\tau \\ &+ \frac{f_{sw}}{L}\int_{t-\frac{\pi}{\omega}}^{t} v_{dc}(\tau)\Delta t_{on}(\tau) d\tau \\ &+ \frac{1}{L}\int_{t-\frac{\pi}{\omega}}^{t} v_\delta(\tau) d\tau \\ &= i_\beta(t) - i_\delta(t), \end{aligned} \tag{3}$$

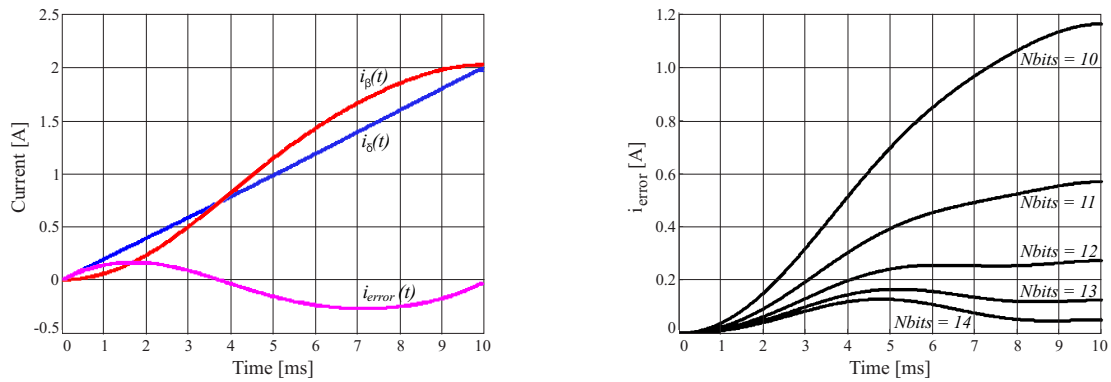


Fig. 4. Current estimation error a) obtained with i_β and optimized linear i_δ, and b) achieved with different number of bits used to represent v_{dig}.

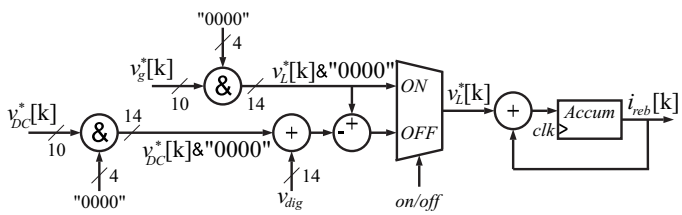


Fig. 5. Current estimator hardware implementation with higher resolution.

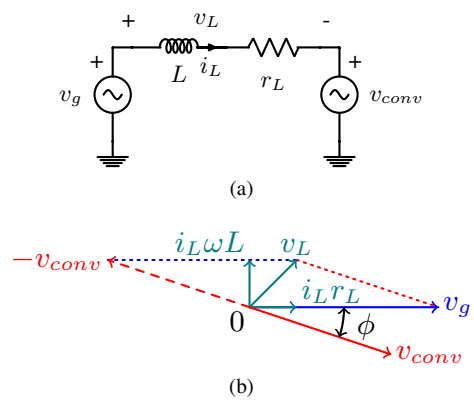


Fig. 6. a) AC variables in bridgeless Dual Boost topology and b) phasor diagram.

where ω and q represent the utility frequency and the bin LSB resolution of the voltages, respectively. $d(t)$ represents the duty cycle. Current estimation errors are due to uncompensated V_β, and Δt_{on}. V_β represents the voltage across the known parasitics while errors in the ON-time estimation are represented by Δt_{on}. The variable v_δ corresponds to additional, not characterized errors. Well defined deviations from the ideal model, (1) and (2), are corrected with a feedforward action. Each current term of (3) can be represented by i_β and i_δ, corresponding to the initial estimation error and the compensation introduced by qv_{dig}, respectively. Figure 4.a shows the resulting waveforms of the expression (3) terms for a given value of v_{dig} that minimizes the current estimation error i_{error}. The 1 LSB uncertainty in v_{dig} results in a current estimation error, i_{error}, as is plotted in Fig. 4.b, over the half line cycle after the controller (Fig. 3) has reached the steady-state.

With this goal, the proposed high-resolution current rebuilding strategy is shown in Fig. 5, which represents the following actual case: a 10-bit ADC is used to acquire the input and output voltages ($v_g^*[k]$ and $v_{dc}^*[k]$), and 4 LSBs are concatenated to obtain 14-bit length. The signal v_{dig} is 14-bit length to provide the resolution required in the system, and it is added to $v_{dc}^*[k]$. With this approach, the resolution can be increased as needed by adding more LSBs to v_{dig}.

B. Current-sensorless strategy in Group IV PFC controllers

The current sensorless technique proposed for *Group II* and *III* PFC controllers can be extended for *Group IV* controllers. Moreover, diverse PFC topologies can be controlled following equivalent current sensorless approaches, as is shown in this section. In bridgeless topologies, the absence of an input diode bridge [36], [37] removes the natural synchronization of the input line current and the grid voltage and the DCM condition around the voltage zero crossings is lost. In order to overcome these issues, a PLL compensates for the absence of the diode-bridge and generates an accurate, noise-free reference signal for the linear controllers.

For analysis purposes, the schema shown in Fig. 6, where the different AC variables are related through the phasor diagram, corresponds to the converter in Fig. 1.b, with linear control and assuming that the actual grid frequency is around the nominal one. The voltage v_{conv} is the product of the control signal, $u_m(t)$, divided by PWM sawtooth amplitude, V_R, and multiplied by the DC-link voltage, v_{dc}. Since v_{conv} lags v_g, $\phi < 0$ and

$$v_{conv}(t) = V_{conv}\sin(\omega t + \phi) = \frac{v_{dc}}{V_R}u_m(t) \tag{4}$$

The DC-link ripple distorts v_{conv}, unless a large capacitor is used, which would increase the system cost and size. In order to compensate for this effect, the DC-link voltage is represented by

$$v_{dc}(t) = V_{dc} - \frac{I_{dc}}{2\omega C}\sin(2\omega t), \tag{5}$$

where I_{dc} is the DC current.

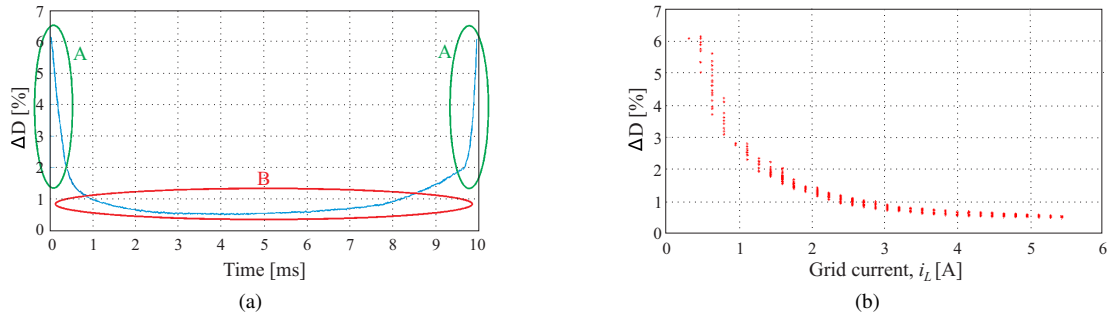


Fig. 7. Effect of a) the delays on the applied duty cycle along a half line period and b) the PFC current on the applied duty cycle.

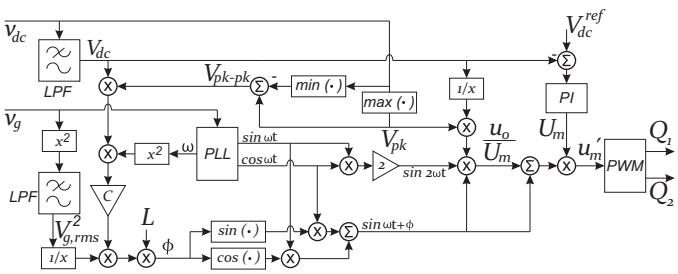


Fig. 8. Proposed current-sensorless controller described in Section II.B.

Therefore, to obtain a sinusoidal current in phase with the grid voltage, the effect of the DC-link voltage ripple, whose amplitude is V_{pk}, must be compensated for in (4). This can be achieved by injecting a predistortion $u_o(t)$ [48], resulting in the control signal

$$u_m'(t) = u_m(t) + u_o(t) = U_m \sin(\omega t + \phi) + u_o(t). \quad (6)$$

By replacing (6) in (4), $u_o(t)$ is obtained

$$u_o(t) \approx \frac{U_m I_{dc}}{2 V_R \omega C V_{dc}} \sin(\omega t + \phi) \sin(2\omega t), \quad (7)$$

which is rewritten using the first and third harmonic as

$$u_o(t) \approx \frac{U_m I_{dc}}{4 V_R \omega C V_{dc}} \left(\cos(\omega t - \phi) - \cos(3\omega t + \phi)\right), \quad (8)$$

where U_m is the power command given by the outer loop, and includes the average DC-link voltage controller. For further circuit simplification, the output voltage acquisition is not used to control the line current in this technique, even though the ripple amplitude of the output voltage is used to estimate the load. The average DC voltage, V_{dc}, is assumed to be constant in steady-state and known for a given application. The capacitance C is also known, for the given the application. The remaining variables need to be evaluated and incorporated by the circuit. Deviations of these parameters due to the manufacturing process, circuit changes and aging are compensated by the control action due to the outer voltage control loop. The grid frequency, ω, which is not constant but bounded, and the term 3ω are provided by a digital PLL. However, there are still two terms that need to be calculated: ϕ and I_{dc}. Their initial values can be obtained from the following analysis. The DC current is obtained from V_{pk}, as expressed below.

TABLE I
BOOST PFC OPERATING CONDITIONS

$V_{g,rms}$	230 V	V_{dc}	400 V
ω	314.16 rad/s	C	220 µF
f_{sw}	100 kHz	R_{load}	250 Ω
L	1 mH	R_L	0.3 Ω
V_D	0.6 V	R_D	0.3 Ω
R_{on}	0.18 Ω		

$$I_{dc} = V_{pk} \cdot 2\omega C \quad (9)$$

Meanwhile, ϕ can be approximated by the following expression, assuming 100% efficiency in the power converter.

$$\phi = \frac{LC\omega^2 V_{dc} V_{pk-pk}}{V_{g,rms}^2} \quad (10)$$

Other effects, such as switching delay or parasitics can be bounded, but the controller deals with them by adjusting the above parameters dynamically. For instance, the switching delay depends on the current through the power device, the voltage across the power device and the driver itself [51]. The effect of the delays throughout one grid half-period on the real duty cycle applied to the power converter, compared with the theoretical one, are shown in Fig. 7.a and Fig. 7.b. The implemented control scheme is shown in the Fig. 8.

III. SIMULATION RESULTS

A. High-resolution current-sensorless strategy in Group II PFC controllers

A current sensorless Boost converter with diode-bridge using the high-resolution error compensation feedback loop is modeled and evaluated. The model parameters are given in Table I and, from (3) and Fig. 4.a, the selected resolution is 14 bits. The simulation results obtained are shown in Fig. 9, where the maximum current estimation error achieved is 30 mA. The evaluated PF and THD_i are 0.997 and 1.78 % respectively.

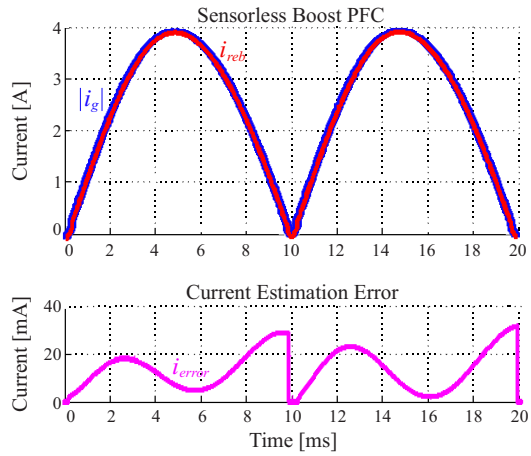


Fig. 9. Current waveforms with the proposed high-resolution compensation error.

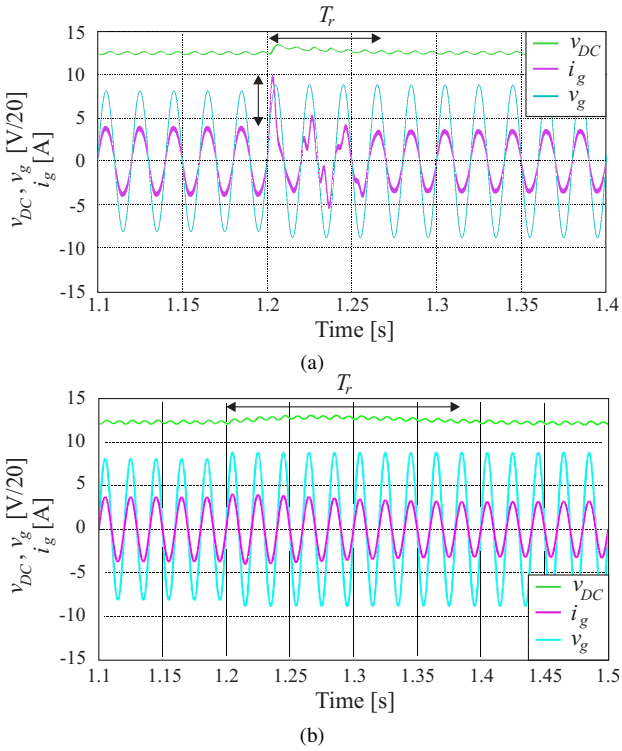


Fig. 10. Bridgeless dual boost response (simulation) to an input rms voltage step from 115 V to 125 V. a) sensorless controller and b) sensor-based equivalent controller. Green, v_{dc}, 5 V/div. Purple, i_g, 5 A/div. Blue $v_g/20$, 5 V/div. Time scale 50 ms/div.

B. Current-sensorless strategy in Group III PFC controllers

The simulation parameters for the bridgeless topology are shown in Table II. To evaluate the response of this method, Fig 10 shows the simulation results before and after a rms voltage step from 115 V to 125 V. At 1.2 s, a grid voltage step is applied. It can be seen that the grid current becomes temporarily non-sinusoidal because the PLL loses synchronization during the transient recovery. However, once the PLL is locked again, the grid current obtained is sinusoidal and in phase with the grid voltage. The response time T_r is 72.4 ms and the maximum input current during the transient reaches

TABLE II
BRIDGELESS PFC OPERATING CONDITIONS

$V_{g,rms}$	115 V	V_{dc}	250 V
ω	314.16 rad/s	C	550 µF
f_{sw}	98.5 kHz	R_{load}	200 Ω
L	1.1 mH		

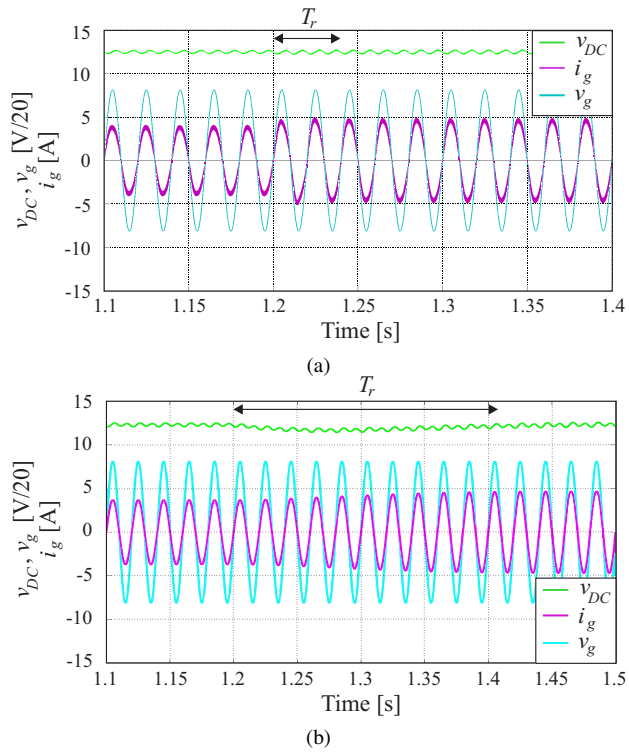


Fig. 11. Bridgeless dual boost response (simulation) to a load step from 200 Ω to 167 Ω. a) sensorless controller and b) sensor-based equivalent controller. Green, v_{dc}, 5 V/div. Purple, i_g, 5 A/div. Blue $v_g/20$, 5 V/div. Time scale 50 ms/div.

9.77 A. The obtained results with the equivalent sensor-based approach controller is shown in Fig. 10.b, where the grid current waveform keeps the sinusoidal shape but exhibits a slower response, $T_r = 187.6$ ms.

A load step from $R = 200\ \Omega$ to $R = 167\ \Omega$ is shown in Fig. 11. The step is applied at 1.2 s. In this case, since the PLL is not affected by the load step, the algorithm adapts to the new conditions instantaneously and i_g is slightly distorted during $T_r = 28.1$ ms. The grid peak current varies from 3.79 A to 4.65 A, and output voltage ripple increases 1 % after T_r. The response of the sensor-based controller (Fig. 11.b) is slower, due to absence of the third-harmonic injection strategy in Fig. 11.a, and reaches $T_r = 203.2$ ms.

The performance of the proposed controller has been evaluated in steady-state and a load transient, considering different resolutions for $u_o(t)$ in (8). Results are shown in Fig. 12.a and 12.b, respectively. Three different $u_o(t)$ resolutions (10, 12 and 16 bits) and a 12 bits ADC is used to acquire v_g. Figure 12.a shows that increasing the resolution improves the i_g waveform. The THD_i is 8.8 % with 10 bits, 5.0 % with 12 bits and reaches 4.2 % with 16 bits. Fig. 12.b shows that to increase the resolution has a negligible effect on the i_g

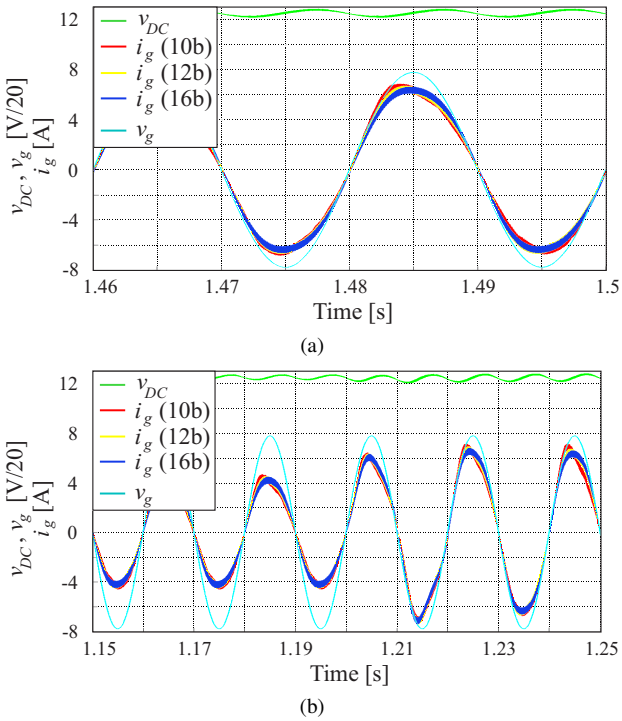


Fig. 12. Effect of resolution on the third-harmonic injection strategy performance. a) steady-state, b) load step transient.

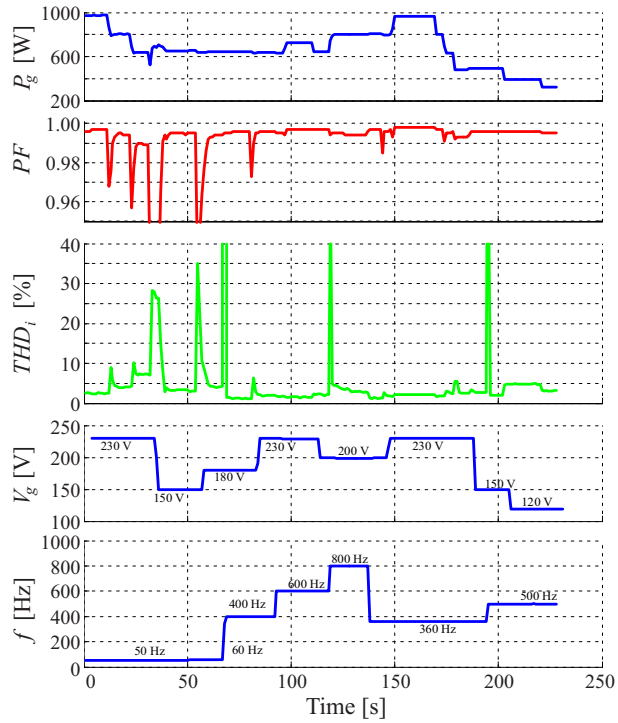


Fig. 13. Experimental time evolution of the different electrical variables with $V_{dc} = 400$ V, $f_{sw} = 96$ kHz.

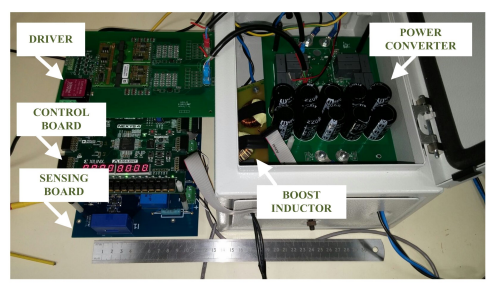


Fig. 14. Experimental prototype of the bridgeless sensorless converter and controller.

waveform in the load step.

IV. Experimental Results

A. High-resolution current-sensorless strategy in Group II PFC controllers

A 1 kW Boost converter with diode-bridge using the digital feedback loop for sensorless topologies is built and tested. The output dc voltage reference is 400 V with an input rms voltage ranging from 120 V to 250 V. The resolution is obtained using (3) at the zero-crossing of v_g, $v_g = 0$ V, assuming an upper boundary for the output voltage, $V_{dc,max}$, $q = V_{dc,max}/(2N-1)$. In the experimental set-up, $q \approx 25$ mV. The switching frequency is 96 kHz. The capacitance of output capacitor is 220 µF, the inductance of the inductor is $L = 1$ mH, the MOSFET and diode used to build the prototype are a IRFP27N60K from International Rectifier™and a IDH12S60 from Infineon™. The digital PFC controller is described in VHDL and implemented in a Xilinx XC3S200E field programmable gate array (FPGA). A second order *ad-hoc* sigma delta ADC is used for the output voltage and a commercial TLV1572 serial 10-bit ADC for the input voltage to obtain the voltage data.

The DCM time feedback loop sets v_{dig} to compensate for the current estimation error in all the different situations. To evaluate this approach, the converter controlled by the FPGA is tested under different voltage, grid frequency, and randomly applied load steps. The results of this experiment are shown in Fig. 13. The variables V_g (rms input voltage) and ω (grid frequency) are modified manually in the Agilent 6813B AC power source, used to supply the Boost converter, and the power demanded from the grid P_g (input voltage) is changed with load steps. PF (power factor) and THD_i are the output variables used to evaluate the performance of the controller. It can be observed that every step in V_g, ω or P_g decreases the PF value. The more aggressive the step is, the higher the instantaneous change in the PF value. At the same time, in parallel with the PF modification, the THD_i value increases. This current distortion is detected by the DCM time feedback loop, which compensates for the DCM time mismatch, always increasing the PF up to a value greater than 0.990. At the frequency steps from 60 Hz to 400 Hz, from 400 Hz to 800 Hz and from 360 Hz to 500 Hz, the THD_i shows impulse like modifications over time due to the effective error compensation, while apparently the PF remains high because the power analyzer does not track such high-speed changes.

B. Current-sensorless strategy in Group IV PFC controllers

A laboratory prototype of a bridgeless dual boost converter (Fig. 14) has been developed. The laboratory setup consists of

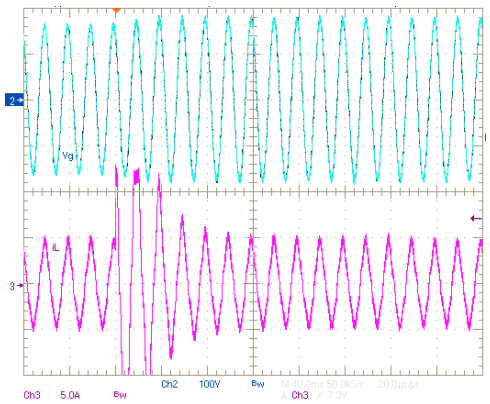


Fig. 15. Experimental results of bridgeless sensorless controller response under 115 V to 125 V input rms voltage step response. Above, input voltage, v_g, 100 V/div. Below, input current, i_L, 5 A/div. Time scale 40 ms/div.

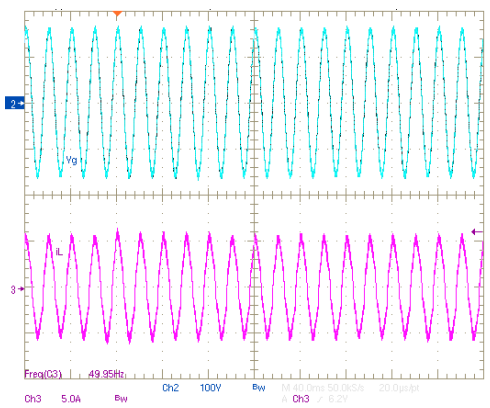


Fig. 16. Experimental result of the bridgeless sensorless controller response under 200 Ω to 167 Ω load step. Above, input voltage, v_g, 100 V/div. Below, input current, i_L, 5 A/div. Time scale 40 ms/div.

the following elements:

- For ease of implementation, a Full-Bridge topology based on Vincotech™Power MOSFET Modules V23990-P722-F64-PM, where the two upper MOSFETs are disabled, is used.
- Power MOSFET drivers based on Scale cores (2SC0650P).
- Sensing Board. Used to measure the DC-link and the grid voltages needed to implement the proposed algorithm.
- Digilent™Nexys 4 board (based on Xilinx 7 XC7A100T-1CSG324C) used to implement the digital control.

Throughout the experimental validation, the switching delays are compensated for by limiting the duty cycle to 90 % around voltage zero crossing (zone A) and subtracting a constant value for the rest of the half period (zone B), as shown in Fig. 7.a.

The results are the following. Firstly, in the same way as for the simulation results, a grid rms voltage step was applied from 115 V to 125 V in Fig. 15.

Similarly, in a second experiment following simulation tests, a load step from 200 Ω to 167 Ω was applied, obtaining the results shown in Fig. 16.

Finally, in steady state, the results obtained are shown in Fig.

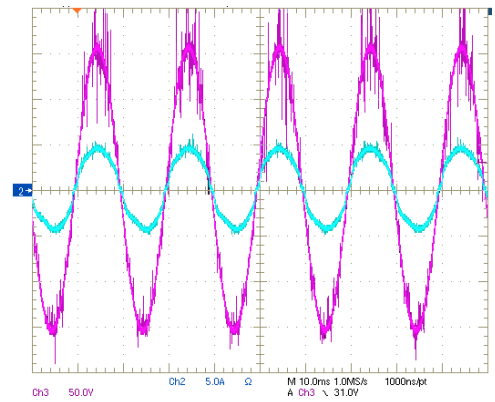


Fig. 17. Steady-state result of the bridgeless sensorless controller under the conditions in Table I. Blue, i_L, 5 A/div. Purple v_g, 50 V/div. Time scale 10 ms/div.

17. The values obtained are THD_i = 6.3 % and $PF = 0.996$, which fulfils the standard IEC 61000-3-2, Class C.

V. Conclusion

In addition to the advantages that digital controllers obtain for power converters in terms of flexibility and synchronization, PFC stages benefit from simplifications in the power variable acquisition circuits and filters, resulting in cost savings, better power efficiency and lower harmonic distortion. Current sensorless control simplifies the acquisition and signal-conditioning circuitry, and reduces the interaction between the power and the control circuits, improving noise immunity.

Strategies to generate PFC controllers have been reviewed and classified into four groups to identify the feasibility of adapting those controllers to using the estimation of the current with a plant model approach. Different current sensorless controllers have also been reviewed, identifying their limited range of operation in terms of input voltage and load along with the approaches that compensate for the current estimation errors that greatly extend the applicability range.

Therefore, the potential application range of PFC controllers without current sensors covers all the input voltage amplitudes and frequencies as well as a wide load range, when a complete cancelation of the current estimation errors is achieved with an extra feedback loop included for this purpose. This specific feedback loop is inherently slow and obtains the duty cycle with the required resolution. The PFC response is improved with predictive modulators and feed-forward algorithms that rapidly bring the duty cycle sequence to the optimum one.

By replacing the threshold detection of the converter operating in DCM or current zero crossing with the reference of a PLL, several advantages are found, including the extension of the current sensorless control technique to bridgeless topologies and improvements in the controller response under grid voltage events. The compensation of the estimation errors using a third-harmonic component using the PLL reference leads to a faster response of the estimation error cancellation and lower distortion in input voltage and load transients. The two discussed approaches have been investigated via computer

simulations and experimentally. This approach makes it possible to obtain a PFC controller without current sensor within the ranges covered by commercial PFC ICs.

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Felipe López received the Telecommunication Engineering degree from the University of Vigo, Galicia, Spain, in 2012 and the Master's degree in Industrial Engineering from the University of Cantabria, Cantabria, Spain in 2015.

Since 2013 he has been with the TEISA Department at the Universidad de Cantabria where he is working towards his PhD. Since 2017 he is working as Power Electronics engineer at Norvento Enerxía. His research interests include control of switching power converters and power quality.

Víctor M. López-Martín (S'10) was born in Torrelavega, Cantabria, Spain, in 1985. He received the Electronics and Control Engineering degree from the University of Cantabria, Santander, Spain, in 2009, and the Power Electronics PhD degree from University of Cantabria in 2013.

From June to September 2012, he was a Visiting Scholar in the Colorado Power Electronics Center (CoPEC), University of Colorado at Boulder, and from September to December 2012 at the Utah State University Power Laboratory, Logan, USA. Both periods with the Professor R. Zane as an Advisor. Since 2015 he is working as Power Electronics designer in IK4-Ikerlan, in the Power Electronics area. His research interests include SiC power modules, power converters for traction and renewable energy applications, and resonant converters.

Dr. López received the IEEE/IEL Electronic Library Award in 2009.

Francisco J. Azcondo (S'90-M'92-SM'00) received the Electrical Engineering degree from the Universidad Politécnica de Madrid, Madrid, Spain, in 1989, and the Ph.D. degree from the University of Cantabria, Santander, Spain, in 1993. He has been a Visiting Researcher with the Department of Electrical, Computer, and Energy Engineering, University of Colorado, Boulder, CO, USA, from 2004 to 2010, the Department of Electronics and Communication Engineering, University of Toronto, Toronto, ON, Canada, in 2007, and the Utah State University Power Electronics Laboratory, Department of Electronics and Communication Engineering, Utah State University, Logan, UT, USA, in 2013. Since 2004, he has been a Special Member (appointed as a Graduate Faculty) with the Department of Electrical, Computer, and Energy Engineering, University of Colorado, renovated until 2017.

He is currently a Professor with the Department of Electronics Technology, Systems and Automation Engineering, and Dean of the School of Industrial and Telecommunications Engineering, University of Cantabria. His current research interests include modeling and control of switch-mode power converters and resonant converters, digital control capabilities for switched-mode power supplies, and current sensorless control for grid connected converters and applications, such as outdoor lighting, electrical discharge machining, and arc welding.

Dr. Azcondo has been the Chair of the IEEE Industrial Electronics Society - Power Electronics Society Spanish Joint Chapter from 2008 to 2011. He has been an Associate Editor of the IEEE Transaction on Industrial Electronics. At present, he is an Associate Editor of the IEEE Transaction on Power Electronics and the IEEE Journal of Emerging and Selected Topics in Power Electronics.

Luca Corradini (S'06-M'09-SM'14) received the Laurea degree in electronic engineering and the Ph.D. degree in industrial electronics from the University of Padova, Italy, in 2004 and 2008 respectively.

From 2008 to 2011 he was a postdoctoral Research Associate at the Colorado Power Electronics Center (CoPEC), University of Colorado at Boulder, USA. From 2011 to 2017 he was Assistant Professor at the University of Padova, Italy, where he has been Associate Professor since 2017.

His research interests in power electronics are primarily focused on digital control and modeling of switched-mode power converters, and power management solutions for energy harvesting systems.

Dr. Corradini received the second 2008 Prize Paper Award from the Industrial Power Converter Committee of the IEEE Industry Applications Society. He is currently an Associate Editor of the IEEE Transactions on Power Electronics.

Alberto Pigazo (M'05-SM'14) was born in Santander, Spain. He received the M.Sc. and Ph.D. degrees in physics (electronics) from the University of Cantabria, Santander, Spain, in 1997 and 2004 respectively.

Since 2012 he has been an Associate Professor with the Dept. of Computer Science and Electronics, University of Cantabria. He was a guest researcher at the Power Electronics Laboratory, Polytechnic of Bari, Italy, in 2007, and a visiting professor at the Center of Reliable Power Electronics, Dept. of Energy Technology, Aalborg University, Denmark, in 2013, and the Chair of Power Electronics, Christian-Albrecht University of Kiel, Germany, in 2013. His research interests include active power filtering, power converters for grid integration of renewable energy sources and power electronics for ships.