Improving the Dynamic Performance of Bridgeless PFC Controllers with Zero Crossing Detector and Root-Mean-Square Calculation Blocks

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***Abstract*—Bridgeless Power Factor Correctors (PFC) with a controller utilizing rectified ac variables can benefit from well-established strategies and circuits employed in PFCs with diode-bridge front-end. The grid voltage polarity is detected to compute the rms value of the grid voltage, and also used to generate and route the gate signals for the power devices. However, depending on the implementation, grid voltage disturbances may propagate through the polarity detection and RMS calculation stages, leading to a degradation of the input current and output voltage. This issue is addressed in this manuscript by investigating a single-phase bridgeless totem-pole (TP) PFC through simulation and proposing the replacement of the conventional implementation with a frequency-locked loop (FLL) to enhance the converter dynamics.**

***Index Terms*—Power factor corrector (PFC), bridgeless totem-pole (TP), Zero-crossing detector (ZCD), Frequency-locked loop (FLL).**

I. Introduction

Bridgeless Power Factor Correctors (PFCs) result in high power conversion efficiency and power density by eliminating the need for an input bridge rectification stage [1]. Additionally, the utilization of soft switching techniques and wide band gap (WBG) power devices helps to minimize power losses and enables higher switching frequencies [2]–[4]. From a control standpoint, bridgeless PFCs present various challenges [5], including the requirement for an accurate detection of AC voltage zero-crossings to minimize current harmonic distortion. Furthermore, the incorporation of Zero-Crossing Detectors (ZCD) in bridgeless PFCs enables the use of well-established control strategies from diode-bridge PFCs in both analog and digital implementations.

Figure 1 illustrates a single-phase bridgeless totem-pole (TP) branch PFC. The gate signals for the high-frequency (HF) switching are generated by a unipolar pulse width modulator, while the leg switching at the grid frequency relies on the grid voltage polarity. Consequently, the bridgeless TP PFC operates as a boost PFC during each semi-cycle of the grid voltage [3].

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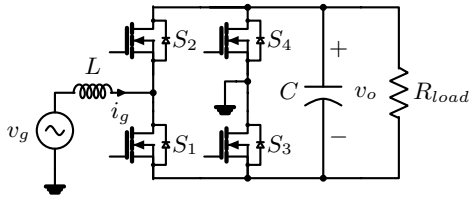

Fig. 1: Single-phase bridgeless totem-pole PFC.

The ac side variables are measured and conditioned to generate rectified ac signals for the inner and outer control loops. In analog controllers, this rectification is achieved through a signal conditioning circuitry when utilizing integrated circuits (IC), such as the UCC28070 by Texas Instruments [6] or the ICE3PCS01G by Infineon [7]. Alternatively, in controllers implemented in digital electronic devices, such as the UCD3138 by Texas Instruments [8], the rectification of AC signals is performed digitally, as depicted in Fig. 2.

This manuscript assesses the performance of a single-phase bridgeless TP PFC with a conventional digital controller implementation that utilizes rectified ac variables, particularly under grid voltage variations. Furthermore, a proposed enhancement of the converter dynamics is introduced, involving the substitution of the conventional grid voltage polarity and rms calculation block with a frequency-locked loop (FLL). The effectiveness of this proposal is verified through simulation tests.

II. Digital controller with rectified ac variables

The outer control loop in Fig. 2 regulates the output voltage, v_o, by adjusting the amplitude of the input reference current, i_g^*, through a PI controller, G_v. This controller acts on the error signal between the reference output voltage, V_o^{ref}, and the measured output voltage, v_o.

The instantaneous phase in $\left|i_g^*\right|$ is determined by dividing the rectified grid voltage, $|v_g|$, by its rms value, V_g. This ensures that the bridgeless TP PFC effectively functions as a resistor emulator. The measured ac variables are rectified with the assistance of a $rect$ signal, with value ± 1 depending on the grid voltage polarity.

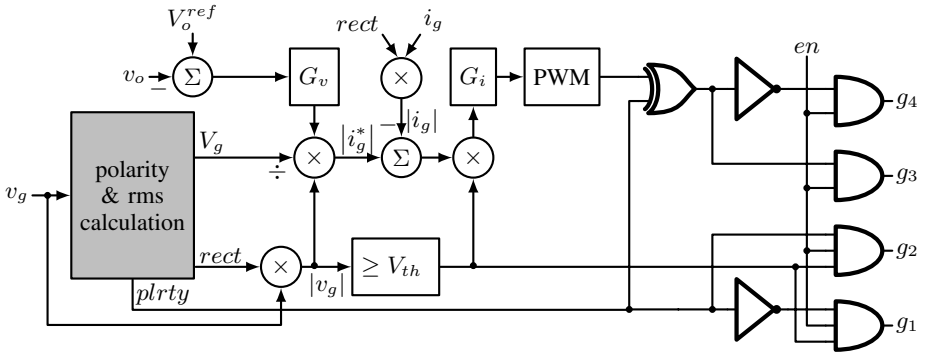

Fig. 2: Digital controller with rectified ac variables for the single-phase bridgeless TP PFC.

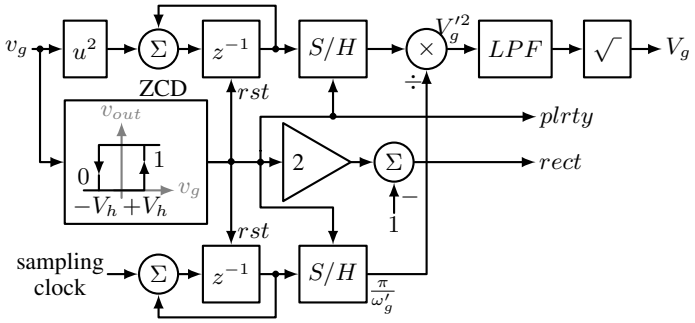

Fig. 3: Conventional implementation of the *polarity & rms calculation* block.

The inner current control loop compares the rectified measured grid current, $|i_g|$, with the reference current, $|i_g^*|$. The resulting error signal is then utilized by a PI controller, designed using standard techniques applicable to PFCs with diode-bridge front-end [9].

To mitigate the impact of duty cycle jumps caused by polarity changes in the grid voltage, the current controller is temporarily disabled during zero crossings. This is achieved by comparing $|v_g|$ with a threshold voltage, V_{th}, typically set at a sufficiently low value.

Furthermore, the logic polarity signal, $plrty$, is employed to route the gate signals for HF switching devices and select the appropriate device to switch on in the grid frequency switching branch.

The *polarity & rms calculation* block, in Fig. 2, is responsible for evaluating V_g and providing the signals $rect$ and $plrty$.

A. Conventional implementation of the polarity & rms calculation block

Figure 3 illustrates the conventional digital implementation of the polarity and RMS calculation block. A zero-crossing detector (ZCD) is employed to generate the $plrty$ signal, which incorporates a hysteresis band, $\pm V_h$, to reject noise in the measurement chain. The $rect$ signal, utilized for rectifying the AC variables, is derived by level shifting the $plrty$ signal. Both the falling and rising edges of the $plrty$ signal are utilized to reset two accumulators responsible for integrating v_g^2 and determining the duration of each half-period of the grid voltage, denoted as $\frac{\pi}{\omega_g'}$. The grid frequency estimation, ω_g', derived from the ZCD has effect on a very first calculation of the rms value of v_g, $V_g'^2$, which, assumed half-period symmetry of v_g, results in

$$V_g'^2[n] \approx \frac{\omega_g'[n]}{\pi} \sum_{i=W[n-1]+1}^{W[n]} v_g^2[i] T_s, \tag{1}$$

with $W[n] - W[n-1]$ being the number of samples per semiperiod n of the grid voltage, i.e. $W[n] - W[n-1] = round\left(\frac{\pi}{\omega_g'[n]} \frac{1}{T_s}\right)$, and T_s is the sampling period of the controller, which typically matches the switching frequency, T_{sw}.

Since (1) updates based on the edges of the $plrty$ signal, a low-pass filter (LPF) is necessary for smoothing. Typically, a first-order LPF with a cutoff frequency set below the nominal grid frequency, ω_0, is employed. Ultimately, V_g is obtained by taking the square root of the LPF output.

B. Proposed implementation of the polarity & rms calculation block

The conventional implementation of the polarity and rms calculation block may suffer from inaccurate detection of polarity changes, leading to a degradation in the evaluation of (1). Additionally, the low cutoff frequency utilized in the LPF can result in slower converter dynamics. This is because the variations in V_g need to be compensated by the outer control loop, as illustrated in Fig. 2.

To address these issues, the proposed solution employs a second-order generalized integrator (SOGI) with a frequency-locked loop (FLL). The SOGI-FLL approach has been extensively used in grid-following (GFL) power converters for grid synchronization purposes [10]–[15]. By implementing the configuration illustrated in Fig. 4, achieving a faster estimation of V_g is possible. This, in turn, eliminates the requirement for the outer control loop to compensate for such variations.

The parameter K_{SOGI} leverages the harmonic filtering capabilities of the SOGI cell in steady-state while also affecting the dynamic response. Similarly, the parameter γ_{FLL} balances the speed of the frequency adaptation strategy with the ripple

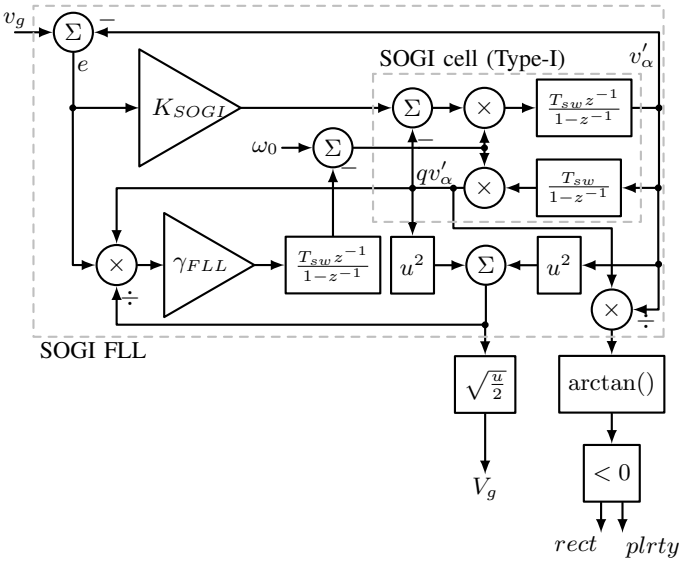

Fig. 4: Proposed implementation of the *polarity & rms calculation* block.

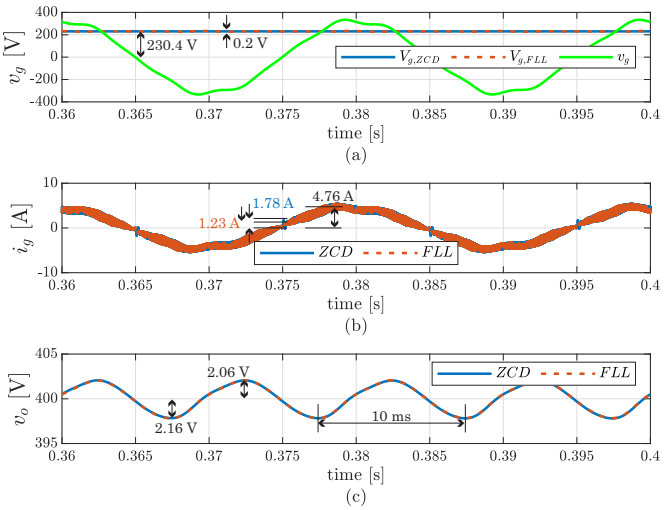

Fig. 5: Steady-state results with harmonically distorted grid voltages. a) grid voltage, b) grid current, and c) output voltage

of the estimated grid frequency. The estimation of V_g is derived from the fundamental amplitude estimation, used within the FLL to maintain its dynamic response remains unaffected by grid voltage variations. Both the $rect$ and $plrty$ signals are generated by comparing the phase of the grid voltage fundamental with zero.

Since the estimation of V_g is based solely on the fundamental grid voltage, any deviations from the actual V_g values are primarily caused by grid voltage harmonics. In low voltage distribution grids, these harmonics are typically relatively small, with a total harmonic distortion (THD) of less than $5\,\%$. Furthermore, these harmonic components change over a larger time scale, such as daily variations.

Similar to the conventional implementation, the outer control loop must compensate for these effects caused by grid voltage harmonics to ensure accurate regulation of the output voltage despite the presence of harmonics in the grid voltage.

III. Simulation Results

A digitally controlled bridgeless TP PFC has been modeled in MATLAB/Simulink® and PLECS®, using the following parameter values: nominal grid frequency $f_{g,nom} = 50\,\text{Hz}$, nominal grid voltage $V_{g,nom} = 230\,\text{V}$, inductor value $L = 500\,\text{mH}$, capacitor value $C = 1.41\,\text{mF}$, load resistance $R_{load} = 220\,\Omega$, reference output voltage $V_{o,ref} = 400\,\text{V}$, threshold voltage for the current controller and power devices switching at low frequency, $V_{th} = 4.3\,\text{V}$, and HF switching frequency $f_{sw} = 100\,\text{kHz}$.

The ac variables, v_g and i_g, are rectified using the polarity signal $plrty$. The inner current control loop is designed with a crossover frequency of $10\,\text{kHz}$ and a phase margin of $60°$. The outer control loop is designed for a crossover frequency of $1.6\,\text{Hz}$.

The conventional implementation uses a ZCD with a symmetrical hysteresis band, i.e., $V_h = 10\,\text{V}$, which provides the $plrty$ signal. Additionally, the scheme shown in Fig. 3 is used to obtain V_g. The first-order low-pass filter (LPF) utilized has a nominal cutoff frequency of $4.6\,\text{Hz}$, dynamically adjusted by the edges of the ZCD.

The proposed implementation, based on a SOGI-FLL (Fig. 4), uses $K_{SOGI} = 1.4142$ and $\gamma_{FLL} = 0.0001$.

Tests have been conducted using harmonically distorted grid voltages with $4\,\%$ 5^{th} and $3\,\%$ 7^{th} harmonics, resulting in a total harmonic distortion of the grid voltage (THD_v) of $5\,\%$. The relative phases of these harmonics are $117.6°$, displacing v_g and fundamental zero-crossings by $3.6°$. In order to compare the performance, the total harmonic distortion of the grid current (THD_i) is evaluated up to the 50^{th} harmonic. Additionally, the fundamental power factor (PF_1) and the total power factor (PF) are considered, as specified in IEEE standard 1459 [16]. These parameters provide insights into the efficiency and quality of the power conversion process.

A. Steady-state results with harmonically distorted grid voltage

In steady-state, under harmonically distorted grid voltage conditions, both implementations demonstrate similar performance, as depicted in Fig. 5. The ZCD-based implementation accurately evaluates the rms value of the grid voltage, resulting in a value of $230.4\,\text{V}$ with zero ripple. In contrast, the FLL-based implementation yields an average value of $230.2\,\text{V}$ with a maximum ripple of $3.67\,\text{V}$. Both controller implementations result in a peak grid current of $4.76\,\text{A}$. However, during v_g zero-crossings, the ZCD-based implementation exhibits a transient overcurrent of $1.78\,\text{A}$ while $1.23\,\text{A}$ for the FLL-based, as illustrated in Fig. 5.b. Figure 5.c demonstrates that the ripple of v_o is similarly asymmetric in both implementations.

According to Fig. 6, both controller implementations exhibit similar performance in terms of PF and PF_1. However, the

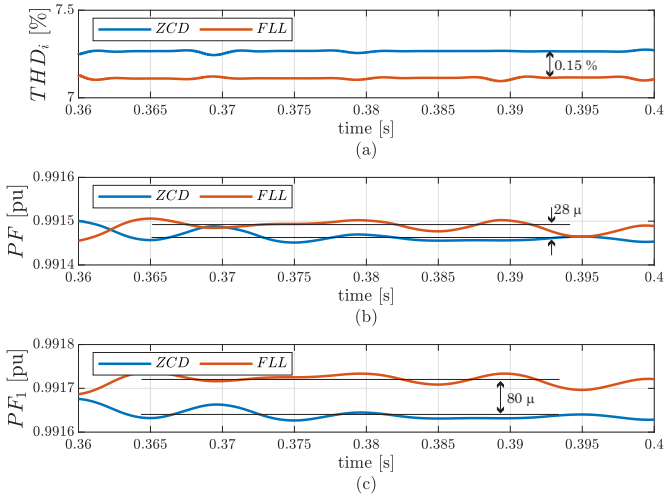

Fig. 6: Steady-state results with harmonically distorted grid voltages. a) THD_i, b) PF, and c) PF_1.

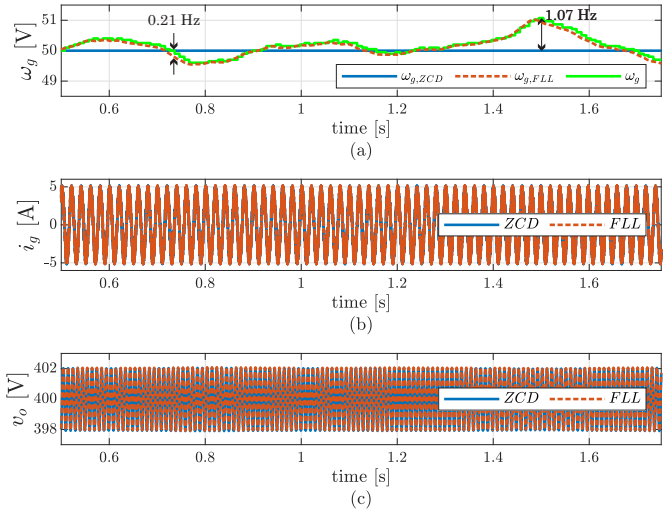

Fig. 7: Grid frequency variations with pure sinusoidal grid voltage. a) grid voltage, b) grid current, and c) output voltage.

proposed implementation based on the SOGI-FLL results in a $0.15\,\%$ lower THD_i than the conventional implementation.

B. Grid frequency variations with pure sinusoidal grid voltage

In the case of a random frequency profile, as depicted in Fig. 7.a, with a pure sinusoidal grid voltage, the ZCD implementation fails to track accurately the applied frequency, ω_g, exhibiting a maximum error of $1.07\,\text{Hz}$. On the other hand, the SOGI-FLL implementation shows faster and more accurate frequency tracking, with a maximum error of $0.21\,\text{Hz}$. However, as observed from the input current in Fig. 7.b and the output voltage in Fig. 7.c, both implementations perform similarly in this scenario.

According to Fig. 8.a, the conventional implementation generally exhibits a higher THD_i than the proposed implementation, with a maximum difference of $1.93\,\%$. Additionally, the effects of grid frequency excursions over time are more

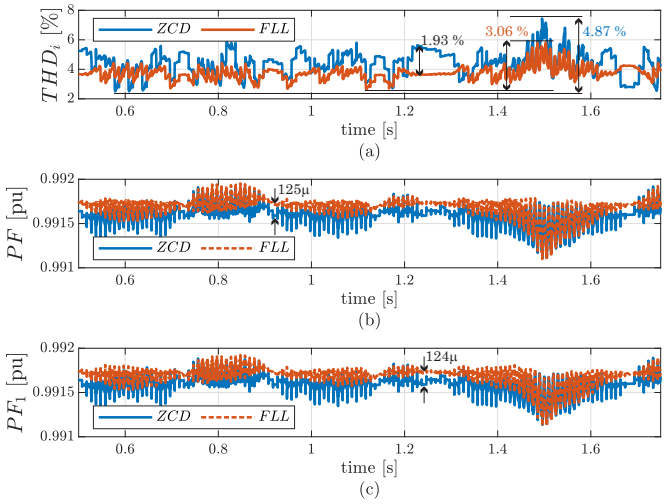

Fig. 8: Grid frequency variations with pure sinusoidal grid voltage. a) THD_i, b) PF, and c) PF_1.

significant for the conventional implementation, resulting in a maximum THD_i variation of $4.87\,\%$, whereas the proposed implementation shows a lower variation of $3.06\,\%$. Similar to the previous test, the proposed implementation demonstrates slightly better performance regarding the power factors (PF_1 and PF).

C. Slow voltage dip with harmonically distorted grid voltage

When a slow voltage dip ($\pm 0.69\,\text{V}\,\text{ms}^{-1}$) is applied to the harmonically distorted grid voltage, the proposed implementation demonstrates faster stabilization of V_g values, achieving stability after $6\,\text{ms}$, as shown in Fig. 9.a. In contrast, the conventional implementation takes significantly longer, requiring $196.5\,\text{ms}$ to stabilize. As a result of this difference, the conventional implementation experiences an increase in the peak input current by $300.8\,\text{mA}$ after the falling transient, as depicted in Fig. 9.b. On the other hand, the proposed implementation exhibits lower effects from this transient, leading to a $1.16\,\text{V}$ reduction in the peak output voltage, as shown in Fig. 9.c.

During the voltage dip, the proposed implementation achieves a $0.69\,\%$ reduction in THD_i compared to the conventional implementation. Additionally, similar to the previous test, the proposed implementation exhibits lower variation in THD_i throughout the test, with values of $3.15\,\%$ for the conventional implementation and $2.51\,\%$ for the proposed one, as shown in Fig. 10.a. Once again, the proposed implementation shows slightly improved performance in terms of power factors.

D. Slow voltage variations with pure sinusoidal grid voltage

Both implementations have been subjected to slow voltage variations of the grid voltage, ranging from $185\,\text{V}$ to $250\,\text{V}$ at a frequency of $2.27\,\text{Hz}$, with a maximum slope of $325\,\text{V}\,\text{s}^{-1}$. In Fig. 11.a, the conventional implementation fails to accurately track the amplitude variations, resulting in a $4.85\,\text{V}$ lower V_g

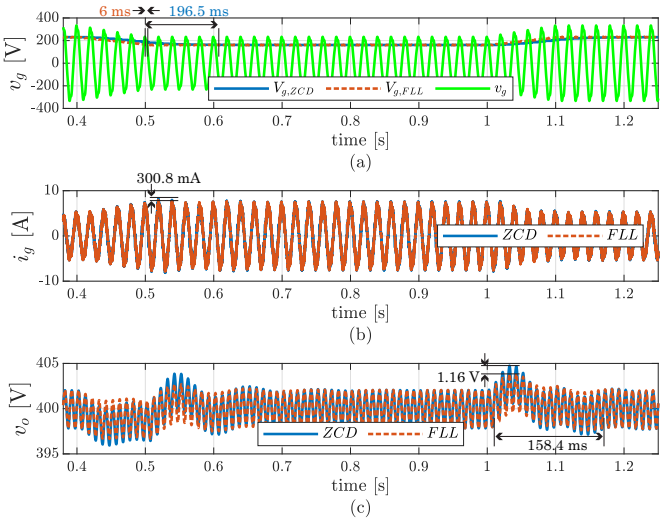

Fig. 9: Slow voltage dip with harmonically distorted grid voltage. a) grid voltage, b) grid current, and c) output voltage.

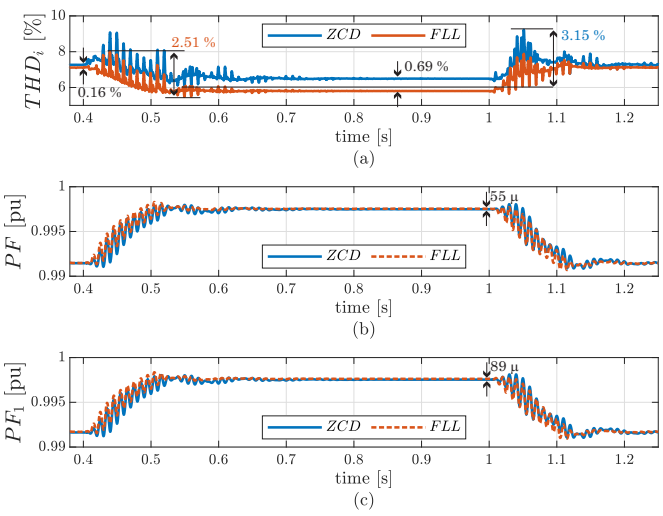

Fig. 10: Slow voltage dip with harmonically distorted grid voltage. a) THD_i, b) PF, and c) PF_1.

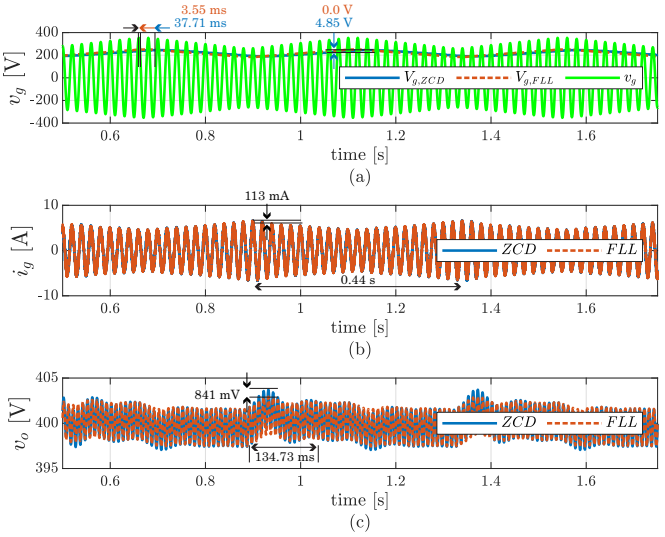

Fig. 11: Slow voltage variations with pure sinusoidal grid voltage. a) grid voltage, b) grid current, and c) output voltage.

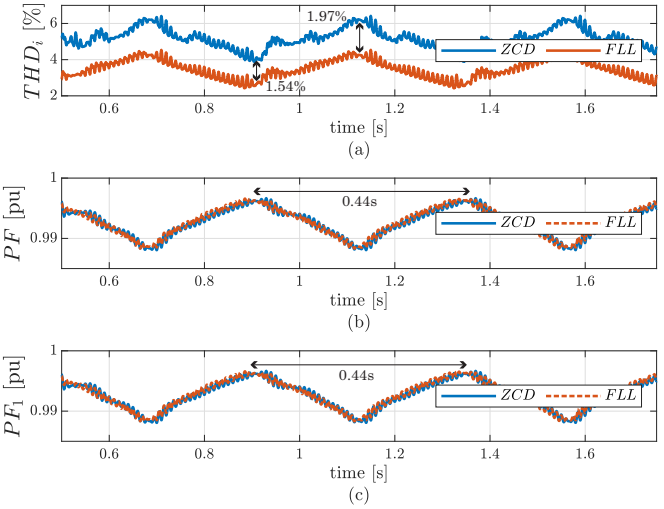

Fig. 12: Slow voltage variations with pure sinusoidal grid voltage. a) THD_i, b) PF, and c) PF_1.

value. Furthermore, the response of the conventional implementation is delayed by 37.71 ms, while the proposed implementation exhibits a smaller delay of only 3.55 ms. These discrepancies affect both the outer and inner control loops, resulting in significant differences in the amplitude of the input current. Specifically, the conventional implementation exhibits a 113 mA higher amplitude of i_g than the proposed implementation, along with 841 mV higher peak values of v_o. Moreover, the conventional implementation displays larger transients of v_o, lasting 134.73 ms, as illustrated in Fig. 11.c.

As a result of the observed differences, the THD_i patterns, depicted in Fig. 12.a, exhibit distances in the range of [1.54 %, 1.97 %], with lower values for the proposed implementation. Slight variations are also apparent in the PF and PF_1 values.

IV. Conclusion

Digital control of single-phase bridgeless totem-pole (TP) power factor correctors (PFC) using rectified ac variables offers advantages by leveraging established control strategies from PFCs with diode-bridge front-end. However, grid voltage disturbances that propagate through the polarity detection and RMS calculation block can negatively impact the input current and output voltage. This occurs because the outer voltage loop must compensate for the effects of these disturbances across the hysteresis band of the zero-crossing detector (ZCD) and the low cutoff frequency of the low-pass filter (LPF) utilized.

In this study, these issues have been evaluated and addressed by the utilization of a second-order generalized integrator (SOGI) with a frequency-locked loop (FLL), known as the SOGI-FLL. This approach significantly improves the converter

dynamics by providing a faster and more accurate estimation of the grid voltage during transients and slow variations.

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