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On the Thermal Degradation of Tunnel Diodes in Multijunction Solar Cells

Ignacio Rey-Stolle[1,2,a)], Iván García[1], Enrique Barrigón[1,3], Javier Olea[4], David Pastor[4], Mario Ochoa[1], Laura Barrutia[1], Carlos Algora[1], Wladek Walukiewicz[2]

[1] *Instituto de Energía Solar, Universidad Politécnica de Madrid, Madrid, Spain*
[2] *Materials Science Division, Lawrence Berkeley National Lab., Berkeley, CA, USA*
[3] *Present address: Solid State Physics, Lund University, Lund, Sweden*
[4] *Facultad CC. Físicas, Universidad Complutense de Madrid, Madrid, Spain*

[a)] Corresponding author: ignacio.reystolle@upm.es

Abstract. Tunnel junctions are essential components of multijunction solar cells. These highly doped p/n junctions provide the electrical interconnect between the subcells that constitute a multijunction solar cell device. The conductivity and the peak tunneling current of tunnel diodes are known to be severely affected by thermal load. This is a general phenomenon observed in tunnel junctions despite the materials used, the dopants employed or the growth technique applied. Despite this generality, the explanations for this thermal degradation tend to be quite material/dopant specific. On the contrary, in this work we apply the amphoteric native defect model to explain this issue. In this context, the degradation can be explained as a consequence of the net loss of free carrier concentration produced by the creation of native compensating defects in the highly doped layers of the tunnel junction. Experiments carried out on n^{++} GaAs agree well with the model.

INTRODUCTION

Tunnel diodes –also termed tunnel junctions– are used as transparent low-resistive interconnects between subcells in monolithic multijunction solar cells [1-3]. The attractive feature of tunnel junctions is that at low bias they exhibit a linear resistor-like *J-V* dependence characterized by the tunnel junction equivalent resistance or zero-bias resistance (r_{eq}). This linear behavior continues in forward bias until the so-called peak tunneling current density (J_p) is reached (see Figure 1). This ohmic region in the *J-V* curve is essential for low-loss electrical interconnects between the subcells. In the particular case of CPV applications, this holds true with the additional requirements that r_{eq} has to be low enough so as not to add a significant contribution to the series resistance of the devices and J_p has to be high enough in order not to limit the circulation of the large current densities produced under concentrator operation [1].

However, it is widely reported that tunnel junctions thermally degrade when grown within a multijunction solar cell. In essence, the thermal load associated to the growth of the upper layers will produce an increase in r_{eq} and a decrease in J_p [1]. An example of such is depicted in Figure 1, where the performance of *as-grown* and thermally annealed tunnel junctions is compared for two representative cases, namely, 1) a p^{++}AlGaAs:C/n^{++}GaInP:Te tunnel diode, which would be typical for a top-cell/middle cell connection, and 2) a p^{++}GaAs/n^{++}GaAs tunnel diode, which would be commonplace for a middle-cell/bottom-cell connection.

The fact of the matter is that similar thermal degradation has been observed in tunnel junctions regardless of the particular material combination used in anode and cathode (pGaAs/nGaAs, pAlGaAs/nGaAs, pAlGaAs/nGaInP, pGaAsSb/nGaInAs, …) and for a number of p-type (Zn, Be, C) and n-type (S, Si, Te, Se) dopants. This fact seems to suggest that the root cause behind this phenomenon is neither material specific nor dopant specific. Conversely,

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the explanations found in the literature to account for such thermal degradation tend to be quite material/dopant specific. For instance, it is often argued that the thermal load brings about the diffusion of the dopants out of the anode and/or cathode layers with subsequent smearing of doping profiles at the tunnel junction [2]. Despite the fact that this has been observed in some specific cases, where tunnel diodes were grown using fast diffusers as dopants (Zn) [2], thermal degradation is also observed in other designs that use very slow diffusers (C, Te, Se) where no evidence of diffusion could be found after the thermal treatments [1] [3]. Another hypothesis states that thermal annealing passivates or modifies key traps that are responsible for the trap-assisted tunneling mechanism. However, this seems difficult to marry with the fact that similar thermal degradation is observed in tunnel junctions grown both by MBE and MOVPE using a wide variety of materials and dopants. Traps and defects tend to be linked to a particular growth technique, material and dopant combination and therefore it would be surprising that different approaches always yielded traps at the right energy level and concentration in *as-grown* material, which would in turn be quenched, passivated or altered after a thermal load is applied.

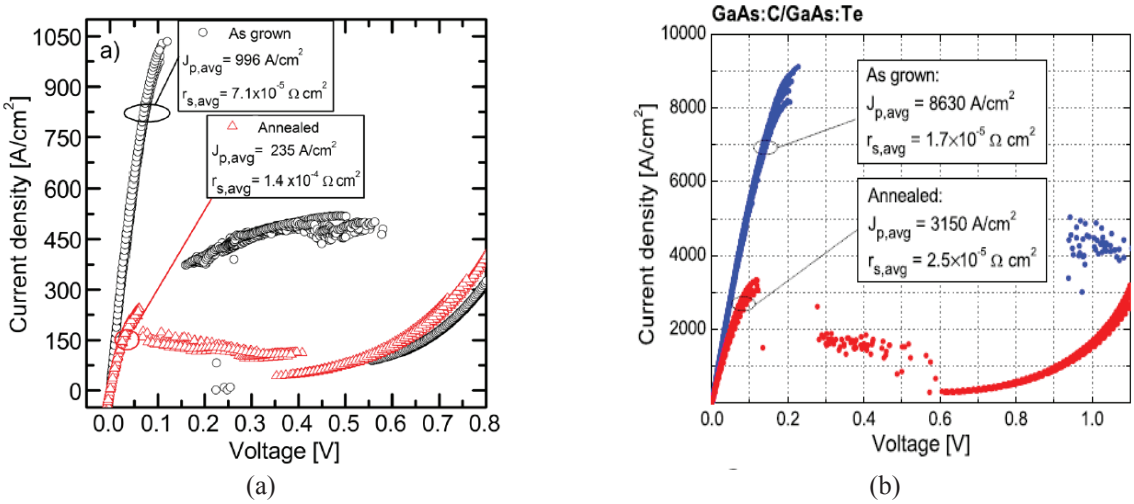

FIGURE 1. (a) *J-V* measurements of p^{++}AlGaAs/n^{++}GaInP tunnel diodes *as-grown* (black circles) and after thermal annealing at 675ºC for 30 min (red triangles) [1] (b) *J-V* measurements of p^{++}GaAs/n^{++}GaAs tunnel diodes as-grown (blue circles) and after thermal annealing at 675ºC for 30 min (red circles) [3]. In both graphs, several devices of the same type have been plotted to give an idea of the device-to-device variability. The values of J_p and r_{eq} included as labels are the averages among the measurements. The shape of the curve beyond J_p, corresponds to the negative resistance region (not clearly observable in some of these examples because of oscillations in the power supply) followed by the typical Shockley dependence.

All this evidence seems to suggest that thermal degradation of tunnel diodes is still not adequately understood. And this fact is relevant because the push for higher solar cell efficiencies is driving up the number of subcells in multijunction devices from 3 to 4, 5 or even 6. This extends the length of the growth processes and thus the impact of the thermal load on the tunnel junctions grown first. On top of this, possibly new high bandgap materials in the tunnel junctions will need be incorporated in the new tunnel junctions to be devised for such 5J and 6J designs. In addition, the use of some key new materials, that are to be incorporated in some 4-junction solar cells, will boost the thermal load of the processes. Particularly, 1-eV diluted nitride alloys (GaInAsNSb) need to be annealed to improve their photovoltaic performance thus increasing significantly the thermal budget of the mere epitaxy [4]. .

Accordingly, the main goal of this work is to present a new approach to understand the thermal degradation of tunnel junctions, which is based on the so-called amphoteric native defect model [5, 6]. This model is neither material specific nor dopant specific and thus could provide a more general framework to understand this phenomenon. To this end, in this paper we briefly introduce the amphoteric native defect model; we then discuss its application to a basic tunnel junction design based on a p^{++}GaAs/n^{++}GaAs; then we conduct a series of thermal degradation experiments on GaAs to confirm the trends described by the model; and to conclude we simulate the impact that such thermal load would cause on a tunnel junction.

THE AMPHOTERIC NATIVE DEFECT MODEL APPLIED TO TUNNEL JUNCTIONS

All semiconductors contain native point defects such as vacancies, interstitials as well as anti-sites, in the case of compound semiconductors. The precise amount of each of these will depend on a number of factors such as the growth technique, the process conditions (specially the temperature) and the precursors used, just to name a few. Once created in the crystal, if energy is available, these native defects may interact and undergo a number of transformations following different reaction paths given by a vast family of possible Frenkel reactions. Of particular interest among these transformations are those that represent amphoteric reactions. To illustrate this concept let us consider the case of GaAs and the following reactions:

$$V_{As}^{3+} + As_{\mathrm{Ga}} + 3e \leftrightarrow As_{As} + V_{Ga}^{3-} \quad (1)$$

$$V_{As}^{3+} + Ga_{Ga} + 3e \leftrightarrow Ga_{As} + V_{Ga}^{3-} \quad (2)$$

Reaction (1), when going from left to right, represents the formation of a gallium vacancy from the recombination of an arsenic vacancy and an arsenic anti-site. Reaction (2), when going from left to right, represents the formation of a gallium vacancy and a gallium anti-site from the combination of an arsenic vacancy and a gallium atom. Obviously, just the opposite process occurs in each case when the reactions run from right to left. In both reactions (1) and (2), we have considered that –according to first principle calculations [5]– the most likely ionization state for each vacancy is 3, so we have triply negatively charged gallium vacancies (V_{Ga}^{3-}) and triply positively charged arsenic vacancies (V_{As}^{3+}). A key point to note here is that the formation of V_{As}^{3+} at the left side of both reactions requires the release of three electrons (or the capture of three holes), therefore V_{As}^{3+} acts as a triple donor. Similarly, the formation of V_{Ga}^{3-} at the right side of both reactions requires the capture of three electrons (or the release of three holes), therefore V_{Ga}^{3-} acts as a triple acceptor. Therefore, reactions (1) and (2) are amphoteric since they can produce either donors or acceptors. It is important to note that because of the high charge state of the defects involved in the reactions (1) and (2) the formation energy of the defects very strongly depends on the Fermi energy.

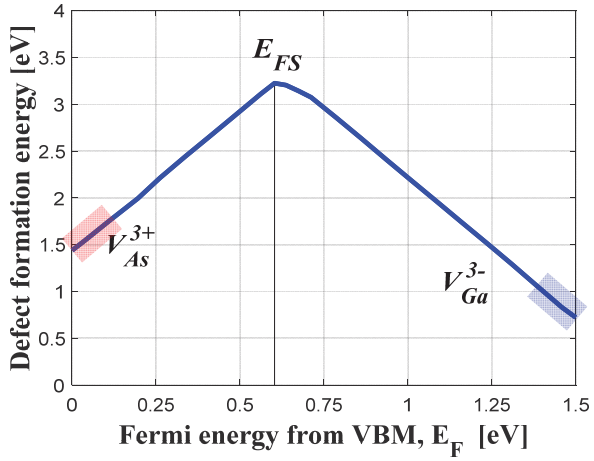

FIGURE 2. Minimum defect formation energies for the native defects involved in reactions (1) and (2) [5]. The label next to each line indicates what defect is formed in each portion of the curve. The part shaded in blue in the line at the right of the graph corresponds to the formation energy of a triply charged gallium vacancy in n^{++}GaAs in the doping range used in tunnel junctions. Analogously, the part shaded in pink in the line at the left in the graph corresponds to the formation energy of a triply charged arsenic vacancy in p^{++}GaAs in the doping range used in tunnel junctions.

The amphoteric native defect model devised by Walukiewicz [5, 6] states that native defect concentration and defect reactions are controlled by the location of the Fermi energy in the semiconductor measured with respect to an internal energy reference, the so called Fermi level stabilization energy (E_{FS}). Again for the case of GaAs, this is

illustrated in Fig. 2, where we plot the minimum defect formation energy needed to create one of the native defects involved in reactions (1) and (2) [5]. Fig.2 is divided in two different regions by the Fermi level stabilization energy (E_{FS}), which in the case of GaAs is ~0.6 eV above the valence band maximum (VBM). In the left section of Fig.2, that corresponds to GaAs samples in which the Fermi level is near the valence band (i.e. p-type GaAs), the defect that requires the least amount of energy to be formed is V_{As}^{3+}, so reactions (1) and (2) would run from right to left if energy is made available. On the contrary, In the right section of Fig.2, that corresponds to GaAs samples in which the Fermi level is near the conduction band (i.e. n-type GaAs), the defect that requires the least amount of energy to be formed is V_{Ga}^{3-}, so reactions (1) and (2) would run from left to right if energy is made available. Obviously, in the vicinity of E_{FS}, the formation of both defects needs a similar amount of energy and there will be a dynamic equilibrium in reactions (1) and (2).

The mechanism just described lays the foundation of an explanation to what occurs in a tunnel junction when submitted to elevated temperatures. Again, basing our discussion on GaAs, let us consider what should occur to a p^{++}GaAs/n^{++}GaAs tunnel junction (Fig 1.b) in the light of the defect properties shown in Fig 2. Starting in the n^{++}GaAs cathode we could assume that the material *as-grown* is highly doped for kinetic reasons. In the case of the device of Fig 1.b the electron concentration was $N_D = 3 \cdot 10^{19}$ cm^{-3}. Under this circumstances, the semiconductor reaches degeneracy and the Fermi level lies very close (or even within) the conduction band. This situation corresponds to a low formation energy for a V_{Ga}^{3-} (triple acceptor), as is illustrated with the blue shaded area in Fig. 2. In other words, ultra high n-doping provides the best conditions for the rapid generation of compensating acceptors. Thereby, as energy is made available in the form of thermal load in the process, compensation rapidly evolves decreasing the net electron concentration in the n-GaAs cathode. This in turn causes the Fermi energy to move away from the conduction band and hence increases the energy needed to form new compensating acceptors (i.e. we move along the line uphill). Accordingly, the compensation process should start vigorously in n^{++}GaAs but should weaken when the electron concentration goes down and the Fermi energy falls below the conduction band edge. Qualitatively, analogous arguments could be used to describe what takes place in the p++GaAs anode, with the compensation driven by the generation of V_{As}^{3+} triple donors. However, Fig. 2 reflects an inherent quantitative asymmetry between n-GaAs and p-GaAs: the minimum defect formation energy for a compensating donor is ~1.5 eV, virtually double than the minimum defect formation energy for a compensating acceptor (~0.75 eV). In other words, compensation is much cheaper (in terms of energy) in n-type GaAs than it is in p-type GaAs. This is so because E_{FS} is closer to the valence band in this material. This fact has been suggested to explain why it is easier to reach significantly higher dopings in p-type than in n-type GaAs [6].

Overall, Fig. 2 sketches a mechanism that will lower the net effective concentration of free carriers in the cathode (mostly) and anode of a GaAs tunnel junction. Evidently, the connection to tunnel junction thermal degradation is straightforward: a lower effective doping in the junction produces higher barrier widths and therefore directly affects the tunneling probability, reducing the diode peak tunneling current.

Finally, it is important to note that Fig. 2 is not dopant specific. Therefore, no matter what dopants we use in the tunnel junction, the generation of V_{Ga}^{3-} and V_{As}^{3+} will be just driven by the position of the Fermi level. On the other hand, Fig. 2 is specific for GaAs. Anyhow, amphoteric native defect reactions analogous to (1) and (2) occur in all III-V semiconductors and thus equivalent plots could be calculated for other materials. Obviously, depending on the position of E_{FS} in each material and on the formation energies of different defects the quantitative evolution of the phenomena might differ but the qualitative trends described should still be valid.

THERMALLY INDUCED LOSS OF CONDUCTIVITY IN n^{++}GaAs AND SUBSEQUENT TUNNEL JUNCTION PERFORMANCE

The anode and cathode of tunnel diodes are very thin (~15 nm) layers, which makes it extremely challenging to study their conductivity and defects. As a result of this and to provide some experimental evidence to validate the predictions of the tunnel-junction thermal degradation model described in the last section, some experiments were carried out on n++GaAs layers. In particular, we grew by MOVPE n++GaAs layers, with a thickness of 1μm, doped with Te to a level of $N_D = 1.2 \cdot 10^{19}$ cm^{-3}, on semi-insulating GaAs substrates. The growth time for these layers was 20 min. and the growth temperature was 550ºC as for the *real* tunnel junctions. We focused our attention on n++GaAs since the model predicts that the compensation process should be clearly more intense than in p++GaAs. After growth, these structures were annealed at 675°C, which is the nominal temperature of our baseline triple junction

solar cell process, in the MOVPE reactor for 15, 30 and 60 min. We conducted the anneals under AsH_3 overpressure to avoid GaAs surface decomposition. Subsequently, changes in the electrical properties of the samples were analyzed by Hall-Van der Pauw measurements.

Fig 3 shows the evolution of the average free electron concentration and mean mobility as a function of annealing time at 675°C for the samples. Figure 3.a shows that free carrier concentration decreases over annealing time and so does mobility (Fig. 3.b). As the annealing time increases, smaller rates of decline in mobility and carrier concentration are observed, suggesting a possible (not checked) saturation of the phenomenon for annealing times longer than 60 minutes. The values of mobility obtained for non-annealed samples (μ=1.250 $cm^2/V \cdot s$) are in perfect agreement with values reported in the literature for heavily doped n^{++}GaAs:Te with similar carrier concentrations grown by MOVPE [7] indicating that the quality of the material grown is comparable to other studies.

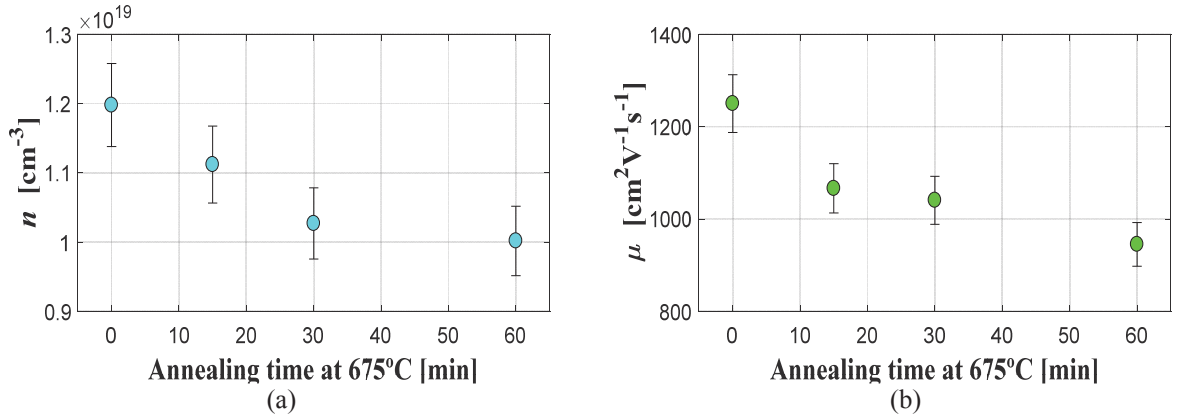

FIGURE 3. Evolution of free electron concentration (a) and Hall mobility (b) in n++GaAs (tunnel diode cathode) versus annealing time at 675ºC. A net loss of free electrons is observable, which indicates the presence of a compensation mechanism triggered by temperature, which manifests itself as a drop in mobility. As indicated in the text, these test structures were 1 μm thick n++GaAs layers.

TABLE 1. Characteristics of the tunnel junctions simulated

	TJ ***as-grown***	**TJ annealed 30min @ 675C**
Net dopant concentration in p^{++}GaAs anode [cm^{-3}]	7×10^{19}	7×10^{19}
Thickness of p^{++}GaAs anode [nm]	20	20
Net dopant concentration in n^{++}GaAs cathode [cm^{-3}]	3×10^{19}	2.5×10^{19}
Thickness of $^{n++}$GaAs cathode [nm]	15	15
Simulated tunneling width [nm]	6.2	6.6
Peak tunneling current [A/cm^2]	8.630*	2.290

* This value fixed and used to calculate the constants of the model

The results of Fig. 3 are consistent with the predictions of the model. Free carrier concentration decreases with annealing time and this decline comes with a parallel loss in mobility, which is a sign of compensation. In addition, this decline seems to lose vigor with annealing time. For instance, for samples annealed for 30 min, the loss in net

free electron concentration is of 15%, whereas the loss in mobility is of 17%. If we go back to Fig 1.b, it is precisely an annealing of 30 min what causes the big difference in peak tunneling current – from 8.630 to 3.150 A/cm^2, a factor of ~2.7– between the two tunnel junctions presented in this figure. Therefore, an obvious question that arises is if the decline observed in net n-type doping can justify a loss by almost a factor of three in J_p. To answer this question we followed the semi-analytical simulation approach for tunnel junctions described in [8], and applied it to the tunnel junction structures included in Table 1. As this table shows, for the *as-grown* tunnel junction we assumed the structural parameters described in [3]. For the *annealed* tunnel junction, we assumed that the only parameter changing is the net electron concentration at the cathode. We assumed a drop of 20% (to $2.5 \cdot 10^{19}$ cm^{-3}) to account for the fact that compensation should be more intense in the case of tunnel junctions –as compared to the experiments in Fig. 3–because the starting free electron concentration is higher (~$3 \cdot 10^{19}$ cm^{-3}).

We solved numerically Poisson's equation for each of the designs in Table 1, using Snider's Poisson solver [9]. In this way, we obtained the band diagrams and tunneling widths in each case, as indicated in Table 1. Then the experimental J_p of the as-grown design was used to determine the constants in the analytical expressions described in [8]. Finally, we used those expressions to calculate the peak tunneling current of the annealed tunnel junction. The calculated value of 2.290 A/cm^2 is ~35% lower than the experimental result of Fig. 1. This is a good agreement given the simplicity of the model used and the number of simplifications made and it provides indirect evidence that the compensation of heavy n-type doping by amphoteric defects is responsible for the temperature induced degradation of the conductivities of tunnel junctions.

More accurate simulations with fully numerical models as well as similar experiments for p^{++}GaAs, p^{++}AlGaAs and n^{++}GaInP, will be conducted to further test the validity and universal nature of this model.

CONCLUSIONS

Thermal degradation of the conductivity of tunnel junctions is an important phenomenon that affects current and future designs of multijunction solar cells. The existing explanations for the degradation process remain material and/or dopant specific despite such degradation has been observed in all tunnel diodes, regardless of the materials and dopants used. In the search for a more general explanation, in this paper we have proposed for the first time a degradation model that is neither material specific nor dopant specific. This model is based on the amphoteric native defect model that postulates that the generation of compensating native defects is controlled by the localization of the Fermi energy, becoming energetically favored (vigorously) in highly doped materials. In this context, the degradation in tunnel junctions can be explained as the result of the net loss of free carrier concentration produced by the creation of native compensating defects in the highly doped layers of the tunnel junction. A lower doping in the junction layers, leads to increased tunneling widths that produce a decrease in the peak tunneling current. Experiments on thermal annealing of n^{++} GaAs have indeed shown the decrease in effective doping predicted by the model. In addition, simulations show that the magnitude of such decrease is consistent with the drop in peak tunneling current observed in GaAs tunnel junctions for the same annealing.

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