

Envelope-based Modeling for Single-Phase Grid-Following and Forming Converters

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Abstract— The study of the interaction with the grid, including synchronization, controller design and stability assessment for 1 ϕ grid-following (GFL) and grid-forming (GFM) power converters requires an efficient modeling tool to design universal grid-connected converters considering the different grid scenarios. From the initial time-periodic system, approximated linear time-invariant (LTI) models are obtained through dynamic phasors, linearization of variables represented in a virtual synchronous rotating reference frame (RRF) or linearization in the frequency domain, i.e. harmonic linearization. The accuracy and complexity of the obtained model depend on the method used. This work proposes to use the well-known envelope modeling approach used for resonant converters but requiring the time periodic input to generate its related phase synchronization for the model. The result is a simple and accurate LTI model of 1 ϕ GFL/GFM power converter for such stability studies. The proposed 1 ϕ modeling approach is valid for any application with phase locked loop (PLL) synchronization. Simulation results validating the proposal are provided.

Keywords— *envelope modeling, phase-locked loop, grid-connected power converters.*

I. INTRODUCTION

The electrical energy processed through power electronics in both low-voltage (LV) and medium-voltage (MV) grids is growing due to the increasing penetration of renewable energy sources, distributed storage systems and non-linear loads, e.g. electric vehicles [1], [2]. Stability studies are challenging due to the characteristics of grid-following (GFL) and grid-forming (GFM) power converters used and the diversification of scenarios [3]. To simplify these studies, analysis techniques associated with linear time-invariant (LTI) systems are preferred; but approximating time-varying systems with LTI methods, while retaining the characteristics relevant to these studies, is also challenging [4], [5].

Certain well-established approaches for 3 ϕ GFL and GFM, such as model linearization with variables representation in a synchronously rotating reference frame (RRF) [6] and linearization in the frequency domain through linear time-periodic (LTP) techniques, i.e. harmonic linearization [7], [8], can also be used for 1 ϕ GFL. These techniques evaluate the effect of both the DC-side and the synchronization subsystem, e.g. phase locked loop (PLL), [9], [10]. Alternatively, to the authors knowledge, only the technique based on dynamic phasors is natively 1 ϕ [11], but it is unable to model low-frequency effects due to DC-side dynamics.

Nowadays bridgeless PFC topologies are preferred because they achieve better efficiency than the ones with a

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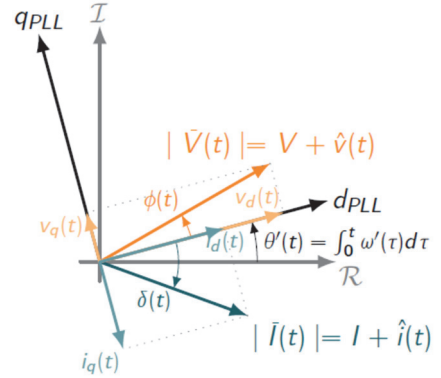


Fig. 1. AC quantities representation for envelope-based modeling.

previous diode bridge stage. With the elimination of the bridge diode, the natural AC current synchronization with input voltage is also eliminated and the AC input to the controller variables acquisition is more challenging. Robust grid synchronization with PLL provides the necessary information to the control circuit to identify the zero crossing AC voltage instant and PLL based algorithms as the delayed signal cancellation technique (DSC) are used to remove unwanted components of the acquired signals [12]. Besides, low bandwidth controllers, i.e. PLL and output voltage control loop need to be evaluated according to grid characteristics and disturbances to compensate for.

This work proposes, for the first time, to use an envelope-based modeling approach to obtain simple and accurate LTI models of 1 ϕ grid-connected converters with a PLL synchronization signal which provides the phase reference to the model for grid interaction and stability studies as well as low frequency bandwidth controller design. It is based on the envelope modeling technique, which has been proved for resonant power converters [13], [14] and is inherently 1 ϕ . The modeling technique is described and validated through simulation.

II. ENVELOPE-BASED MODELING OF 1 ϕ GFL

A. Electrical quantities representation

The envelope-based modeling approach for 1 ϕ GFL - GFM considers that both, the grid voltage, and line current AC quantities can be represented as projections of rotating vectors referred to a complex short-term stationary reference frame,

$$v(t) = \text{Re}\{\vec{v}_{SRF}(t)\}, \quad i(t) = \text{Re}\{\vec{i}_{SRF}(t)\}, \quad (1)$$

with time-varying amplitudes $|\bar{V}(t)|$ and $|\bar{I}(t)|$, respectively.

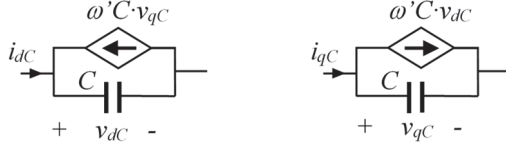


Fig. 2. Large-signal envelope-based model of capacitors.

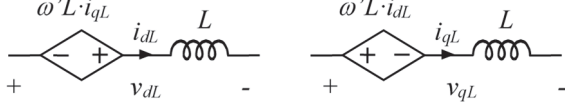


Fig. 3. Large-signal envelope-based model of inductors.

Moreover, it is assumed that although the AC voltage is the independent variable, the output of the synchronization subsystem, PLL, defines a RRF rotating at a time-varying angular frequency ω' . The quote symbol ($'$) denotes a variable estimated by the PLL. Under this assumption, the proposed model incorporates the effect of eventual distortion of the synchronization signal.

The AC quantities in (1) are represented in the RRF defined by the synchronization by means of the grid angle estimation (Fig. 1),

$$\theta'(t) = \int_0^t \omega'(\tau) d\tau. \quad (2)$$

Then, the SRF vectors due to the AC quantities are defined as

$$\vec{v}_{SRF}(t) = |\vec{V}(t)| e^{j(\theta'(t) + \phi(t))} \quad (3)$$

$$\vec{i}_{SRF}(t) = |\vec{I}(t)| e^{j(\theta'(t) + \delta(t))}, \quad (4)$$

where time-varying angles ϕ and δ depend on the relative position of the RRF and voltage and current vectors, respectively.

Following Fig. 1, the RRF representation of (3) and (4) is given by

$$\vec{v}_{RRF}(t) = \vec{v}_{SRF}(t) e^{-j\theta'(t)} = v_d(t) + jv_q(t) \quad (5)$$

$$\vec{i}_{RRF}(t) = \vec{i}_{SRF}(t) e^{-j\theta'(t)} = i_d(t) + ji_q(t), \quad (6)$$

where, d and q subscripts correspond to in-phase and in-quadrature quantities in the RRF, respectively.

These time-varying in-phase and in-quadrature quantities, retaining the whole harmonic spectrum of v and i , can also be represented in the SRF, by

$$\vec{v}_{SRF}(t) = \vec{v}_{RRF}(t) e^{j\theta'(t)} = (v_d(t) + jv_q(t)) e^{j\theta'(t)} \quad (7)$$

$$\vec{i}_{SRF}(t) = \vec{i}_{RRF}(t) e^{j\theta'(t)} = (i_d(t) + ji_q(t)) e^{j\theta'(t)}. \quad (8)$$

B. Modeling passives and switching cells

As in envelope modeling, these AC signal quantities can be used with inductive and capacitive elements, resulting, respectively, in

$$\vec{i}_{SRF}(t) = C \frac{d}{dt} \vec{v}_{SRF}(t) \quad (9)$$

$$\vec{v}_{SRF}(t) = L \frac{d}{dt} \vec{i}_{SRF}(t). \quad (10)$$

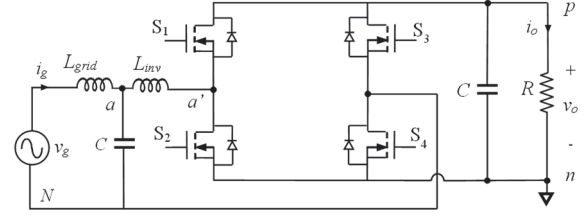


Fig. 4: 1φ totem-pole PFC.

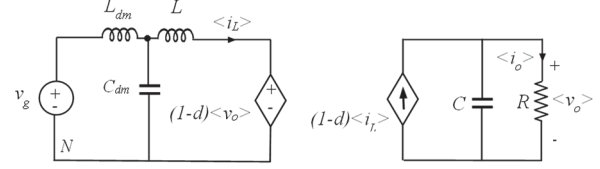


Fig. 5: Average model of 1φ totem-pole PFC.

From (9) and (10), in-phase and in-quadrature components in capacitors and inductors are related through

$$i_d(t) + ji_q(t) = C \frac{d}{dt} (v_d + jv_q) + j\omega'(t)C(v_d + jv_q) \quad (11)$$

$$v_d(t) + jv_q(t) = L \frac{d}{dt} (i_d + ji_q) + j\omega'(t)L(i_d + ji_q). \quad (12)$$

Figures 2 and 3 show the equivalent large signal model obtained from the envelope-based modeling approach (RRF).

C. 1φ totem-pole PFC

The proposed envelope-based approach is used to model the 1φ totem-pole PFC depicted in Fig. 4. Low frequency switches, S_3 and S_4 , act as diodes so the *on* or *off* state depends on the grid voltage polarity and the high frequency branch, S_1 , S_2 , provides three-level PWM at the AC side. Succeeding high frequency components in the line current are filtered out through a LC filter and an accurate zero crossing detection of the grid voltage is needed to achieve a low THD line current [15], [16].

The resulting average model, which is a Boost converter model, is shown in Fig. 5, where d denotes the duty cycle, i.e. $d = t_{on}/T$ for S_2 during the positive grid semi period and for S_1 during the negative semi period. With v_g sinusoidal, $V_o(1-d)$ results in a sinusoidal function in steady state. AC and DC side passive components are kept as it is shown in Fig. 4.

The large-signal envelope-based model, Fig. 6, is obtained by replacing the AC quantities and passives with RRF equivalents and large-signal models in Fig. 2 and Fig. 3, respectively. The average voltage across $a' - N$ corresponds in the RRF to the in phase $(1-d_d) \langle v_o \rangle$ and quadrature $(1-d_q) \langle v_o \rangle$ components in the RRF as represented in Fig. 6. At the DC side, passives remain unchanged. As a result, two AC coupled circuits are obtained to represent the AC side.

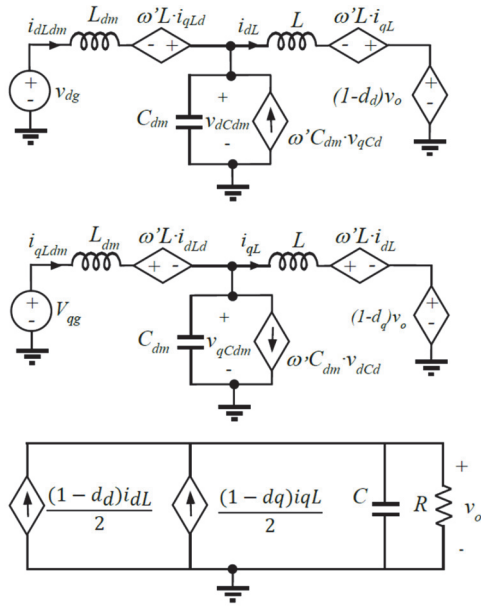


Fig. 6. Large-signal envelope-based model of 1φ totem-pole PFC.

The current injected into the DC side is now composed of two controlled current sources, averaged to ensure power conversion consistency of the magnitudes of the AC and the DC sides. From Fig. 6, the active output power can be evaluated from the inner product of the duty cycle and the line current represented in the RRF, as

$$p(t) = \frac{1}{2} v_o(t) \left\{ (1 - d_d(t)) i_{dL}(t) + (1 - d_q(t)) i_{qL}(t) \right\}. \quad (13)$$

The large-signal model given in Fig. 6 shows that perturbing the load results in model changes while perturbing the grid voltage results not only in PLL but also in model perturbations.

The design of the linear control loops for both for the DC voltage and the AC line current can be carried out following two approaches: i) as usual in 3φ GFL but considering that the vector projections on the imaginary axis (Fig. 1) have no physical meaning, or, ii) for GFM, starting from the plants obtained from the small signal model derived from the envelope-based model. Both approaches are inherently 1φ. Classical inner loop linear current control using $i_{ref} = I_{L,ref} \sin \theta'$ with, $I_{L,ref} = \frac{2p}{V_g}$, p , the power in (13), V_g , the amplitude of the grid voltage and θ' the output of the PLL, results in $i_{qL} \approx 0$. Ideally, in steady state and neglecting the dm filter, with $v_g = V_g \sin(\omega t)$,

$$(1 - d)V_o = V_g \sin(\omega t) - \omega L I_L \cos(\omega t), \quad (14)$$

which corresponds to

$$(1 - d_a)V_o = V_g \quad (15)$$

$$(1 - d_q)V_o = -\omega L \cdot i_{dL} \quad (16)$$

as predicted by the envelope model and averaged models.

III. SIMULATION RESULTS

To validate the envelope-based modeling approach, the switching model of a 1φ totem-pole PFC is modeled in

PLECS® and compared to the envelope-based model in Fig. 6.

The controllers used results from translating the line current and dc voltage control loops, consisting in proportional-integral (PI) controllers [17], plus the PLL to the RRF defined by the PLL. The envelope-based modeling approach is used with two PLLs: a 2S-PLL [18] and a SOGI-PLL [19]. The switched model also considers an adaptive blanking time around grid voltage zero crossings [16], depending on the output load power and the fundamental grid voltage estimation due to the PLL. Simulation parameters are given in Table I.

TABLE I. SIMULATION PARAMETERS

Parameter	Value
Nominal grid frequency, f_0 [Hz]	50
Nominal grid voltage, V_g [V]	230
Switching frequency, f_{sw} [kHz]	65
AC side inductor, L [mH]	1
Parasitic inductor resistance, R_L [mΩ]	500
Output capacitor, C [mF]	248
Nominal DC load, R_o [W]	128
SiC MOSFETs	IMZA65R048M1
Superjunction MOSFETs	IPW60R017C7
Blanking time, T_b [°]	5.4
Reference output voltage, V_o^* [V]	400
PLL settling time, T_{set} [s]	0.2
PLL damping factor, ξ	$\sqrt{2}$
Current loop, crossover frequency, f_c [Hz]	3250
Current loop, phase margin, PM [°]	60
Voltage loop, proportional gain, K_p	0.1
Voltage loop, integral gain, K_i	5

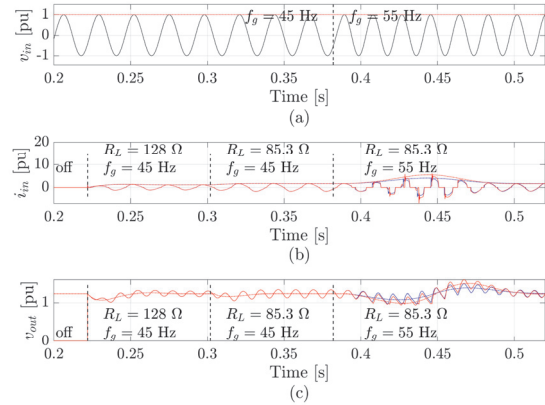


Fig. 7. Switching (solid line) and envelope-based (dashed line) models performance for PLL-2S (blue) and PLL-SOGI (red) under a DC load transient and a frequency step. a) Grid voltage, b) Line current and c) DC voltage. $V_{base} = 230\sqrt{2}$ V, $I_{base} = 5\sqrt{2}$ A.

Fig. 7 shows the results obtained for a DC load transient and a frequency step. The DC load transient, from 128 Ω to 85.3 Ω at 0.295 s occurs before the frequency step, from 45 Hz to 55 Hz. Once the PLLs are locked, the converter starts the operation and the envelope-based model follows the switched model. Both PLLs provide the same RRF voltage across the tests, Fig. 7.a, and the DC load transient results in the same performance for both PLLs, as shown in in Fig. 7.b and 7.c. The subsequent frequency step reveals different

performances, due to the PLLs used. In both cases, the envelope-based model track the switched one and the low frequency characteristics due to the PLL are captured by the envelope-based model. From Fig. 7.b and 7.c, the PLL 2S results in smoother line current and output voltage than the PLL SOGI. For both PLLs, the envelope-based model reveals the frequency step by means of a sudden change in i_{in} and v_{out} . Figure 8 shows the grid angle and frequency estimations due to the PLLs used under the same conditions of Fig. 7. The PLL-2S provides the best grid angle estimation in this test and, therefore, the effect of the frequency step in Fig. 7 is less abrupt than in the case of the PLL-SOGI.

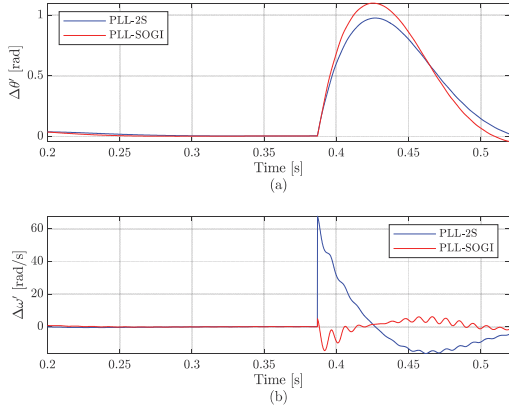


Fig. 8. Errors of the estimated grid angle, θ' , and grid frequency, ω' due to PLL-2S (blue) and PLL-SOGI (red) under a DC load transient and a frequency step. a) Grid voltage, b) Line current and c) DC voltage. $V_{base} = 230\sqrt{2} V$, $I_{base} = 5\sqrt{2} A$.

shown by the envelope-based model. In Fig. 9.c, the output voltage ripple also shifts depending on the PLL used and the effect is tracked by the envelope-based model. Fig. 10 shows the phase and frequency errors due to the PLLs evaluated. In comparison to the frequency step test, both PLLs improve their performances in this test, which can be captured through the envelope-based model in Fig. 9.

The effect of low frequency harmonics on the envelope-based model is also evaluated. Figure 11 shows the results obtained if the grid voltage is polluted by 5th and 7th harmonics, with amplitudes 5% and 3%, respectively. Once the steady state is reached, a DC load transient occurs. From

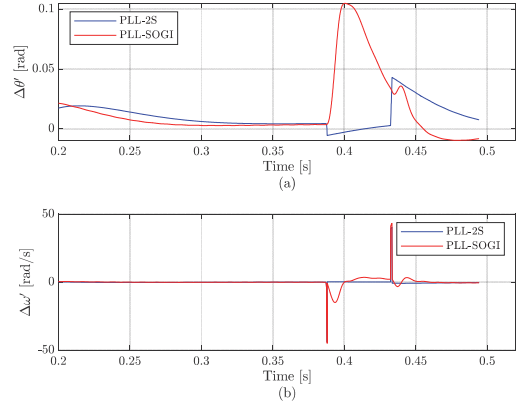


Fig. 10. Errors of the estimated grid angle, θ' , and grid frequency, ω' due to PLL-2S (blue) and PLL-SOGI (red) under a DC load transient and a 50% voltage dip. a) Grid voltage, b) Line current and c) DC voltage. $V_{base} = 230\sqrt{2} V$, $I_{base} = 5\sqrt{2} A$.

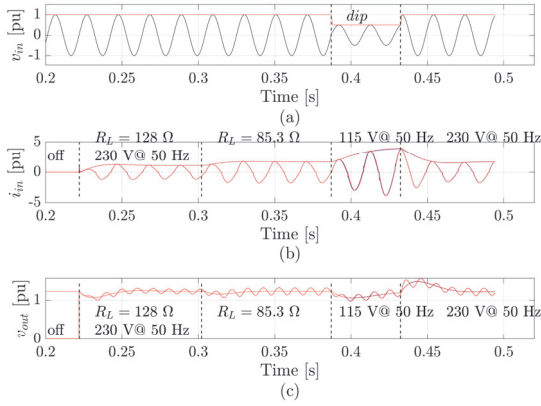


Fig. 9. Switching (solid line) and envelope-based (dashed line) models performance for PLL-2S (blue) and PLL-SOGI (red) under a DC load transient and a 50% voltage dip. a) Grid voltage, b) Line current and c) DC voltage. $V_{base} = 230\sqrt{2} V$, $I_{base} = 5\sqrt{2} A$.

The effect of grid voltage dips is evaluated in Fig. 9 and 10. A pure sinusoidal 230 V 50 Hz grid voltage is used and, following a DC load transient, a voltage dip with 50 % depth and 0.045 s length is occurs. Figure 9.a shows that both PLLs track the voltage dip properly but the differences arise, both in the switched and envelope-based models, for the line current (Fig. 9.b) and the output voltage (Fig. 9.c). The greatest difference is shown in Fig. 9.b, where the SOGI-PLL slightly delays the grid angle estimation (Fig. 10.a) and, consequently, the line current consumption slightly changes in comparison with the totem-pole converter with PLL 2S. This effect is

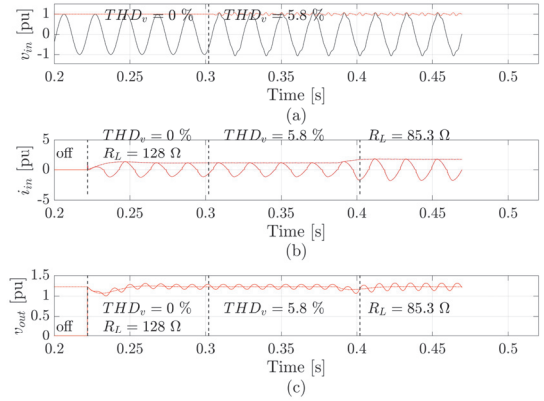


Fig. 11. Switching (solid line) and envelope-based (dashed line) models performance for PLL-2S (blue) and PLL-SOGI (red) under harmonically distorted grid voltages ($THD_v=5.8\%$) and a DC load transient. a) Grid voltage, b) Line current and c) DC voltage. $V_{base} = 230\sqrt{2} V$, $I_{base} = 5\sqrt{2} A$.

Fig. 11.a, the harmonically polluted grid voltage passes through the RRF and, as in the switching model, deteriorates the current waveform, in Fig. 11.b. With the PLLs practically locked (Fig. 12) to the pure sinusoidal grid voltage, the controller is enabled, and the models predicts similar performance. From Fig. 11.b, the voltage harmonics pass through the current controller used, which fails rejecting their effect, specially, at light load. Both PLLs result in similar switched model performances but the PLL-2S exhibits a higher distortion. This effect is also shown by the envelope-

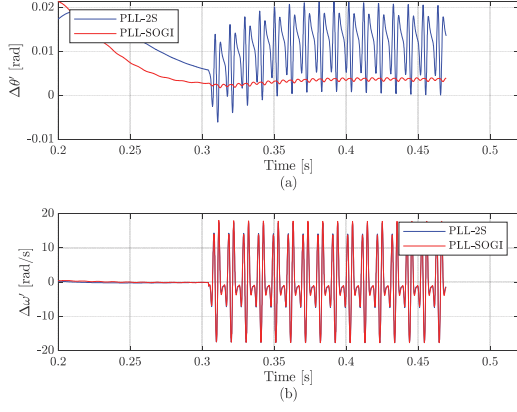


Fig. 12. Errors of the estimated grid angle, θ' , and grid frequency, ω' due to PLL-2S (blue) and PLL-SOGI (red) under harmonically distorted grid voltages ($THD_v=5.8\%$) and a DC load transient. a) Grid voltage, b) Line current and c) DC voltage. $V_{base} = 230\sqrt{2} V$, $I_{base} = 5\sqrt{2} A$.

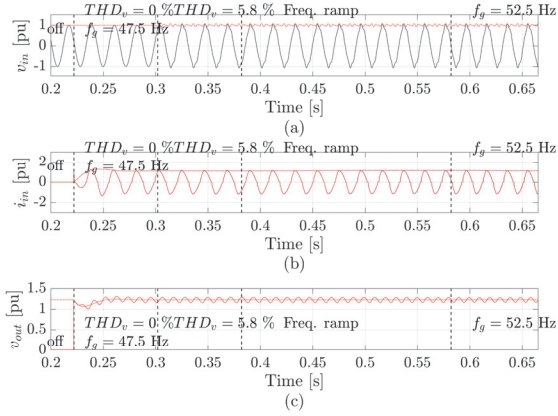


Fig. 13. Switching (solid line) and envelope-based (dashed line) models for PLL-2S (blue) and PLL-SOGI (red) under harmonically distorted grid voltages ($THD_v=5.8\%$) and a frequency ramp (47.5 Hz to 52.5 Hz). a) Grid voltage, b) Line current and c) DC voltage. $V_{base} = 230\sqrt{2} V$, $I_{base} = 5\sqrt{2} A$.

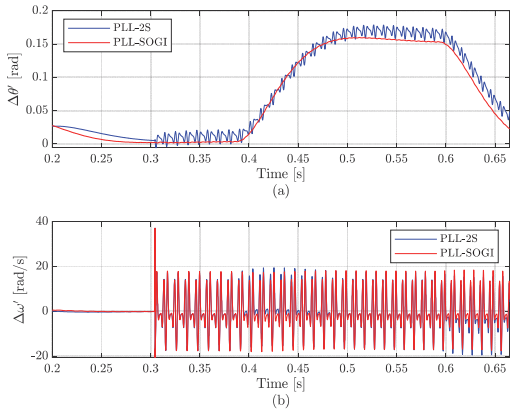


Fig. 14. Errors of the estimated grid angle, θ' , and grid frequency, ω' due to PLL-2S (blue) and PLL-SOGI (red) under harmonically distorted grid voltages ($THD_v=5.8\%$) and a frequency ramp (47.5 Hz to 52.5 Hz). a) Grid voltage, b) Line current and c) DC voltage. $V_{base} = 230\sqrt{2} V$, $I_{base} = 5\sqrt{2} A$.

based model. By increasing the output DC power, the fundamental grid current consumption increases and the harmonic distortion in the line currents decrease. The envelope-based model shows this effect. The output voltage remains unchanged in switched and envelope models using both PLLs, in Fig. 11.c. The performance of both PLLs is shown in Fig. 12, where the low-frequency harmonics has a greatest effect on the 2S-PLL. The harmonic filtering capability of the SOGI-PLL provides a more accurate grid angle estimation (Fig. 12) while the frequency error is similar in both PLLs (Fig. 12.b). These performance differences are translated into the different input current waveforms in Fig. 11.b and the respective envelope-based currents.

The envelope-based modeling approach has also been validated under grid frequency ramps, as shown in Fig. 13, using a +20 Hz/s frequency ramp beginning at 47.5 Hz and with harmonically distorted grid voltage. Figure 13.a shows that the grid voltage translated to the RRF defined by each PLL is maintained during the frequency ramp. According to the switching models, for both PLLs, in Fig. 13.b, the line current amplitude decreases during the frequency ramp, from 6.59 A, at the beginning, to 6.43 A at the end. This figure also shows that the 2S-PLL is faster tracking the ramp, as it is corroborated in Fig. 14. The envelope-based models match the tendency provided by the corresponding switching models. Besides, the current harmonic distortion is reduced during the frequency ramp, and this effect is also revealed by the envelope-based model. The output voltage of the switched model with both PLLs is coincident and agrees with the obtained with the envelope model. Only minor deviations are observed at the beginning and ending instants.

IV. CONCLUSION

This work proposes an envelope-based modeling approach, based on well-known envelope modelling technique in resonant converters, to obtain simple and accurate LTI models of 1 ϕ GFL - GFM for the study of the converter interaction with the grid, synchronization, controller design and stability assessment. The modeling procedure is simple and results in accurate LTI models of 1 ϕ GFL. The concept is verified with a 1 ϕ totem-pole power factor corrector (PFC) simulation model with linear current and voltage control loops and a PLL for synchronization. As it is shown, their utilization with 1 ϕ GFL retains both low-frequency effects due to the DC-side controller and the synchronization subsystem used. The simulation results provided show that the effect of different synchronization subsystems under different grid conditions are tracked by the proposed modeling approach.

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