Final project:
MMIC Envelope detector K-band (22GHz)
Hybrid Envelope detector
S-band (3.5GHz)

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Contents

Part I
MMIC Envelope detector K-band (22GHz)

1 Design purpose

The purpose of the design is to obtain a DC output signal proportional to the input power when there is a single tone signal at the input of the circuit or an envelope when there is a two tone signal instead, so we can make use of it for others systems as for example a bias tuning amplifier as shown in the figure 1. As a multi-purpose device it is desirable a controllable power detector in which we can change the DC output range by tuning some value of the design, as for example the DC bias.

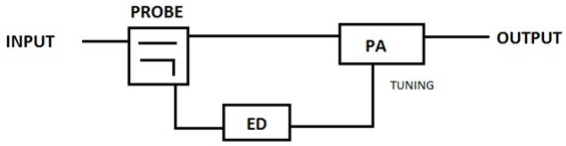

Figure 1: *Schematic of the bias tuning doherty amplifier*

2 Design constraints

The design is developed to work at the K-band frequency (18-27 GHz), namely at 22 GHz. The expected input power is made up of the range between 10 and 20 dBm when the circuit is fed with one tone signal, making the DC output vary 1 volt in the range of [0, –2] Volts depending on the input bias. For example, it is possible set an output from –1 (10 dBm) to 0 (20 dBm) volts using a certain input bias, or instead, an output from –1 to –2 volts for another certain input bias.
When the circuit is fed with a two tone signal the amplitude range expected for each tone varies from 7 to 17 dBm, and it is desirable a bandwidth for the envelope of at least 40 MHz. In order to assure a properly reflection coefficient the parameter S11 should be below –10 dB for the expected input power range and frequency band. The design will be carried out with a GaAs process.

Summary of constraints

- K-band (18-27 GHz) @ 22 GHz
- S11 ≤ -10dB
- Pin $= [10, 20]$dBm
- Variation range of 1 V, around $[0, -2]$ V at the output
- Envelope's bandwidth (2 tone sim.) $\geq$ 40 MHz
- GaAs process

3 Proposed circuit

The starting point is the envelope detector circuit proposed by Zirath[1] shown in the picture 2, in which the author presents an envelope detector consisting in a parallel diode, current biasing through a resistor which forms a low pass filter together with a parallel capacitor, an open stub used to minimize the reflection coefficient and a decoupling capacitor at the input.

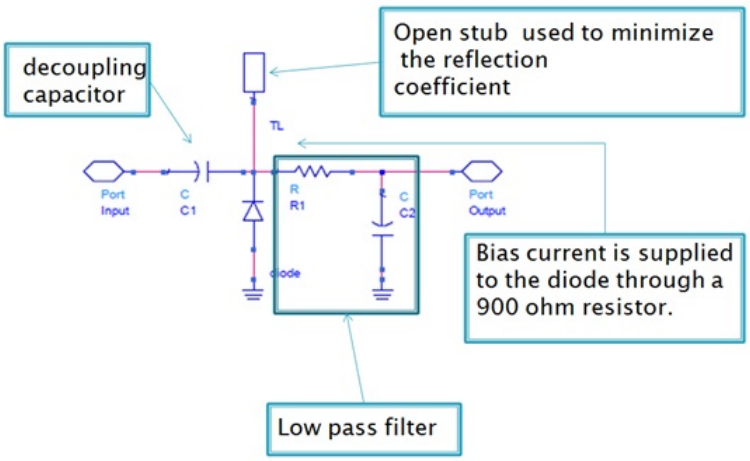

Figure 2: *Zirath's proposed circuit*

4 Carrying out the first design

From the Zirath design, it is developed a first design (figure 3) which consist in the DC decoupling, the parallel diode, the low pass filter (RC filter), an extra resistor (which will be useful later for the transition from current source to the voltage source) and a current source.
The bias current is set by the diode's knee and the first values of the resistors and the capacitor are chosen roughly scaling the Zirath's design values to our frequency (22GHz) and later adjusting them by tuning.

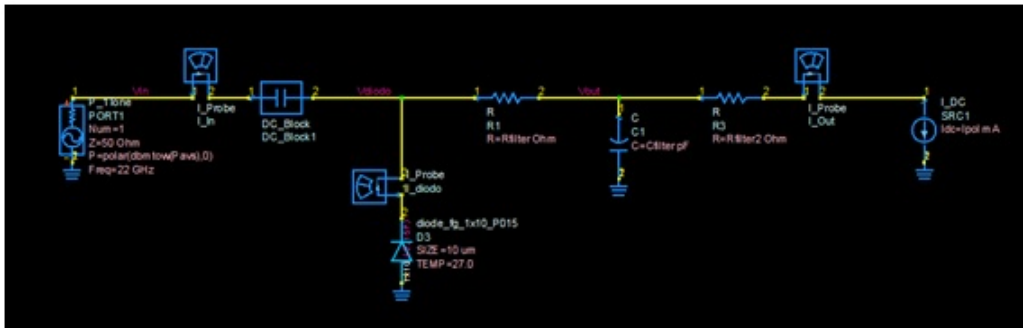

Figure 3: *Schematic of the first design*

4.1 Early results (working at 22GHz)

As early results we obtain a quite linear response at the output and good matching, proving that the circuit works properly.

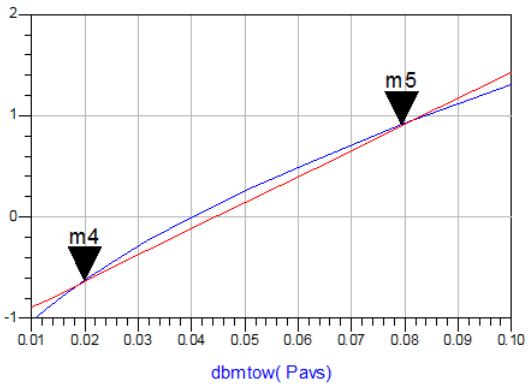

Figure 4: *Output DC vs input power*

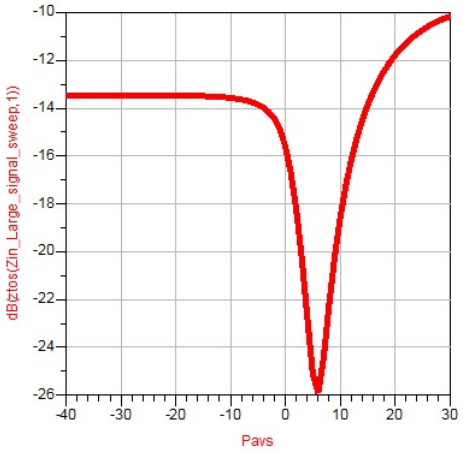

Figure 5: *S11*

5 Diode selection

As the next step, the different kinds of diodes belonging to the technology (different sizes of gate and number of gates) are tested using the topology shown in the previous section, in order to select the one of them which offers us the best performance.
As it is shown in the picture 6 all diodes have a quite similar linearity, though one of them presents a more negative output for the same bias, so this one was chosen as the starting point (1 gate $\times$ 10 μm).

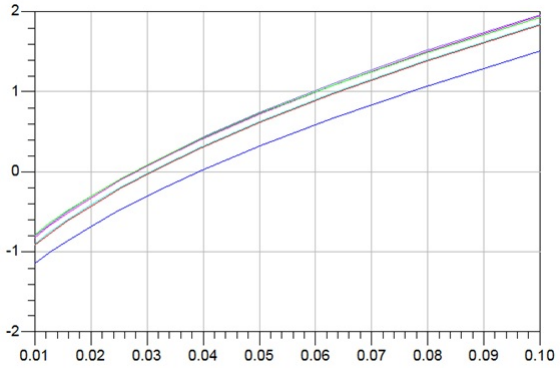

Figure 6: *Diodes comparison*

6 A more practical approach: voltage source

Since a voltage biased circuit is more practical, due to its simplicity, it is decided to change the current source by a voltage source, as shown in the figure 7. The extra-resistor is necessary, since without it the output DC voltage would be constant (the output would be short-circuited with the source).

The voltage source is set at –1.8 V, so that the current through the diode is equal to the current in the previous circuit. Figures 8 and 9 show some results for the one tone analysis.

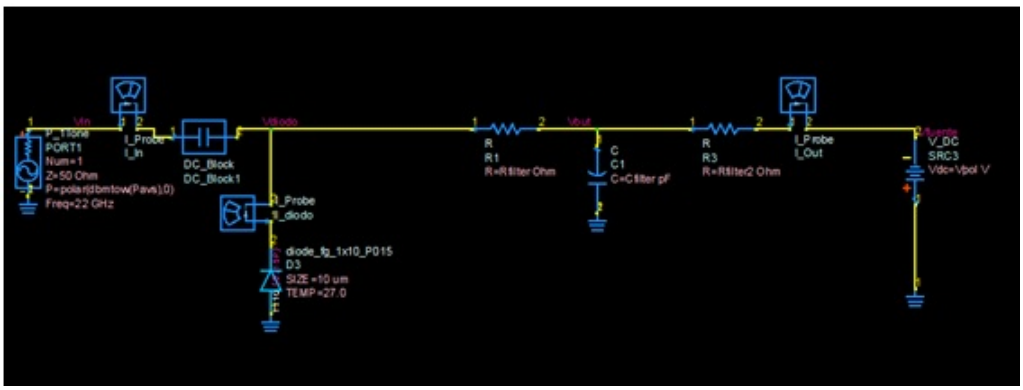

Figure 7: *Voltage source schematic*

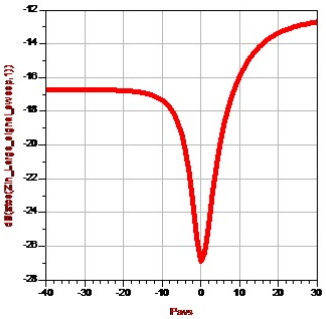

Figure 8: *S11*

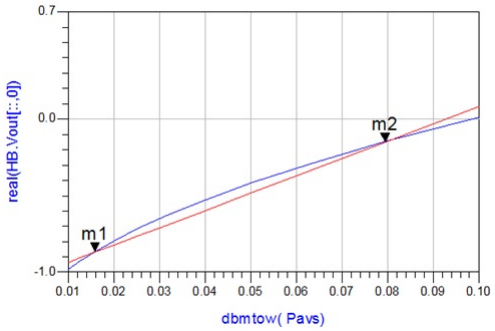

Figure 9: *Vout vs. Pin*

7 Matching improvement

So far, matching issues have not been treated. Our purpose is to improve the matching, above all, for higher input powers.
It requires a trade off between the different polarizations, since the S11 varies depending on the control variable Vbias. Finally the matching shown in the figure 10 is achieved and is realised just by a line path. Later on, after final component changes, all the sizes of the lines are adjusted in order to achieve the best possible matching.

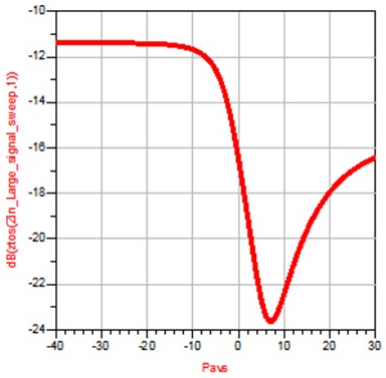

Figure 10: *S11*

8 Real components replacement

The replacement of the ideal components with real components is carried out in order to realise more realistic simulations, and pads are added at the output and input bias.

9 Frequency response and bandwidth

In order to take into account the frequency response and the size of the bandwidth a two tone simulation is performed. The central frequency is set at 22 GHz and both tone are equispaced at both sides of this frequency by δf.
It is desirable to obtain the largest envelope magnitude with the smaller possible harmonics and enough bandwidth.

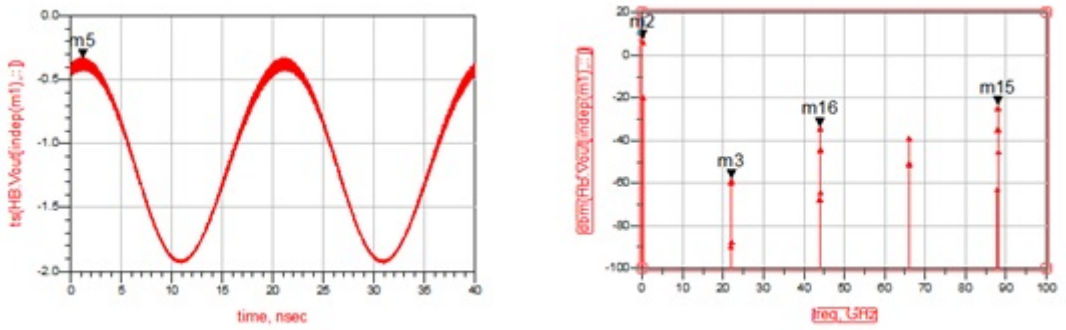

Figure 11: *Envelope in time domain and frequency response*

9.1 Improvement of the frequency response

In order to decrease the biggest harmonics shown in the previous analysis, additional capacitors are added to the design. Good harmonic rejection is achieved, improving the ripple as shown in the figure 12.
It is also added a big shunt capacitor close to the bias input, in order to remove possible RF signals from the source. All these changes are shown in the figure 13.

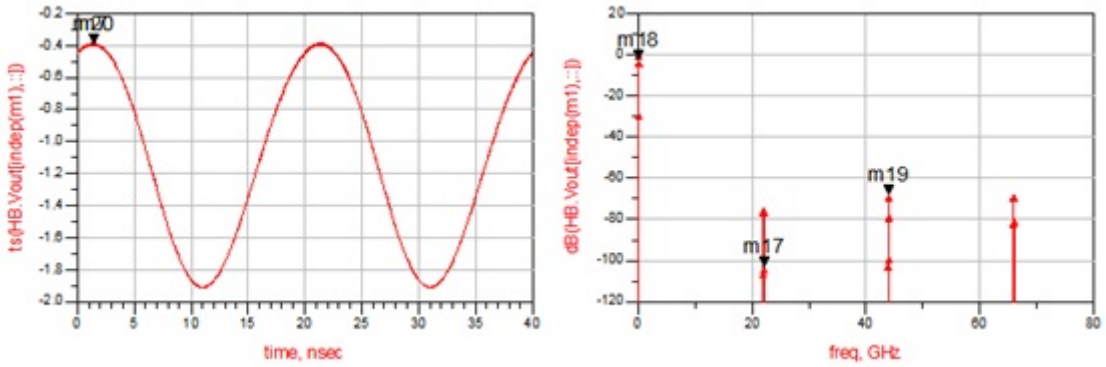

Figure 12: *Improved frequency response*

A reduction of the harmonics and a envelope bandwidth of 140 MHz are achieved, however it is also shown a small reduction in the envelope magnitude. The figure 14 shows the envelope magnitude at the bandwidth limit frequency.

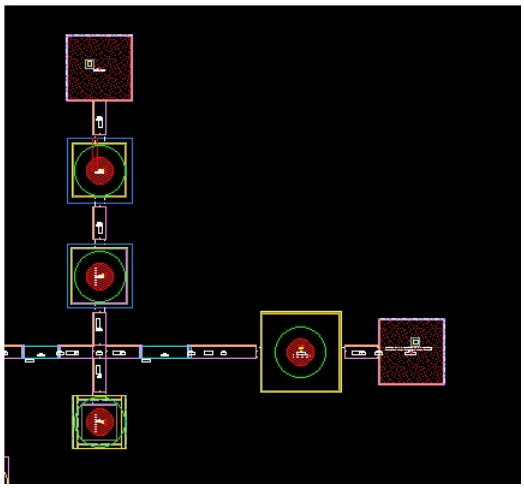

Figure 13: *Added components*

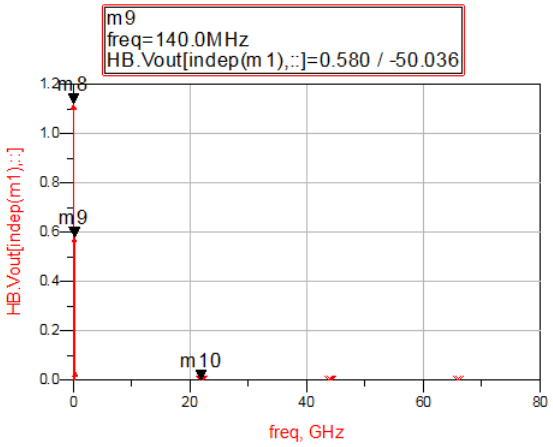

Figure 14: *Envelope's magnitude*

10 Maximum current and power dissipation

A problem to take into account is the maximum current through the different components (which determines the dissipated power), being the diode and the resistors the most restrictive components.

Maximum current allowed through the diode

- 1 gate-10 um $\longrightarrow$ 1.5 mA
- 2 gates-10 um $\longrightarrow$ 2 mA

However, just the bias current is 2.2 mA at the best case. So how to solve this problem?

Possible solutions

Increasing the resistors. We do not need big current to make the circuit linear, the problem is given by the minimum voltage we need at the output when the Pin is lowest, small resistors requires large currents to get that voltage.

Doubling the diode. Using two diodes, the current through each of the diodes is reduced though the Ibias supplied by the source is slightly larger.

Both solutions are implemented, and both of them requires changes of the circuit. The resulting resistors are so big that the bandwidth of the circuit is decreased (since the resistors form a LPF together with the capacitor), so the capacitors which were added to kill the harmonics must be removed. The 1-gate $\times$ 10 μm diodes are maintained since in the case of the 2-gate diodes the current is closer to their limit.
The resistors have maximum current limited by their defined width, so the latter is increased enough to assure this limit is not exceeded.
All these changes force to necessary re-design the matching, adjusting the line path and adding an open stub.

Doubling the diode instead of increasing still more the resistors presents the next advantages-disadvantages:

Advantages

- Offers the largest bandwidth (59 MHz for the worst case).
- The maximum current through the diode is exceeded only with maximum bias voltage (–2.8 V) and highest Pin (being 1.6 mA).
- A good matching is achieved.

Disadvantages

- PDC consumption slightly higher than the others designs (around 2 dB).
- Worse linearity (0.03851 VRMS compared with the previous obtained value of 0.0296).

11 Layout

The final layout is shown in the figure 15. In order to achieved the smallest possible size the resistors are shaped. The bends resistors model does not work properly so the simulation are realised with a normal resistor with the equivalent resistance. The total chip size is 1,253 mm $\times$ 0,93 mm.

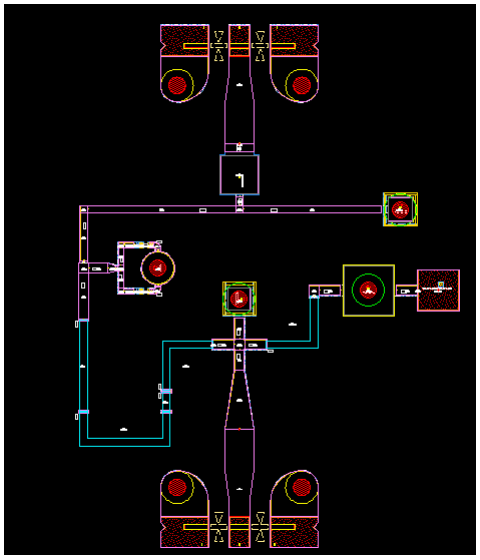

Figure 15: *Final layout*

12 EM simulation

Due to the high frequency of the design it is necessary an EM simulation of the circuit, it takes into account almost all the passive components and block to simulate is shown in the figure 16.

The simulation block is ready though the simulation is not realised yet, therefore the results are not present in this report.

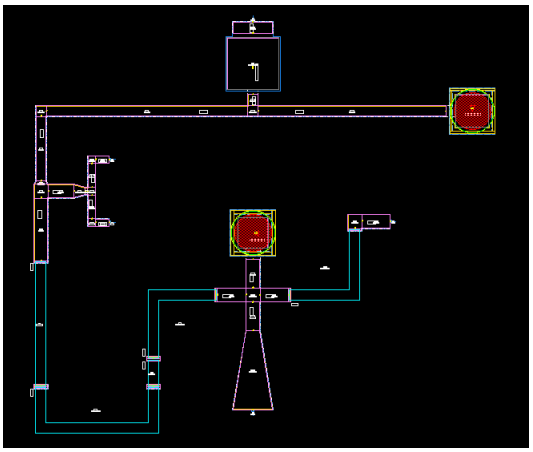

Figure 16: *EM simulation block*

13 Results

This section gathers and shows the one and two tone simulations of the circuit.

13.1 One tone simulation

There are three desirable output ranges $[-2,-1]$,$[-1.5,-0.5]$ and $[-1,0]$. For each one of these ranges is set a different Vbias.

DC output [–1,0] , Vbias=–1.7

The figures 17 and 18 show the results of the one tone simulation with a –1.7 V Vbias.

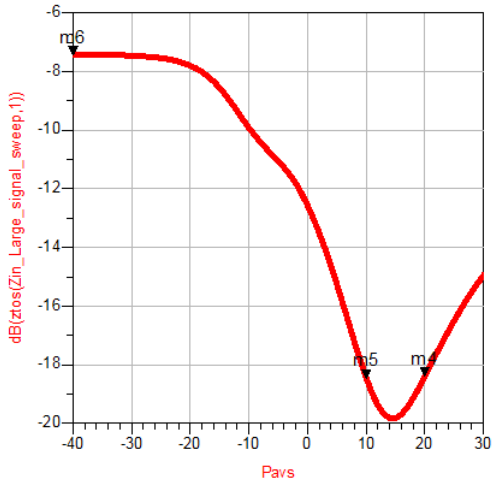

Figure 17: *S11*

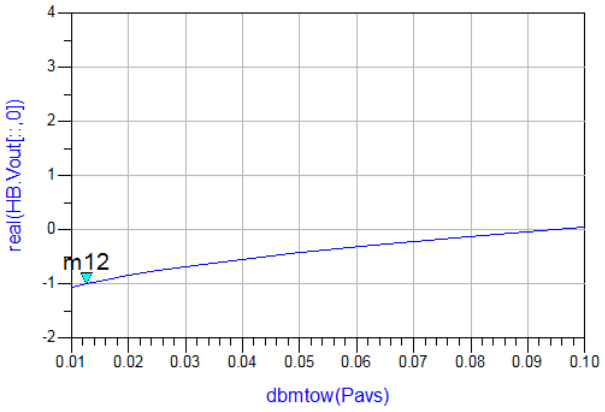

Figure 18: *Vout vs Pin*

The previous figure 17 shows the matching depending on the input power,instead the figure 19 shows the matching depending on the input power and for several frequencies showing a good matching from 21 to 22.5 GHz at the expected input power range ($[10,20]$ dBm).

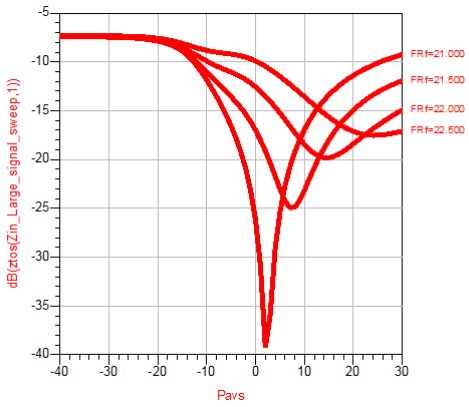

Figure 19: *S11 several frequencies, –1.7V*

DC output [–1.5,–0.5] , Vbias=–2.3

The figures 20 and 21 show the results of the one tone simulation with a –2.3 V Vbias.

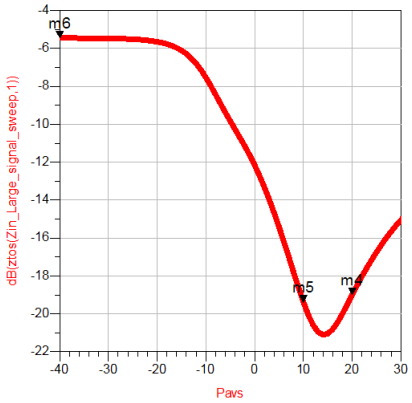

Figure 20: *S11*

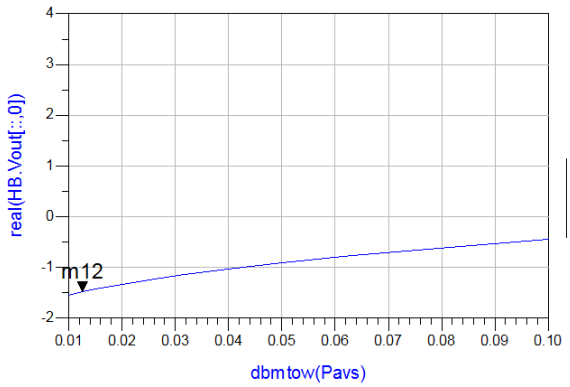

Figure 21: *Vout vs Pin*

The previous figure 20 shows the matching depending on the input power, instead the figure 22 shows the matching depending on the input power and for several frequencies showing a good matching from 21 to 22.5 GHz at the expected input power range ($[10, 20]$dBm).

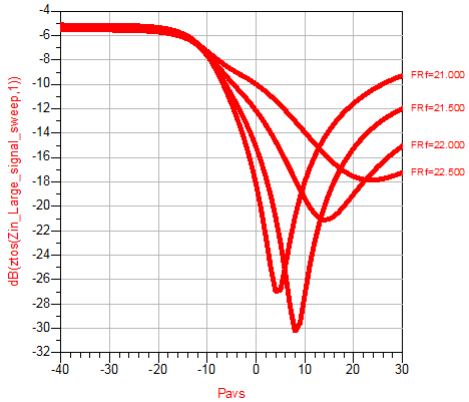

Figure 22: *S11 several frequencies, –2.3 V*

DC output [–2,–1] , Vbias=–2.8

The figures 23 and 24 show the results of the one tone simulation with a –2.8 V Vbias.

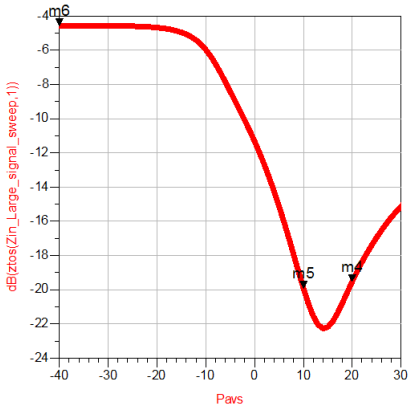

Figure 23: *S11*

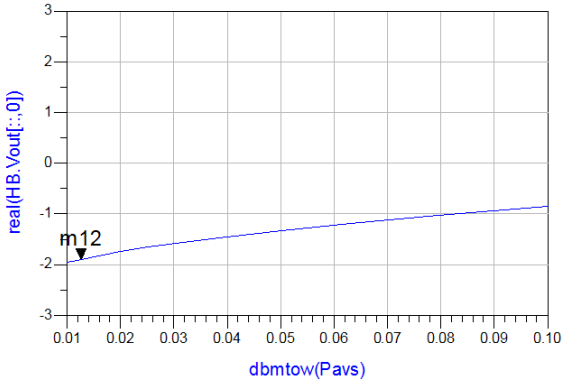

Figure 24: *Vout vs Pin*

The previous figure 23 shows the matching depending on the input power,instead the figure 25 shows the matching depending on the input power and for several frequencies showing a good matching from 21 to 22.5 GHz at the expected input power range ([10, 20]dBm).

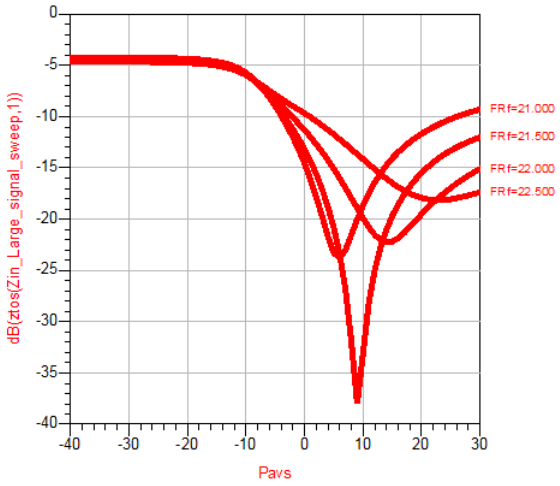

Figure 25: *S11 several frequencies, –2.8 V*

To conclude with the one tone simulation, the figure 26 shows the DC maximum current through each diode (with maximum Vbias and Pin) and the table 1 summarise the most important results (Pdc corresponds to the maximum input power).

Expected DCout (V)	Real DCout(V)	Vbias (V)	Pdc (dBm)	Sens.	VRMSE
$[-1, 0]$	$[-1.056, 0.011]$	–1.7	6.85	12.81	0.03851
$[-1.5, -0.5]$	$[-1.545, -0.448]$	–2.3	8.44	12.816	0.03851
$[-2, -1]$	$[-1.952, -0.855]$	–2.8	9.5	12.817	0.03848

Table 1: *One tone simulation summary*

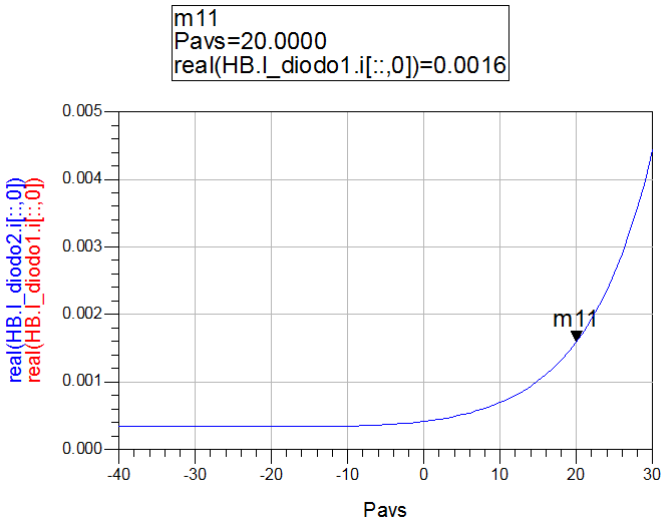

Figure 26: *Maximum current through each diode*

13.2 Two tone simulation

The simulation is carried out at the central frequency of 22 GHz and the frequency of the envelope is swept so that the BW of the circuit can be measure. The measurement was realised for the three different polarization and they show that the smallest BW occurs with the smallest polarization so the figure 27 shows the worst bandwidth at the polarization of –1.7V, being the BW around 59 MHz

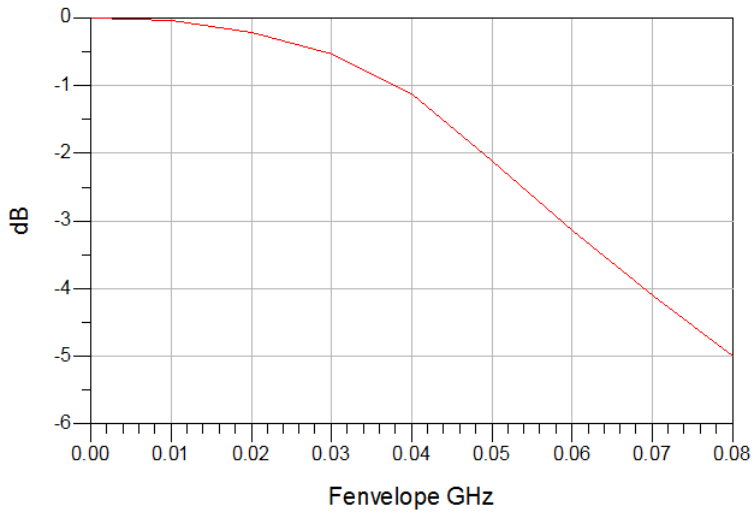

Figure 27: *Envelope bandwidth*

The figures 29 and 28 show the bandwidth for a central frequency of 21 and 22.5 GHz.

The figure 30 shows the relation between the envelope and the harmonics at the polarization of –1.7V and for an envelope frequency of 50 MHz, it is also shown the envelope in the time domain.

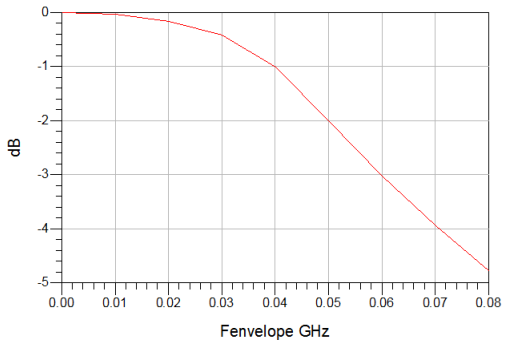

Figure 28: *Envelope BW, $f_{carrier}$ 21 GHz*

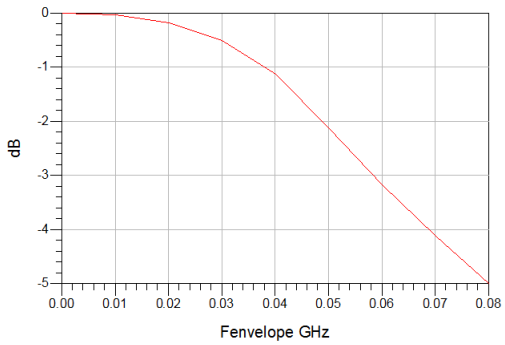

Figure 29: *Envelope BW, $f_{carrier}$ 22.5 GHz*

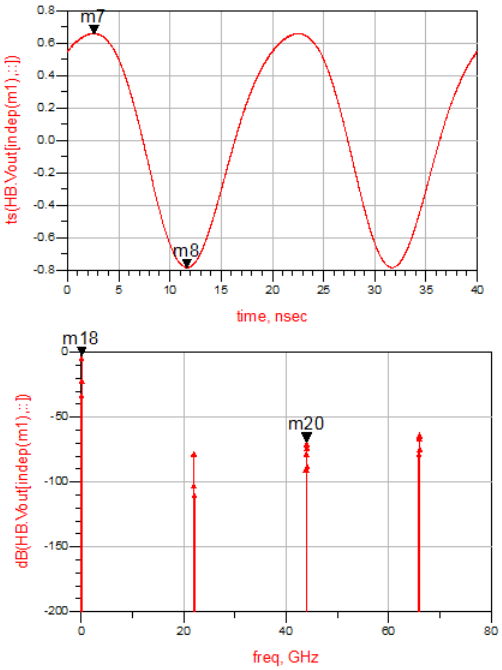

Figure 30: *Envelope and harmonics*

14 Conclusions

An envelope detector for the K-band has been designed. The simulations results show a good matching achieved as well as a good bandwidth, complying all the design constraints. As conclusion of the design, the most limiting feature of the circuit is the maximum current through the diode which obliged to realise some changes in the design, and that could be problematic with maximum Vbias and input power.

Part II
Hybrid design envelope detector S-band (3.5 GHz)

15 Design purpose

The main purpose of this hybrid design is the same as the MMIC design, but now this design is developed to work at the frequency of 3.5 GHz (one of the main frequencies in which works the standard IEEE 802.16 or WIMAX) so it can be used to implement bias tuning with the available Doherty amplifiers.

16 Design constraints

The design is developed to work at the S-band frequency (2-4 GHz), namely at 3.5 GHz, the expected input power is made up of the range between 11 and 21 dBm, the circuit is expected to provide and envelope magnitude around 0.5 V when it is fed with 2 tones with the highest allowed power. It is also desirable a BW larger than 30 MHz.

Finally in order to assure a proper reflection coefficient, the parameter S11 should be below –10 dB for the input power range.

Summary of constraints:

- S-band (2-4 GHz) @ 3.5 GHz
- S11 $\leq$ –10 dB
- Pin = [11,21] dBm
- BW $\geq$ 30 MHz
- Envelope magnitude = 0.5 V @ PinMax

17 Diode selection

The first step is to choose a proper diode taking into account the following features:

- Max forward current
- Max reverse voltage
- Fmax
- Price
- Linearity

Since it is a high frequency design the Schottky diodes seem to be the proper choice. Some Schottky diodes with low price, low capacitance and a spice model available are selected for testing.

17.1 Bandwidth measure of the diode

The bandwidth of each diode is tested using the schematic shown on the figure 31.

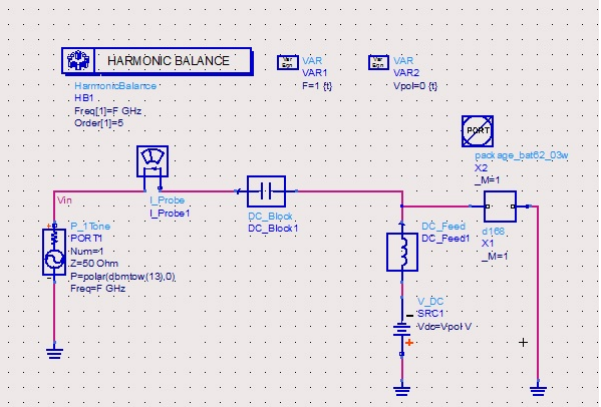

Figure 31: *Diode's bandwidth schematic*

The frequency of the tone is set at a low frequency, then the magnitude of the Vin is measured and the frequency is increased till it is decreased by the root square of two.
To be mention that this bandwidth is valid for this polarization, and the measure can be done with Vin for we are using ideal DC block and DC feed.

The table 2 shows a summary of the bandwidth and some other important features of several tested diodes.

Diode	**Price(euros)**	**BW GHz**($Vpol = 0$)	**If max (mA)**	**Vr max(V)**
Bat17	0.13	9.5	30	4
Bat15_03	0.514	>15	110	4
Bat62_02	2.395	>15	20	40
Bat62_03	0.262	>15	20	40
1ps10sb82	unknown	9.5	30	15
Da2710100L	0.052	***	100	80

Table 2: *Diodes features*

17.2 Linearity and power consumption

The diodes are compared using a first design based on the MMIC design as it is shown in the figure 32, in which some of the diodes present a kind of knee in the middle of the interesting power input band or consume a large amount of power so finally the more linear and with less power consumption diode is chosen.

17.3 Chosen diode

Infineon BAT62-03W, it is a single diode with an SOD323 package. Main features:

- If 20 ma
- Vr 40 V
- Ptot 100 mw
- Ct (Vr=0,f=1MHx)=0.35 pF

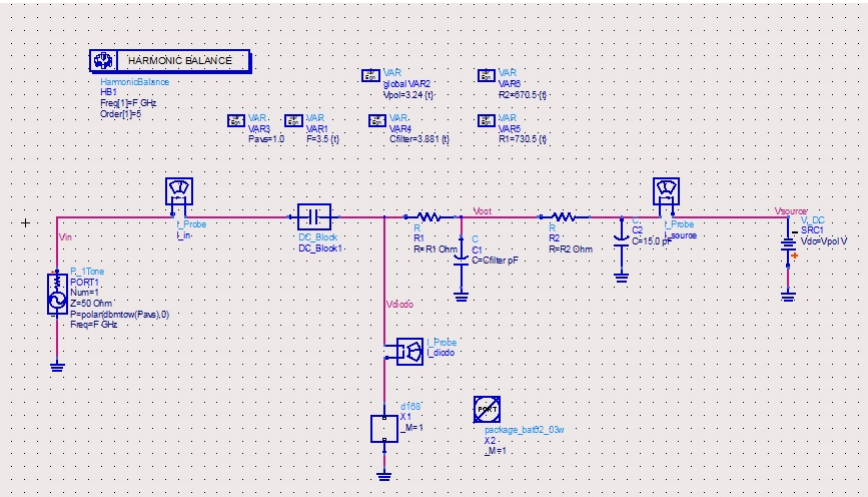

Figure 32: *Schematic based on the MMIC design*

18 Circuit design

As shown in the previous section, our design is based on the MMIC design, though the diode behaviour is quite different.

18.1 Lowpass filter

A simple RC filter like the one used in the MMIC design in order to remove the harmonics turns out to be too poor for this design, so more complex filter is added to the circuit.
The filter is provided by Mini-Circuit and the one which provides the lowest fundamental harmonic and the largest magnitude of the envelope for the 2 tone analysis is chosen.

The model is LFCN-2000 and it provides and attenuation peak at our interest frequency as it is shown in the figure 33.

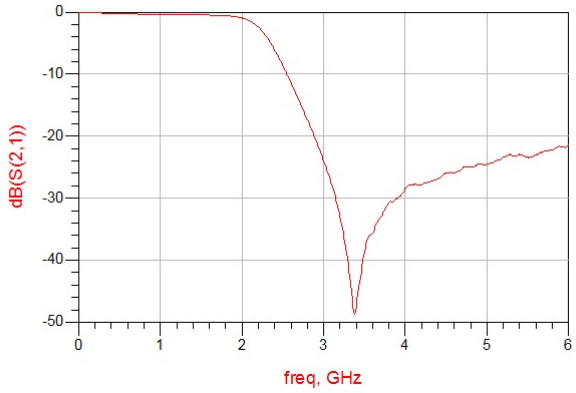

Figure 33: *Filter response*

The capacitance of the original RC filter is kept, since it improves the frequency response (otherwise some harmonics increase), however due to its low value the capacitor is replaced by an open stub.
As a measure to improve the efficiency of the filter a series inductor is placed before the filter, improving the harmonics rejection.

In these early steps it is also realised the first matching networks using up to three lumped components.

18.2 Maximum current through the diode

The maximum forward current through the diodes is 20 mA, however as it is shown in the simulations, this current in our design exceeds this value: some changes are necessary in our design.
As possible solutions we can increase the value of the resistors, decrease the Vbias or increase the number of diodes.
All these possible solutions were tested: decreasing Vbias, the current almost did not decrease; increasing the value of the resistors turns out in a slight change in the current while the magnitude of the envelope is strongly decreased; therefore, the third solution (increasing the number of diodes) was chosen.
Using two diodes, the value of the current was still too close to the limit, so finally a three diodes design was developed. The comparison between the maximum currents through one, two and three diodes is shown in the figure 34. It is remarkable that the DC power consumption of the

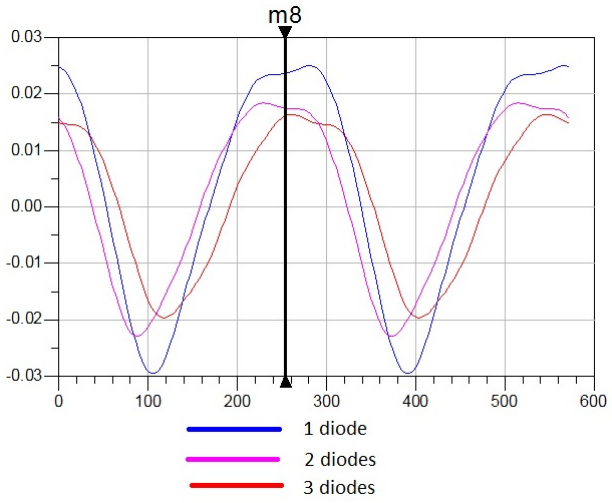

Figure 34: *Currents through the diodes(Maximum forward current 20 mA)*

circuit is only increased in 0.2 dB using three diodes.

18.3 Matching

Initially the matching is realised with lumped components. A good matching is achieved, offering a good frequency response between 3.2 to 3.7 GHz , nevertheless the values of the components turned out to be very low, in particular the inductor values. As a consequence, lumped components are replaced by a line-open stub L-network as shown in the figure 35. Though the frequency response is not as good as in the lumped component case, a good and more easy-reliable matching is achieved from 3.4 to 3.6 GHz.

ADS provides two different kind of open stub models, MLOC and MLEF. Although both different models are equal in the layout representation the behaviour at high frequencies is quite different.
An electromagnetic simulation of an open stub compared with the simulations of both models shows that at high frequencies the MLEF provides a better model so it is used for the input matching network. The achieved matching is shown together with the rest of the results in the section 19. The figure 36 shows the comparison between the MLOC model (red), the EM simulation (magenta) and the MLEF model (blue).

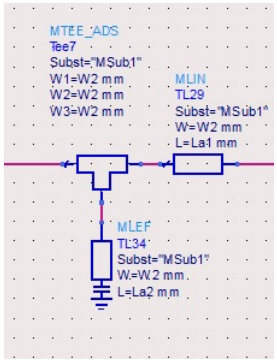

Figure 35: *Matching network*

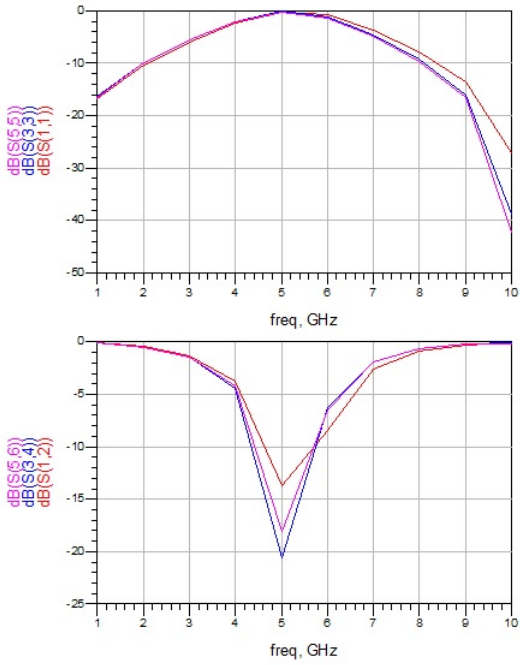

Figure 36: *Open stubs comparison*

18.4 Polarization voltage

Since one of the purposes of the circuit is using it as a part of a power amplifier (in order to implement the bias tuning in a Doherty amplifier) it seems obvious that is desirable the lowest possible DC power consumption, that can be achieved with a 0 V polarization. However, the Vbias is strongly related with the bandwidth of the circuit: the larger is the Vbias, the wider is the bandwidth, so it is necessary a trade off between both of them. Using a 0 V polarization a 28 MHz bandwidth is achieved, a value below the the initial requirement so finally a –3 V polarization is chosen allowing the circuit a 44 MHz bandwidth with a DC power consumption around 10-11 dBm.

19 Simulations results

In this section are shown the results of the one and two tone simulations.

19.0.1 One tone analysis

The following figures (37,38 and 39) show the S11, DC power consumption and position in the smith chart (corresponding to the maximum Pin) when the circuit is fed with one tone signal.

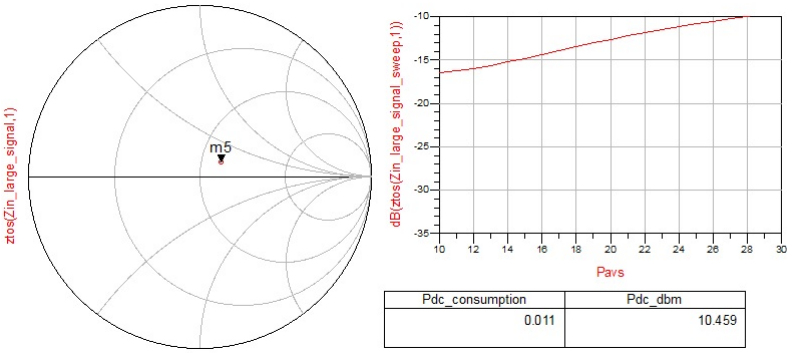

Figure 37: *Matching at 3.4 GHz*

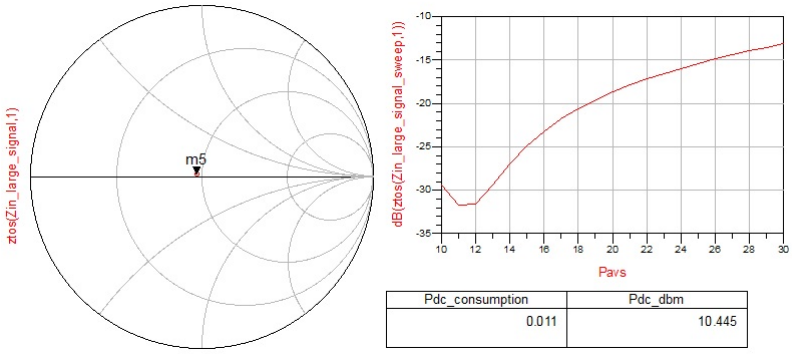

Figure 38: *Matching at 3.5 GHz*

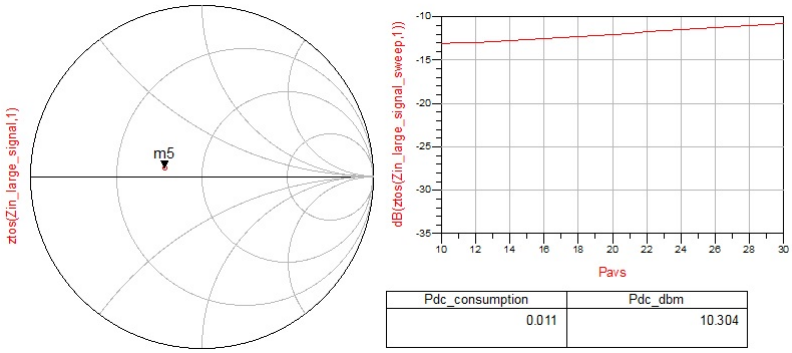

Figure 39: *Matching at 3.6 GHz*

19.1 Two tone analysis

It is achieved a bandwidth for the envelope of 44 MHz using a –3 V Vbias and a carrier with a frequency from 3.4 to 3.6 GHz, this bandwidth is defined as the frequency in which the magnitude of the envelope is equal to the magnitude of the envelope at very low frequency divided by the root square of two (3 dB bandwidth).

The magnitude of the envelope for the maximum input power varies from 0.645 V ($F_{envelope} = 2KHz$) to 0.456 V ($F_{envelope} = 44MHz$) and it is achieved with a power of 18 dBm for each tone.

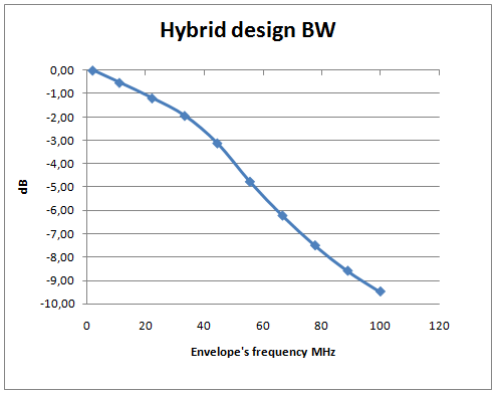

Figure 40: *Simulated BW, Vbias=–3 V, central freq= 3.5 GHz*

In the figures 41, 42 and 43 are shown the envelope in the time and frequency domain together with the different harmonics for an envelope frequency of 36 MHz with a carrier frequency of 3.5 GHz.

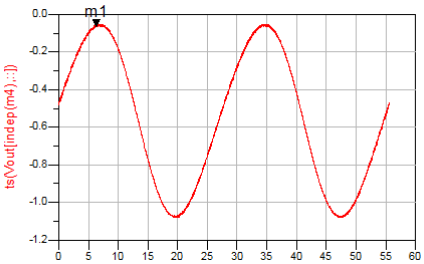

Figure 41: *Envelope 36 MHz, time domain*

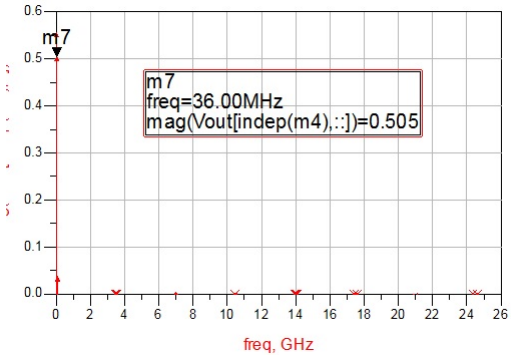

Figure 42: *Magnitude Vout, frequency domain*

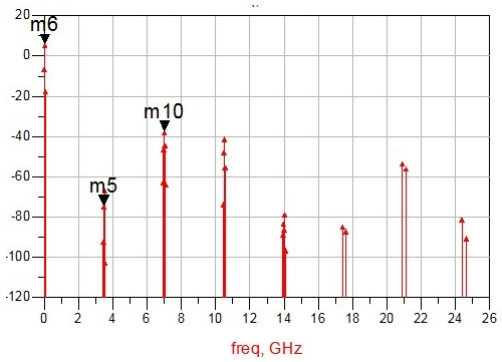

Figure 43: *dBm Vout, frequency domain*

20 Electromagnetic simulations

After the filter the circuit works at low frequencies (below 42 MHz) so an electromagnetic simulation of this part is not necessary, however the previous part works at high frequency so an EM simulation is necessary in order to assure the correct work of the circuit.
This part of the circuit is divided into three different blocks, the first one involves the matching, the second one the 'trident' in which are placed the three diodes and the third one the open stub before the filter, it is shown in the figure 44.

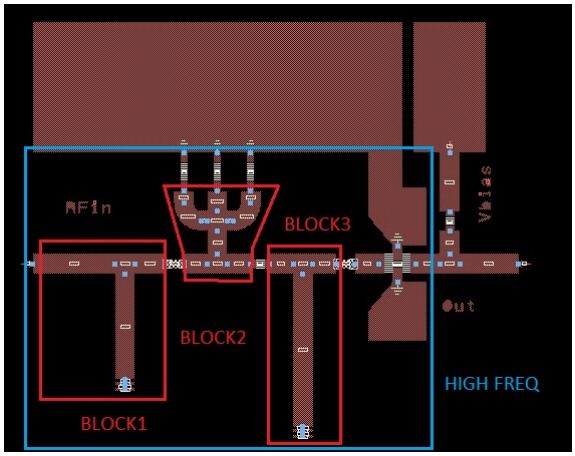

Figure 44: *EM simulation blocks*

Each one of these blocks is simulated, and the EM simulated blocks are added, replacing each respective part of the circuit, to the one and two tone simulations. There are not significant differences between the one tone simulations while in the case of two tone simulations is shown a very lightly reduction of the magnitude of the envelope.

21 Layout

The circuit is tested in measurement setup, which implies two constraints

- The input and the output access lines must be aligned (connectors are not necessary).
- The width of the complete PCB must be below 45 mm.

To correct manufacturing tolerances and model inaccuracies, small pieces of line and gaps are added at the end of the stubs so their length can be modified to improve the matching. The

Murata components include their layout representation, however we will need to design it for the rest of the components (resistors, diodes and filter).
The holes are not included in the layout since they are realised after printing the circuit on the pcb. Since it is used the measuring bench, connectors at the RF input and output of the circuit are not necessary. As a pad for the Vbias is placed a patch of conductor, in which will be solder a wire.
The final version of the layout is shown in the figure 62.

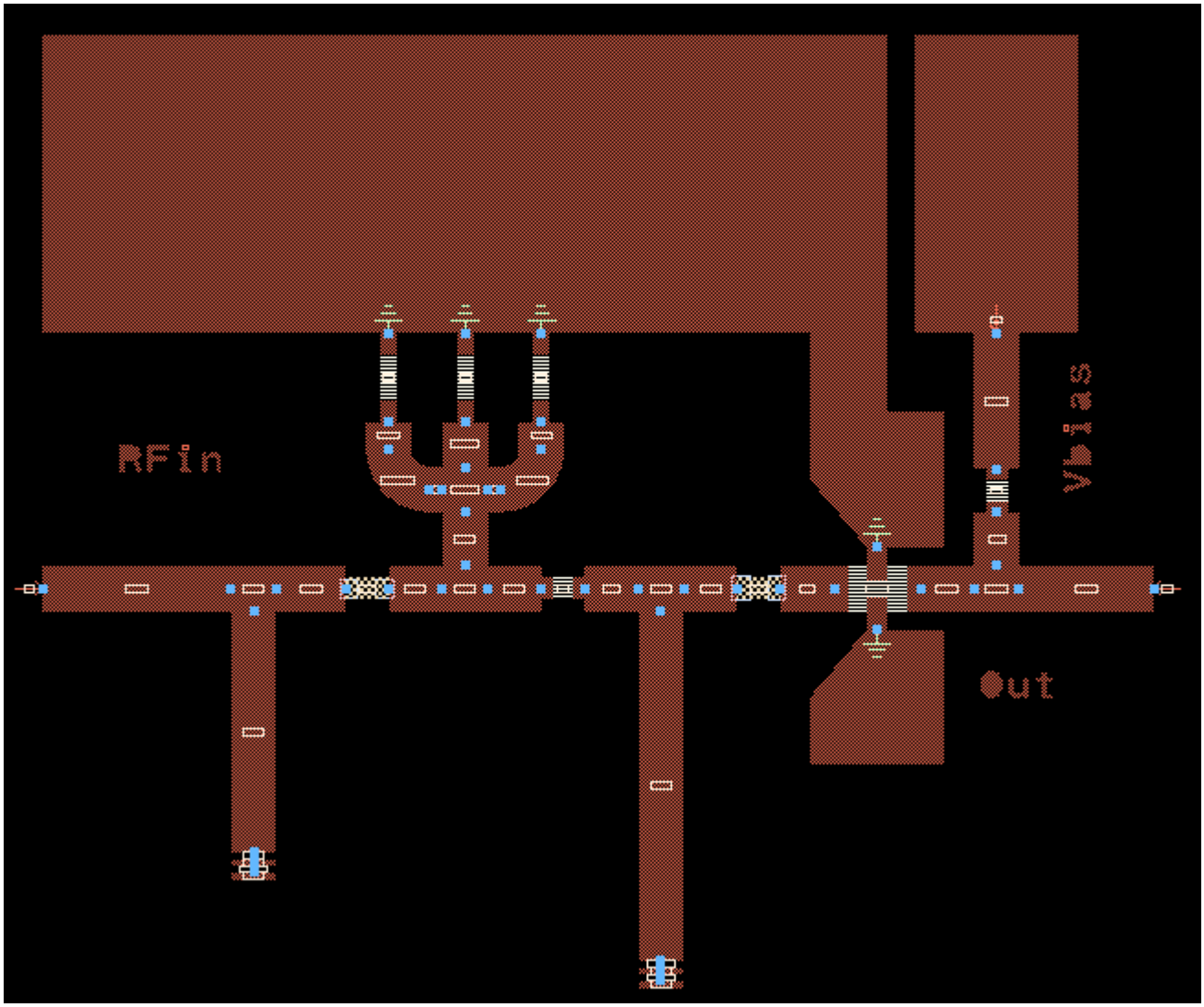

Figure 45: *Layout*

Due to the manufacturing process it is necessary to print a flipped negative of the circuit, which can not be done with ADS so it is done with the help of the program View Mate (the free version).

22 Measures

Two similar envelope detectors are manufactured. In order to characterize the devices the next measurements are realised:

- Measurement of the S parameters (S11).

- Measurement of the DC output when the circuit is feed with one tone.
- Measurement of the envelope at the output when the circuit is feed with two tones.

22.1 S-parameters

Several measurements are made in both devices.

Circuit 1

The S11 parameter is measured at the frequencies from 1 to 6 GHz, the figure 46 shows the simulated S11 (left) and the measured S11 (right) at the polarization of 0 V (red) and –3 V (blue).

It is shown a frequency shift to lower band, as well as worse matching. In order to improve the matching several changes are carried out. The figure 47 shows the improvements achieved by these changes. The red curve represents the original circuit, from this curve the S11 is approached to the desirable frequency of 3.5 GHz by replacing the input capacitor of 4.7 pF by a lower capacitor (3.3 pF) and then cutting input open stub (4 cuts of almost 1mm each are realised).

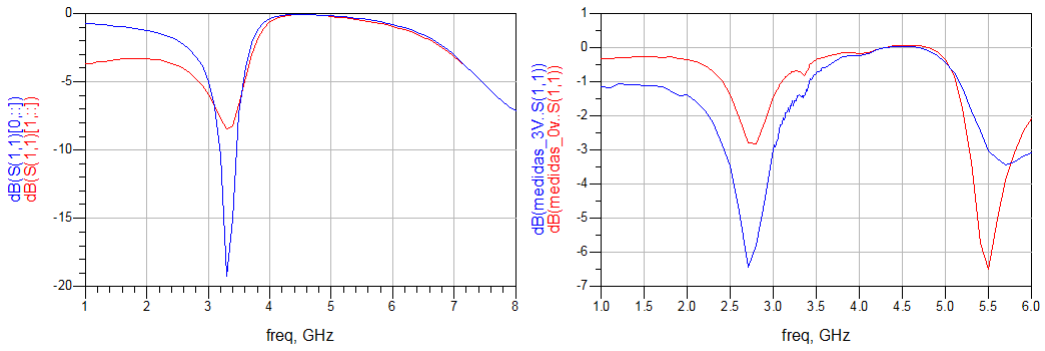

Figure 46: *Circuit 1, simulated and measured S11*

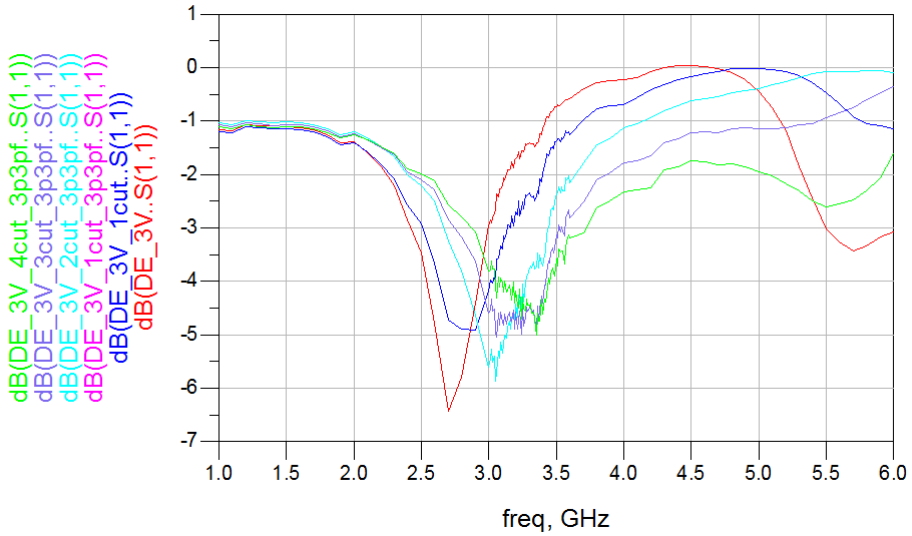

Figure 47: *Improvement of S11*

The figure 48, shows the final S11 of the circuit at the polarization of –3 V (red) and –6 V (blue), it is noticed that for more negative Vbias the matching improves.

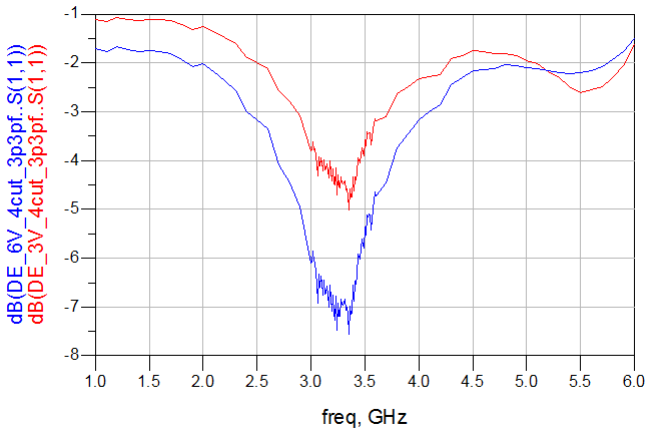

Figure 48: *Final S11*

Circuit 2

The circuit S11 is measured from 1 to 6 GHz with a –3 V Vbias and presents the same problem than the previous one as is shown in the figure 49, the blue curve corresponds to the simulation and the red one to the measurement.

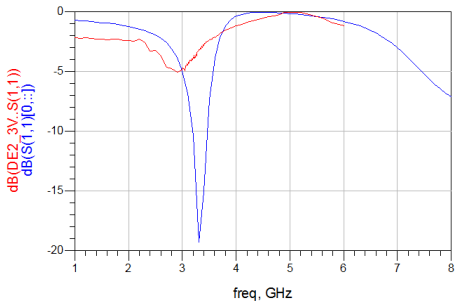

Figure 49: *Circuit 2, measured and simulated S11*

Several changes are realised again, the same than for the previous circuit, the figure 50 shows the improvement of the S11, from the original curve (magenta) to the final version (green). In this case 5 cuts are realised instead of four.

The figure 51, shows the final S11 of the circuit at the polarization of –3 V (red) and –6 V (blue), it is noticed, as in the previous circuit, that for more negative Vbias the matching improves.

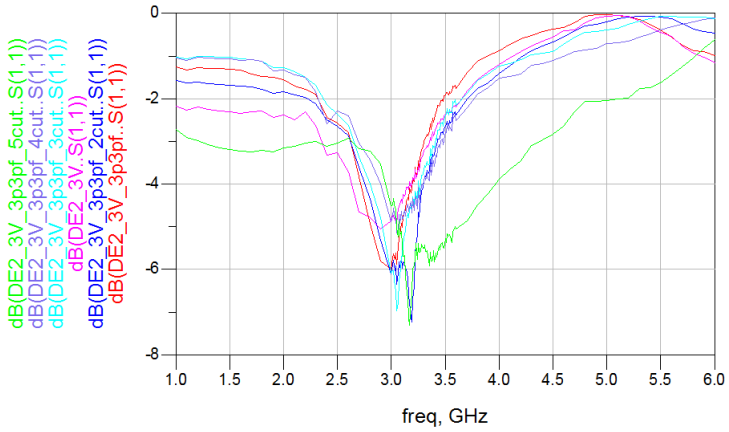

Figure 50: *Improvement of S11*

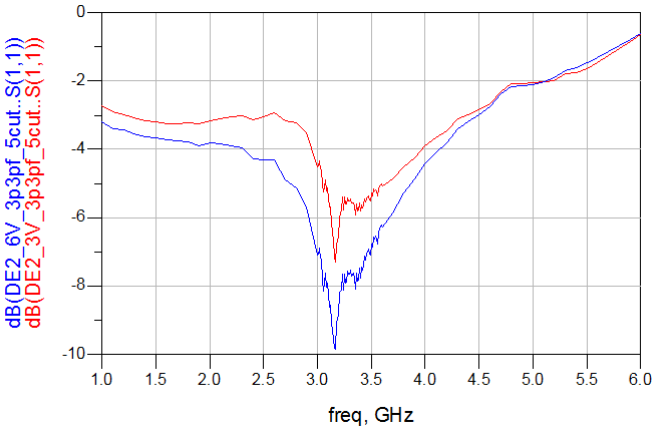

Figure 51

22.2 DC measurement (1 tone)

Both circuits are fed with a 3.5 GHz single tone and the resultant DC at the output is measured for the polarizations of –2, –3 and –4 volts and the results and their comparison with the simulation results are shown in the figures 52, 53 and 54 respectively.

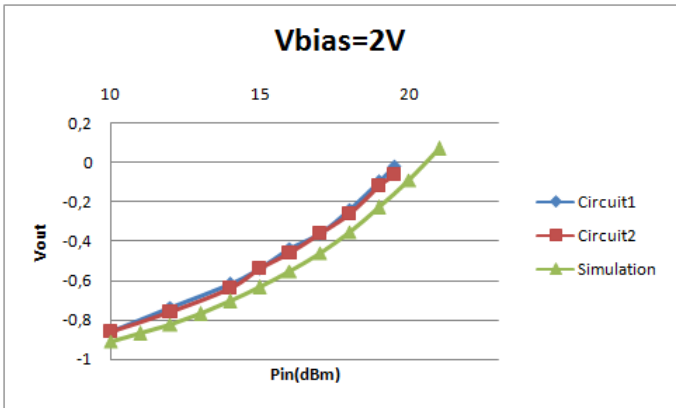

Figure 52

Finally the figure 55 shows the output differences between the different polarizations in the same circuit.

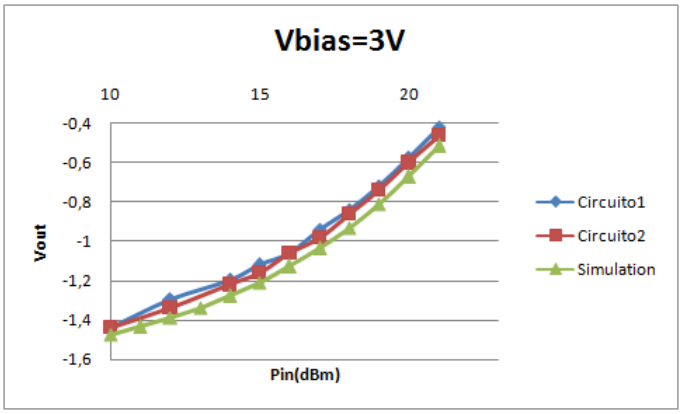

Figure 53

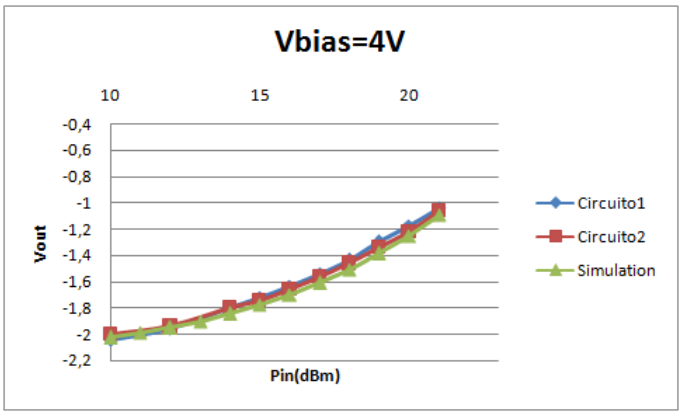

Figure 54

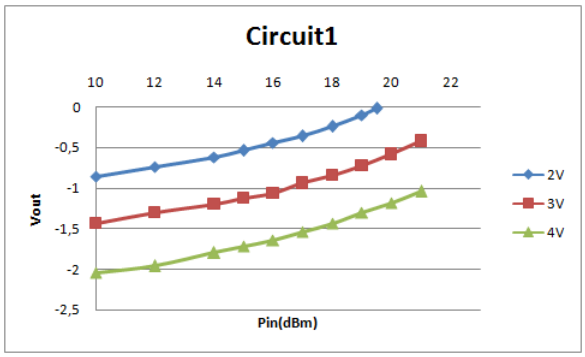

Figure 55: *DC output circuit 1*

22.3 Envelope measurement (2 tones)

In order to measure the envelope bandwidth the circuit is fed with two equispaced tones centred at 3.5 GHz. This signal is generated by modulating a 3.5 GHz tone with a *sin* of frequency δf, therefore the resulting envelope frequency is 2·δf. The space between tones is varied from 10 KHz to 5 MHz. The polarization is set at –3 V and the amplitude of each tone reaches the maximum value of 19 dBm, which means that the average power at the input reaches 16 dBm. The bandwidth of both circuits reaches approximately 2.5 MHz as is shown in the figure 56. This BW is several times smaller than the expected which in simulations reaches 44 MHz.

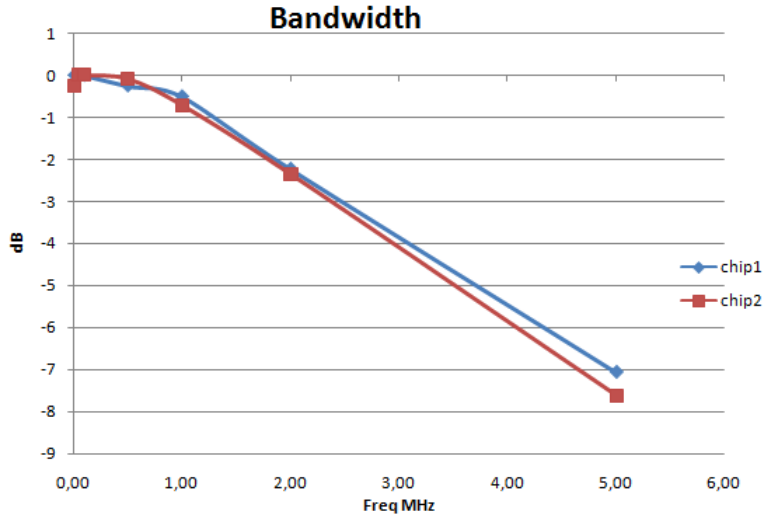

Figure 56: *Normalized frequency response*

The figures 57, 58 and 59 show the measured envelopes for 10 KHz, 5 MHz and 100 KHz. The measurements of the two first figures are realised with the oscilloscope working in the AC mode, while the 100 KHz measurements are realised in DC mode.

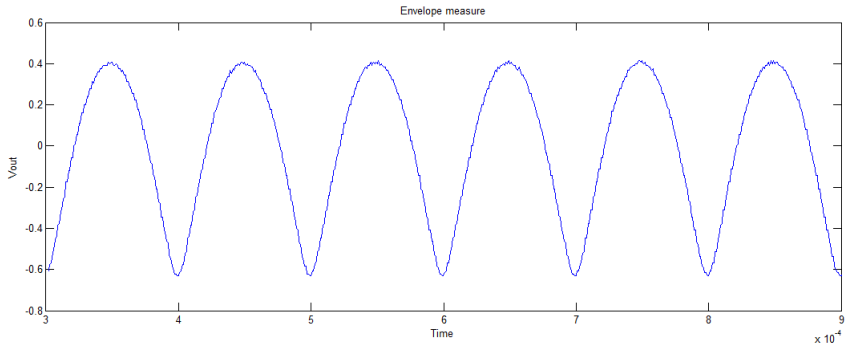

Figure 57: *Measured 10 KHz envelope, AC mode*

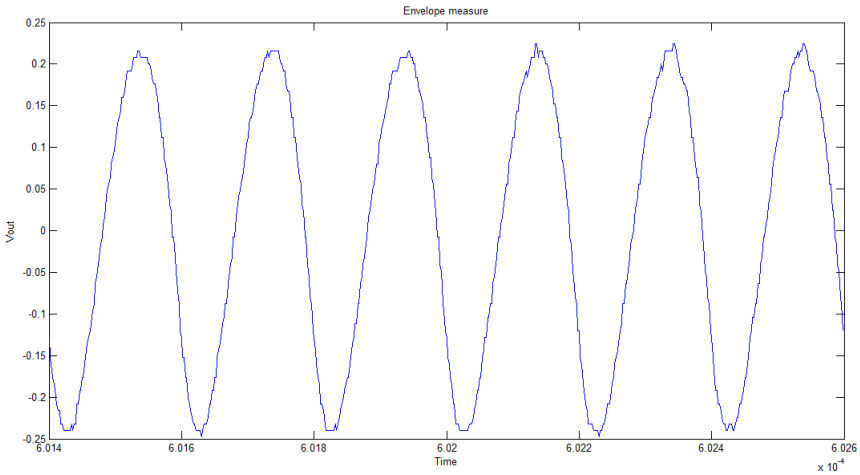

Figure 58: *Measured 5 MHz envelope, AC mode*

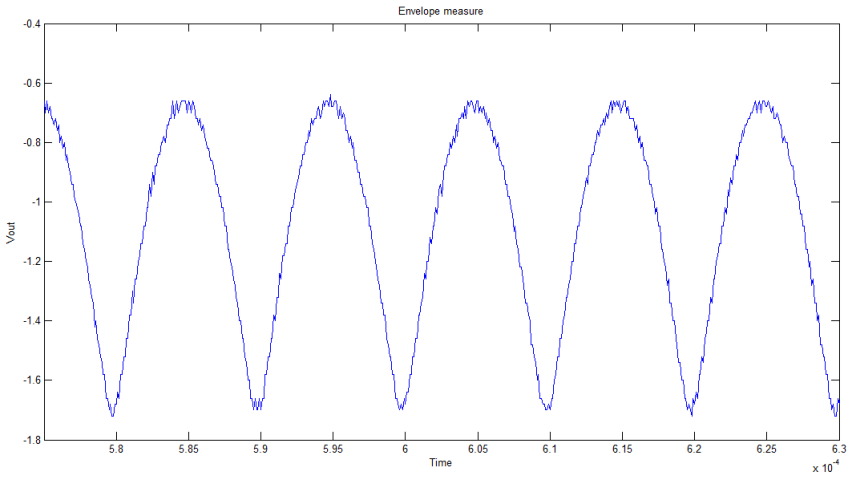

Figure 59: *Measured 100 KHz envelope, DC mode*

22.4 Improving the bandwidth

In order to improve the obtained bandwidth one change is realised in the circuit. The simulations shows that a reduction of the resistor near the diodes turns out in an increase of the bandwidth. So in the simulation the resistor is reduce from 750Ω to 100Ω achieving a BW of 103 MHz. Therefore this change is realised in the circuit 2. The measurement of the bandwidth is shown in the figure 60. As in the previous case the polarization is set to –3 V though having changed the resistor, the Ibias increases from –2 mA up to –3 mA.

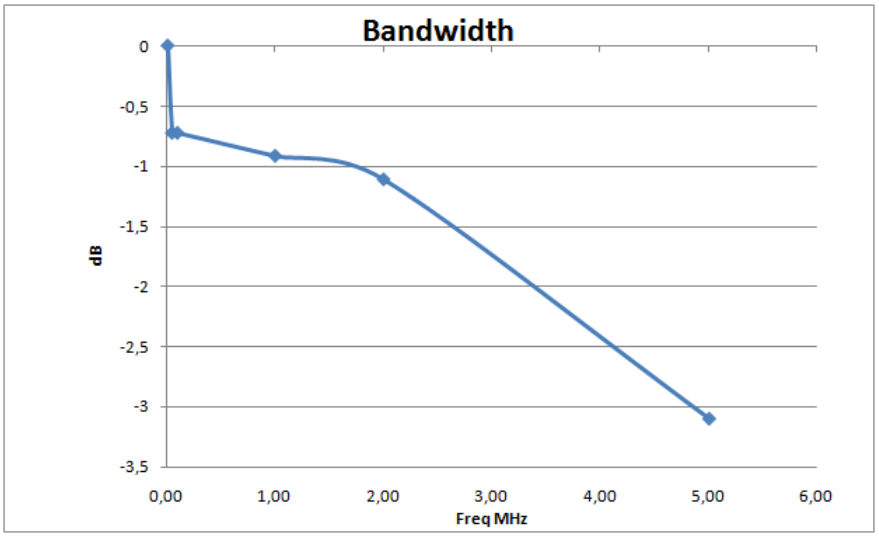

Figure 60: *Improved bandwidth*

As shown in the figure 60 the Bandwidth is doubled though it is still far from the simulated 103 MHz.

23 Conclusions

The obtained envelope detectors differ from the expected results. By changing the input of the circuits (input stub and decoupling capacitor) a decent matching is achieved and the circuits show a good DC output behaviour, being the results very close to the simulation. However, the

two tone measurements show a completely different BW response from the simulations, since the filter has a BW of 2 GHz, the part of the circuit after the filter doesn't affect to the BW nor the inductor before the filter and changing the resistor near the diodes the BW is doubled as in the simulation, it is assumed a wrong diode model for high frequency which could have spoiled the matching and BW.

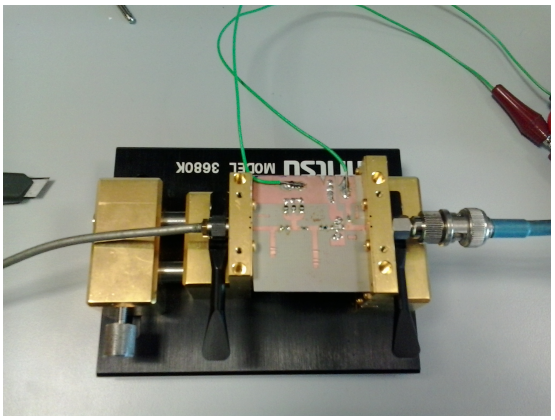

Figure 61: *Envelope detector circuit*

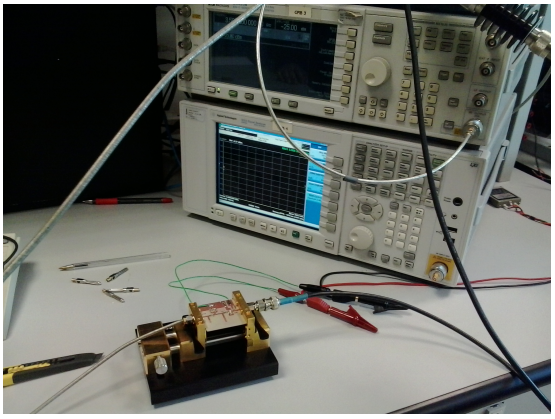

Figure 62: *One and two tone measurements*

References

[1] Herbert Zirath, Zhongxia (Simon): *"Power detectors and envelope detectors in mHEMT MMIC-technology for millimeterwave applications"* , Proceedings of the 5th European Microwave Integrated Circuits Conference.

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