Doherty Power Amplifier

Comparison between standard Doherty and Bias Tuning Doherty

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1. Abstract

The goal of this project is the design, implementation and characterization of a Doherty Power Amplifier (DPA) with bias tuning at 3.5 GHz. The transistor used is a commercial GaN HEMT from Cree inc., with a class AB for the main and a changing class C to AB for the peak. The maximum power provided by the DPA is 28.5W. The efficiency is 67.7% at saturation, and 60.3% at 6 dB back-off. The maximum gain is 14.7 dB with a more linear function than the standard DPAs.

2. WiMAX

This DPA is working at 3.5 GHz, which is the frequency used by the communications standard WiMAX.

WiMAX (Worldwide Interoperability for Microwave Access) is a broadband wireless alternative to cable and DSL. It is a last mile technology that allows high bitrates and high service area (about 50 Km). The standard that defines this technology is the IEEE 802.16. This technology is widely adopted for rural zones, where the population density is low, and the deployment of fiber or cable would be too expensive.

IEE 802.16 is divided in two categories:

- Fixed (IEE 802.16-2004), that operates in the band of 2.5-3.5 GHz and in the license-free 5.8 GHz band.
- Mobile (IEE.802.16), that operates in the band of 2-6 GHz.

Since WiMAX adopts high order modulations, power amplifier needs to be back-off: Doherty scheme provides good efficiency in this condition.

3. Design

Taking as starting point the DPA design made by Jorge Moreno Rubio for its Ph.D. thesis, some changes are made in order to adapt it to a bias tuning implementation.

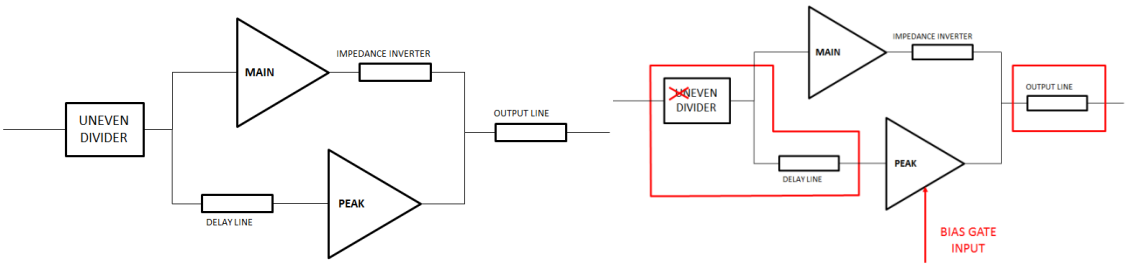


Fig. 1: Original design vs. changes proposed.

3.1 Gate bias functions

The bias tuning here adopted is based on dynamic change of the peak amplifier working conditions, to obtain better performances. One way to control it is changing the gate voltage depending on the input signal. Changing the behavior of the peak can lead to a more linear gain and phase.

The evaluated bias voltage versus input power functions are:

- The original one, a continuous DC voltage of -7V.
- A function with an initial value of -7V that changes abruptly into a value of -2.73V (same bias of main amplifier).
- A function with an initial value of -7V that at a certain point (threshold) rises lineally ending in a value of -2.73V (figures 2 and 3).

The function eventually chosen is the one that changes gradually. This makes the peak amplifier initially work as a class C amplifier, and at a certain point starts to rise the voltage and then gradually works as a class AB amplifier. This guarantees high efficiency in the back-off region, and maximum power delivering by the peak stage at saturation.

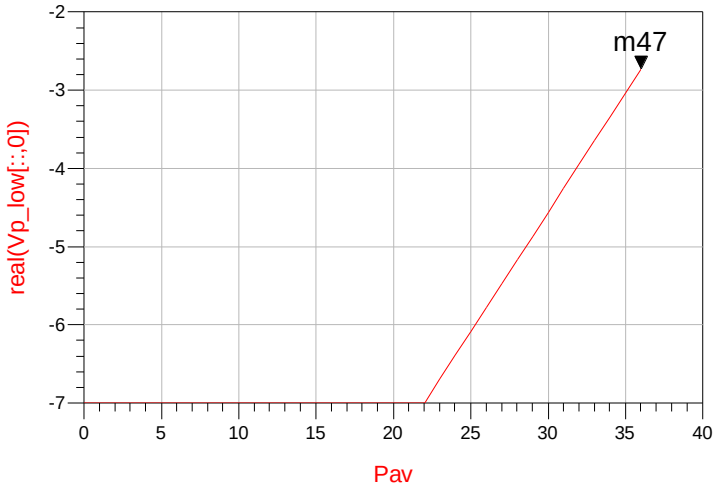


Fig. 2: Vgs function.

```
VAR
Pt1
Vgs=if (Pav >Threshold) then ((-2.73+7)/(36-Threshold))*(Pav-Threshold)-7 else -7 endif
Threshold=21 {t}
```

Fig. 3: Vgs function

3.2 Hybrid

The original hybrid (used as an input power splitter) is replaced with a hybrid that delivers the same power to both amplifiers (Figures 4 and 5).

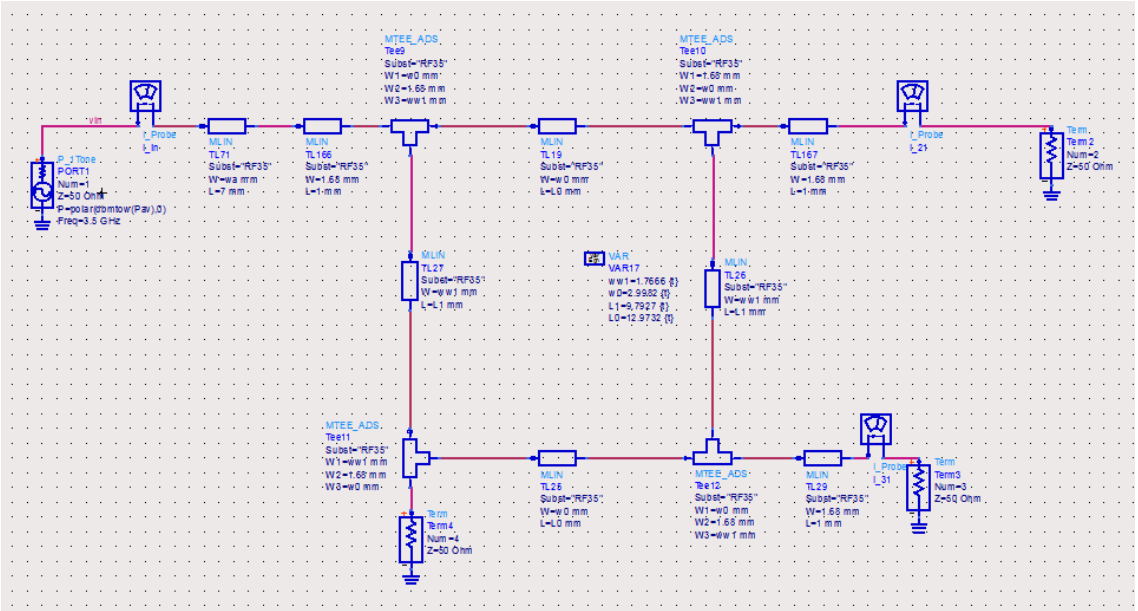


Fig. 4: Hybrid coupler design.

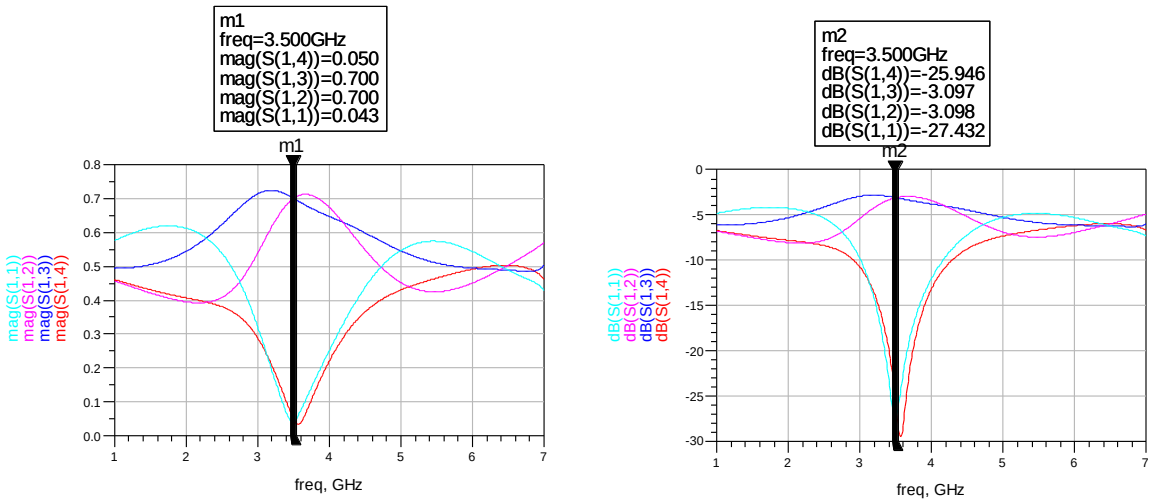


Fig. 5: Hybrid coupler simulations.

3.3 Threshold

The threshold of the function must be adapted, in order to see which variations produces and to decide the optimum point in which the voltage starts to rise.

The most important changes are produced in the gain, the phase, the efficiency, the PAE and the output power.

3.3.1 Phase and gain

- Threshold=36

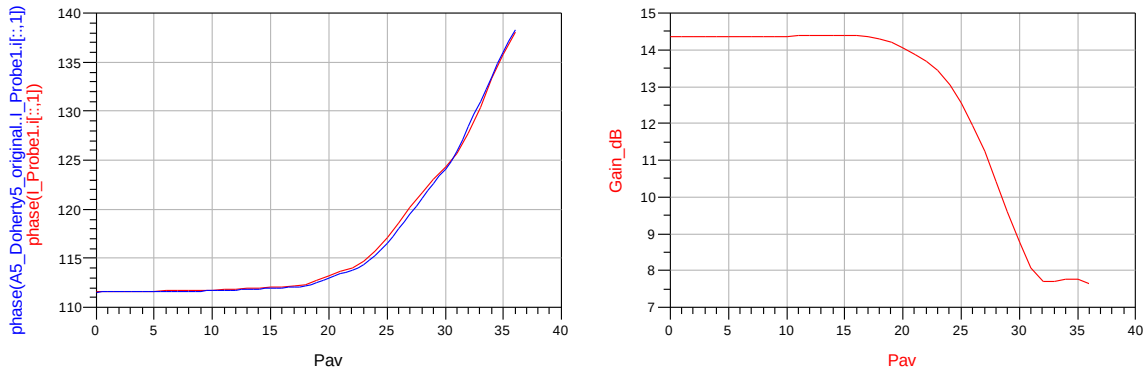
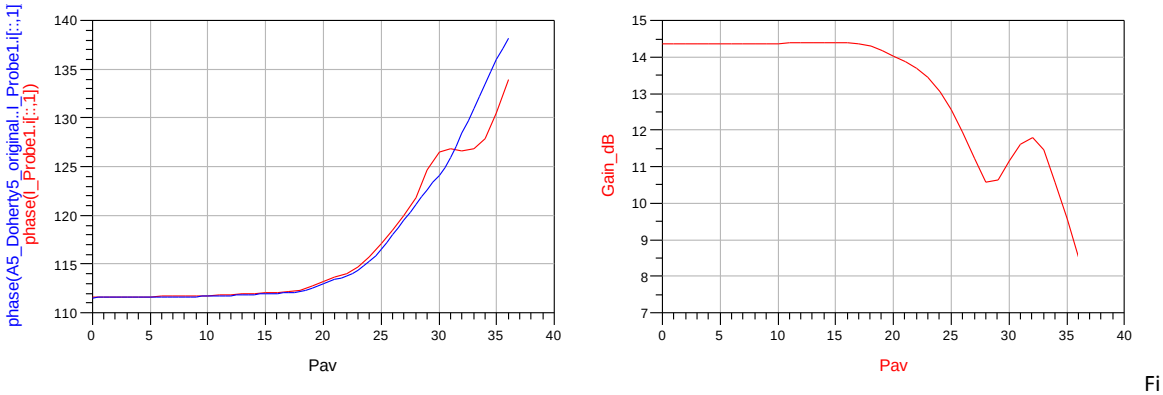


Fig. 6: Gain and phase with a threshold of 36 (the red ones). The blue one is the phase of the original design.

- Threshold=25



Fi

Fig. 7: Gain and phase with a threshold of 25 (the red ones). The blue one is the phase of the original design.

- Threshold=20

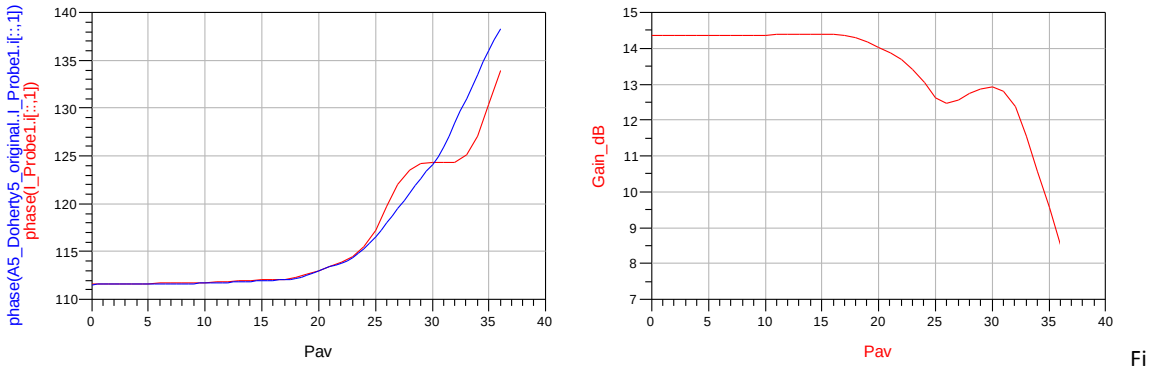


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Fig. 8: Gain and phase with a threshold of 20 (the red ones). The blue one is the phase of the original design.

- Threshold=10

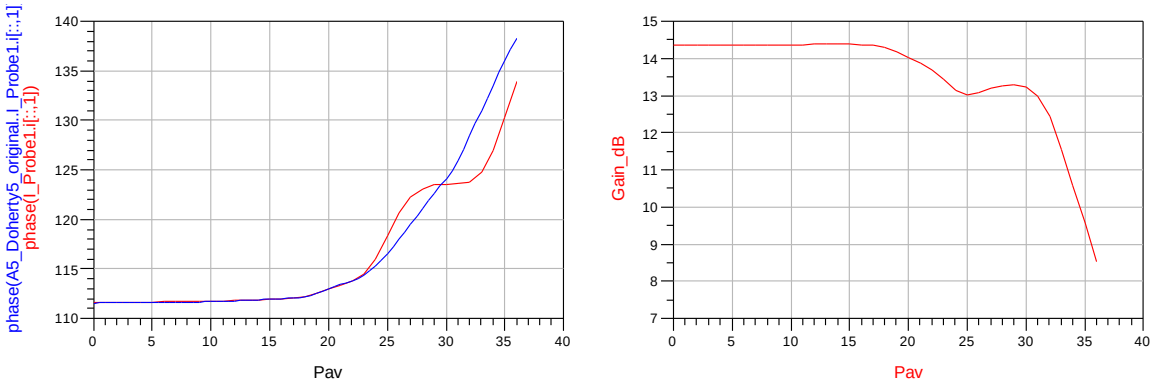

Fig. 9: Gain and phase with a threshold of 10 (the red ones). The blue one is the phase of the original design.

- Threshold=5

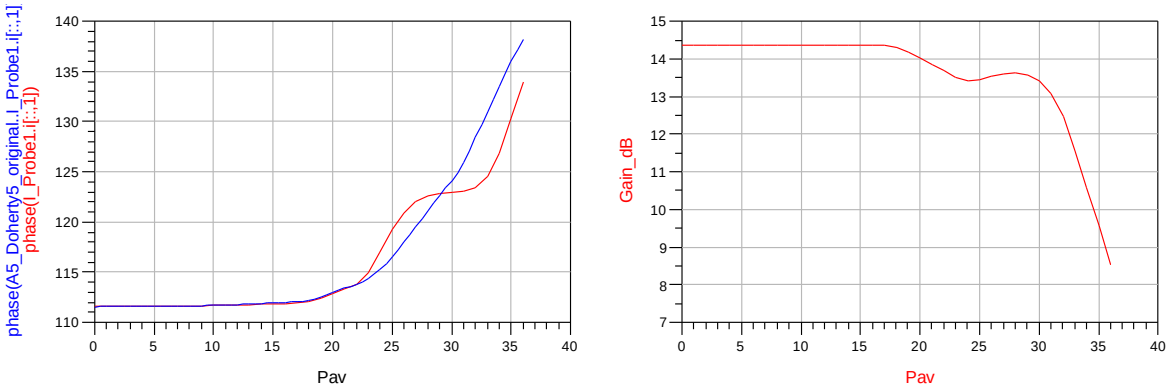

Fig. 10: Gain and phase with a threshold of 5 (the red ones). The blue one is the phase of the original design.

- Threshold=0

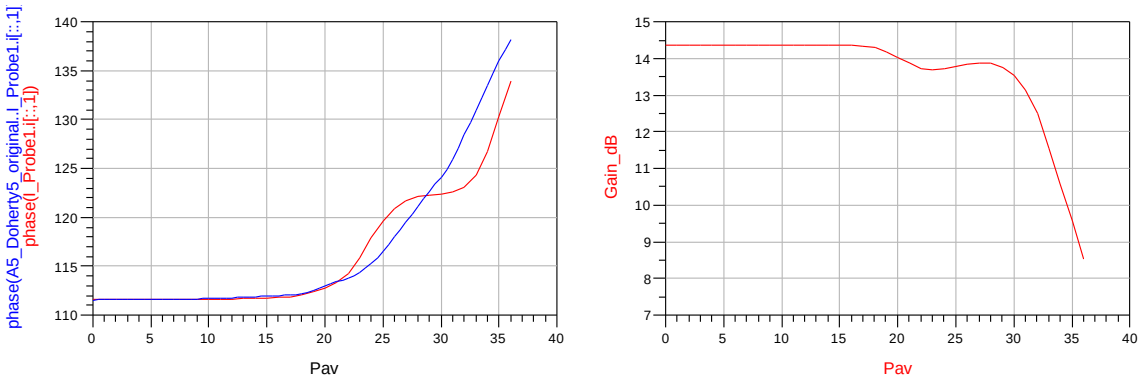

Fig. 11: Gain and phase with a threshold of 0 (the red ones). The blue one is the phase of the original design.

3.3.2 Efficiency and PAE

- Threshold=36

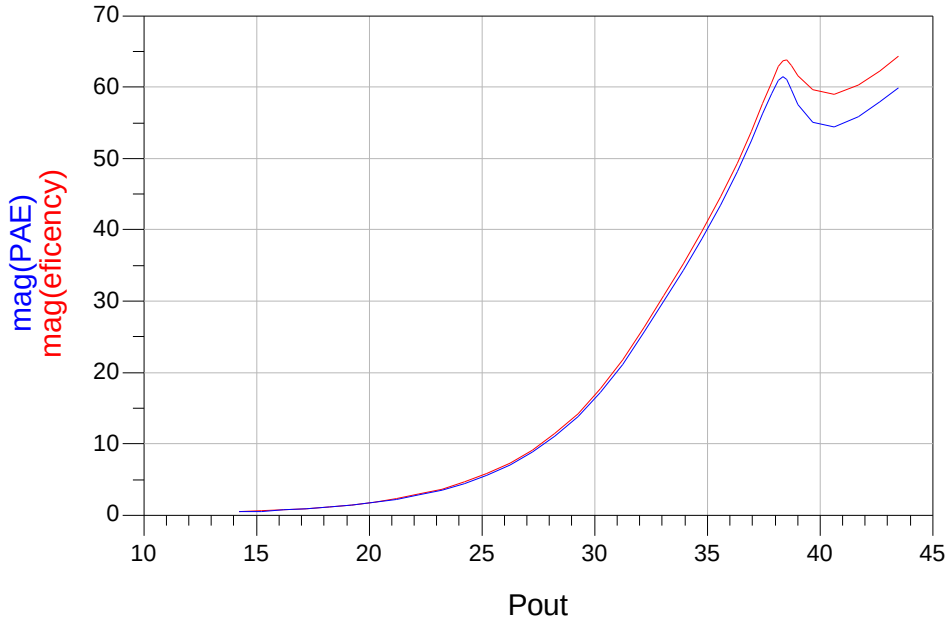

Fig. 12: PAE (blue) and efficiency (red).

- Threshold=25

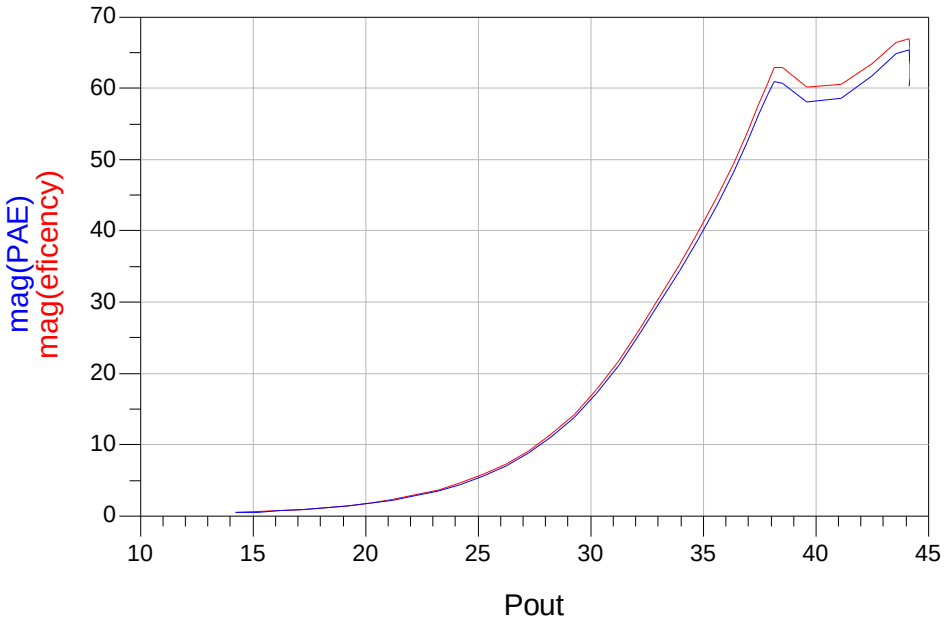

Fig. 13: PAE (blue) and efficiency (red).

- Threshold=20

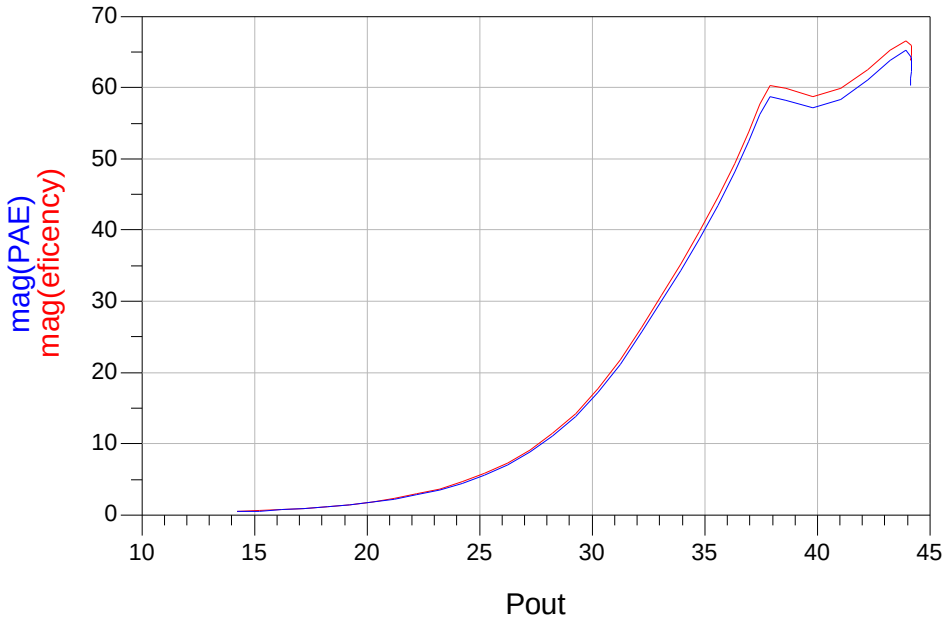

Fig. 14: PAE (blue) and efficiency (red).

- Threshold=10

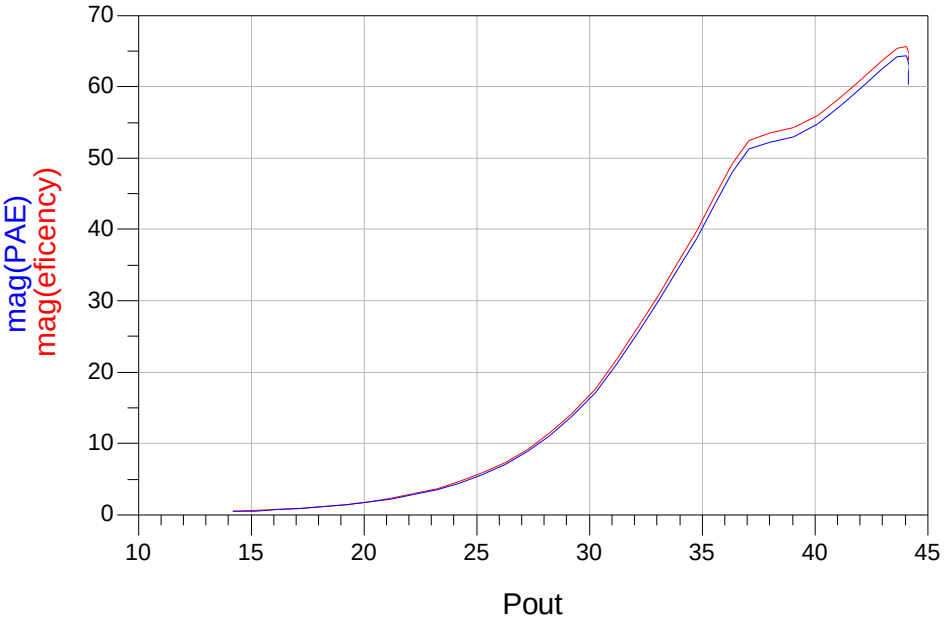

Fig. 15: PAE (blue) and efficiency (red).

- Threshold=5

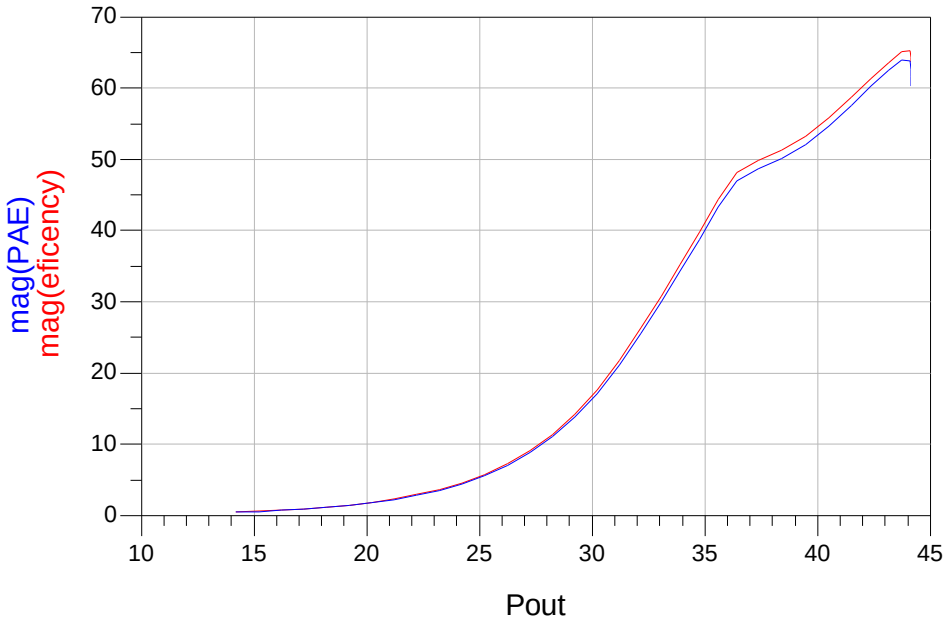

Fig. 16: PAE (blue) and efficiency (red).

- Threshold=0

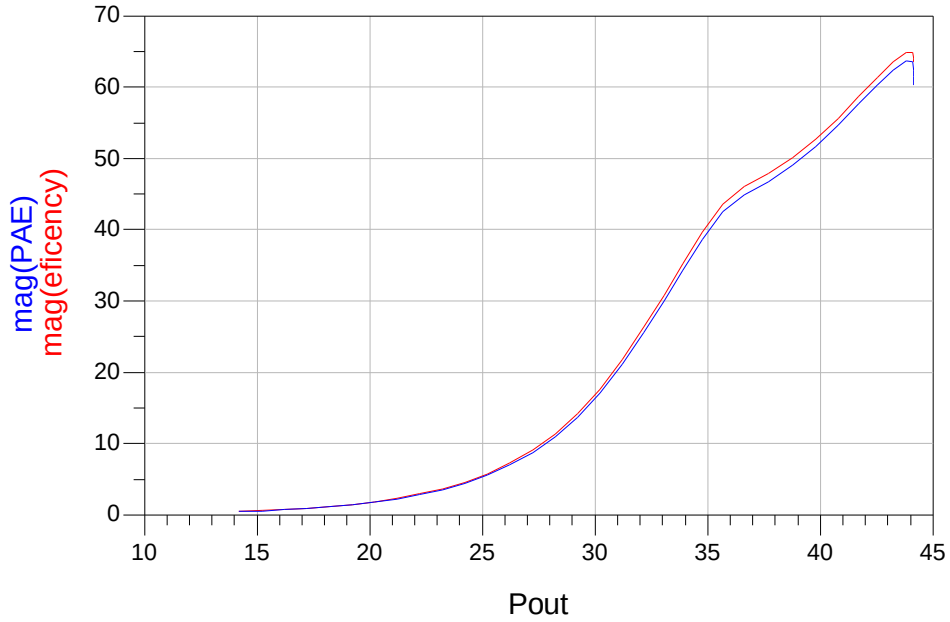

Fig. 17: PAE (blue) and efficiency (red).

3.3.3 Output power

- Threshold=36

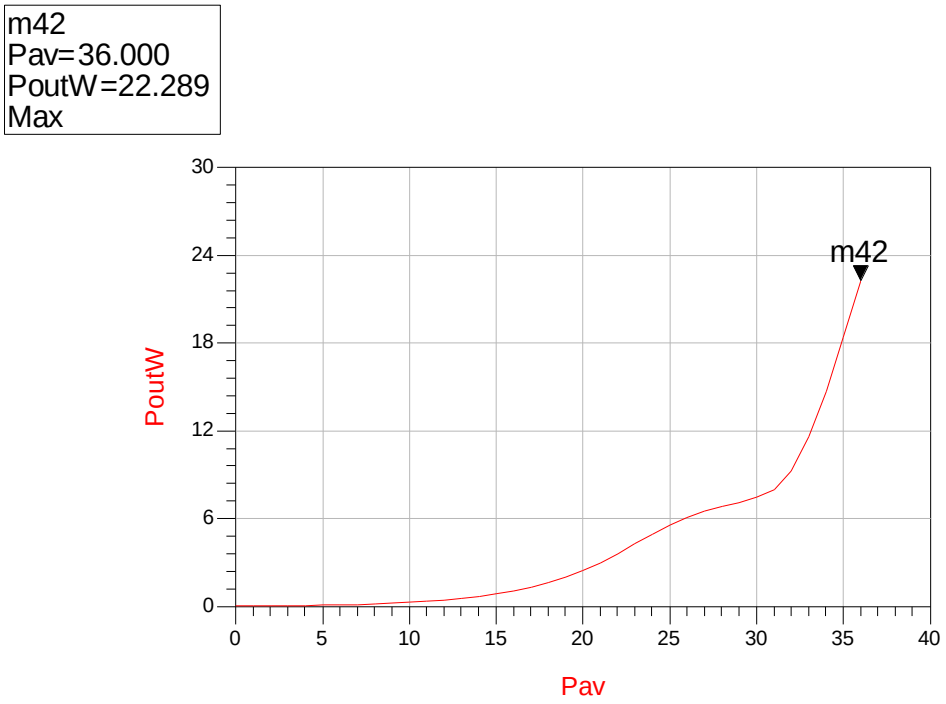

Fig. 18: Output power

- Threshold=25

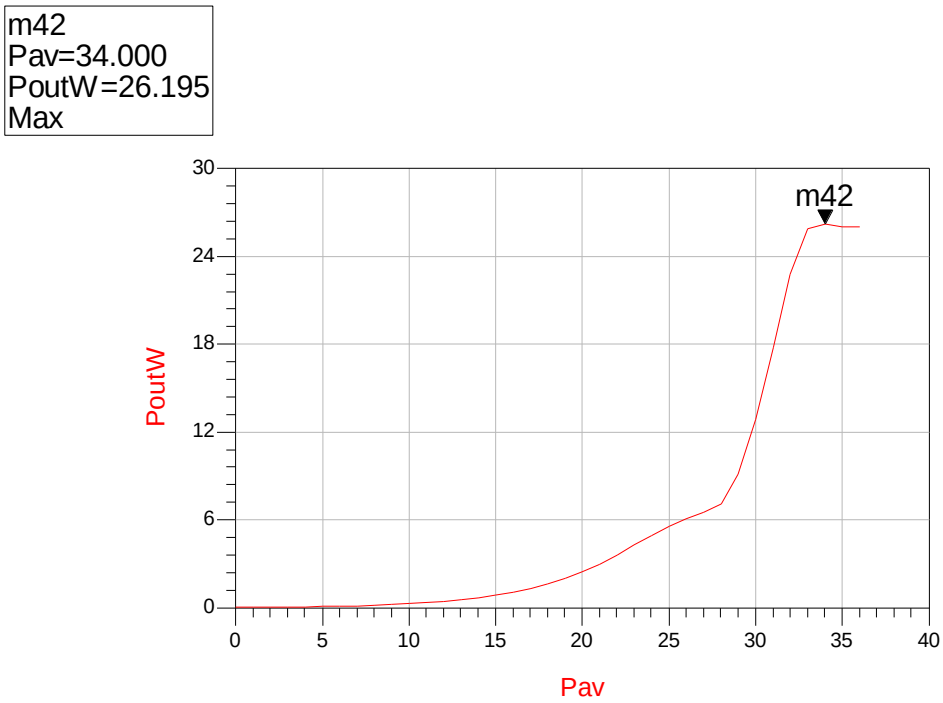

Fig. 19: Output power

- Threshold=20

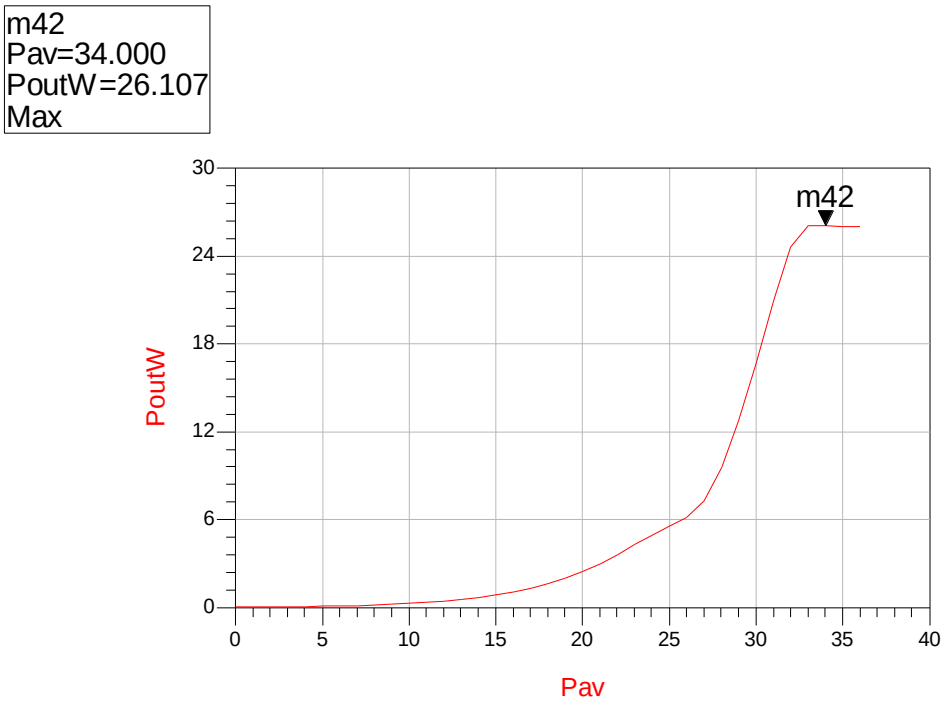

Fig. 20: Output power

- Threshold=10

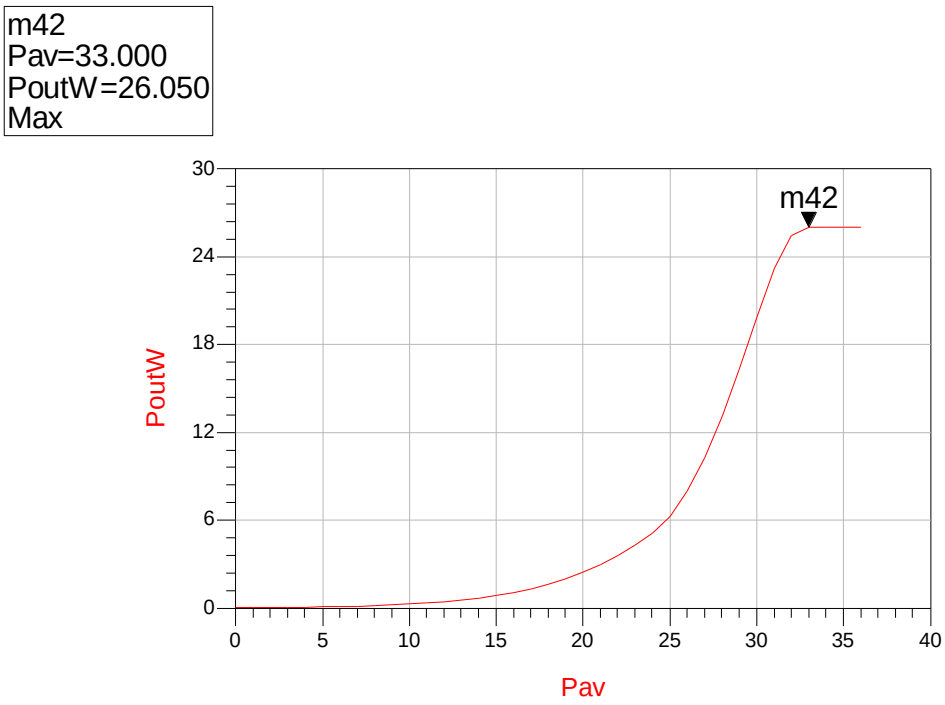

Fig. 21: Output power

- Threshold=5

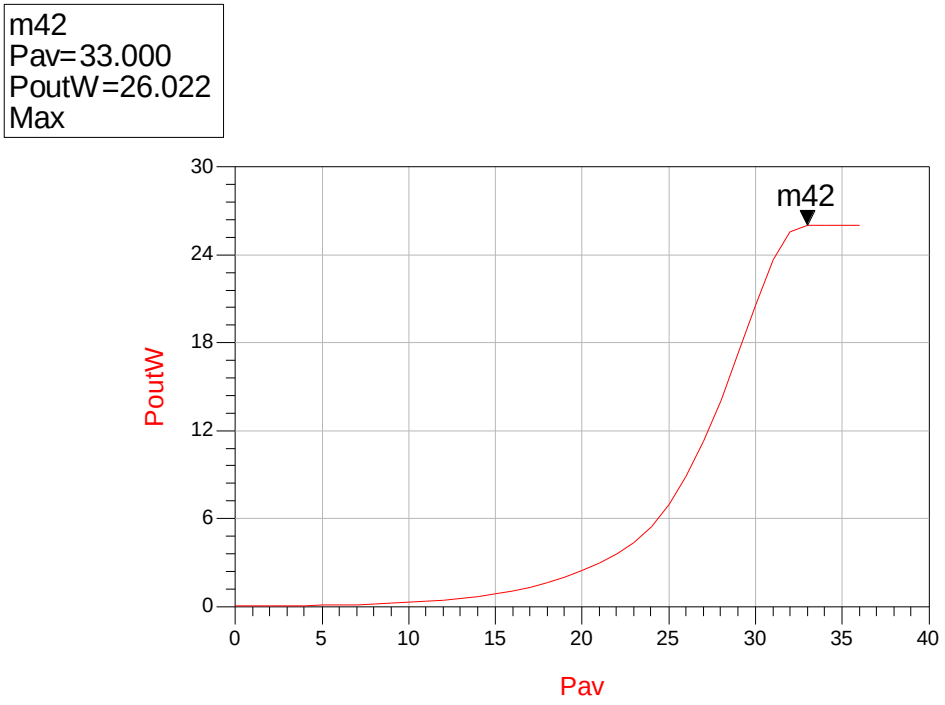

Fig. 22: Output power

- Threshold=0

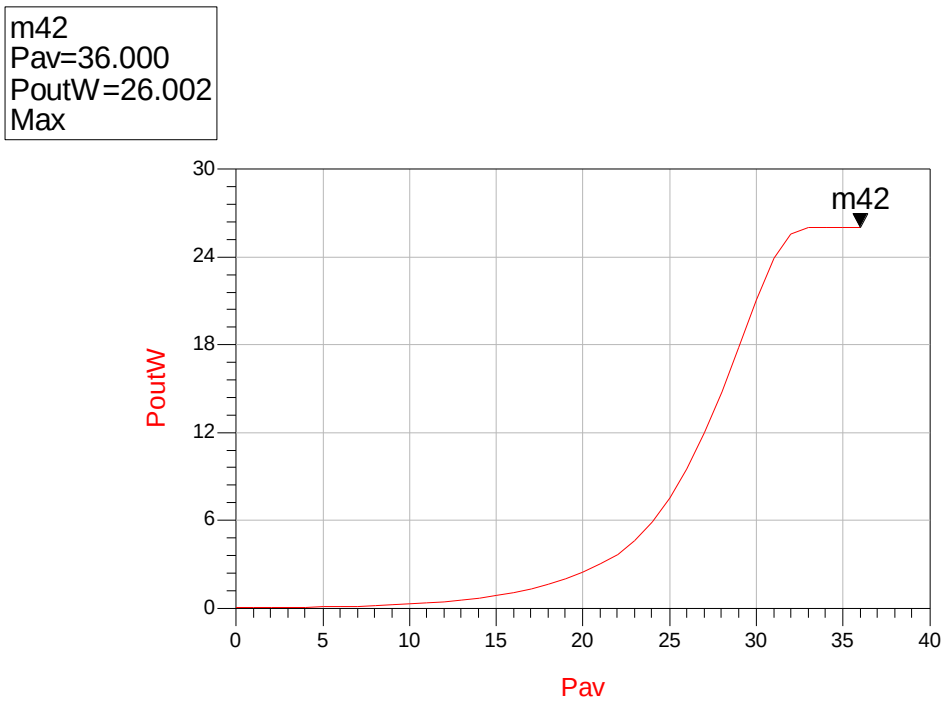

Fig. 23: Output power.

The decrement of the threshold makes the gain and phase become more linear at high input power, but this also makes the efficiency and PAE decrease, especially at back-off. Moreover, the output power increases. This means that is necessary to make a trade-off; so the threshold used is 21.

Using this threshold makes the gain and phase become more linear than the original one, also the maximum gain is 14.389dB.

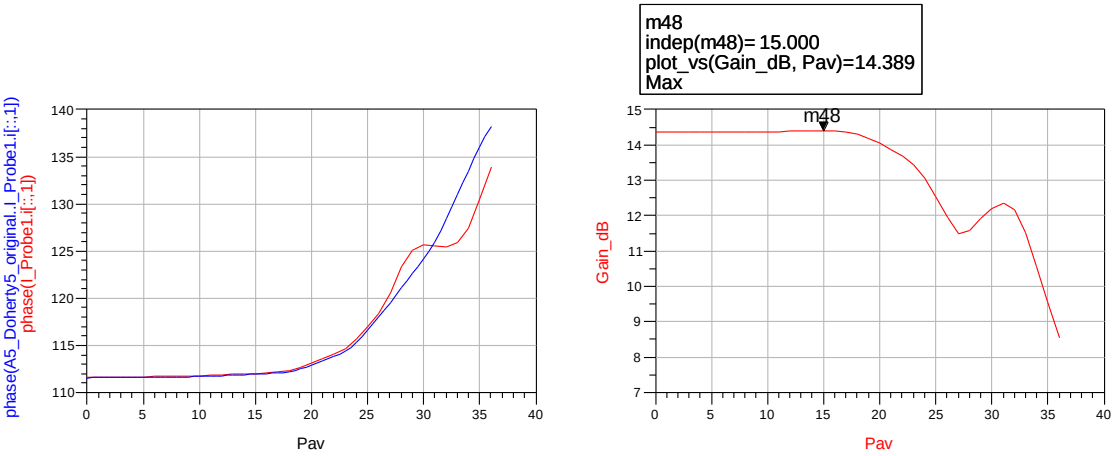

Fig. 24: Phase and gain with the threshold chosen.

The efficiency has a maximum peak of 66.7% and a second peak of 60.9% at 6dB back-off.

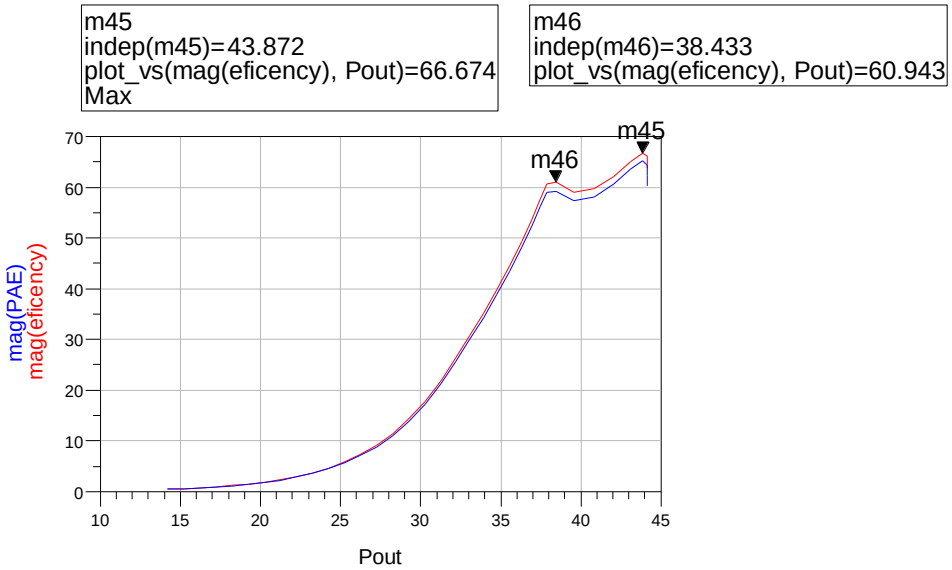

Fig. 25: Efficiency and PAE with the threshold chosen.

Finally, the output power reaches the maximum value of 26 W and saturates with a lower value of the input power.

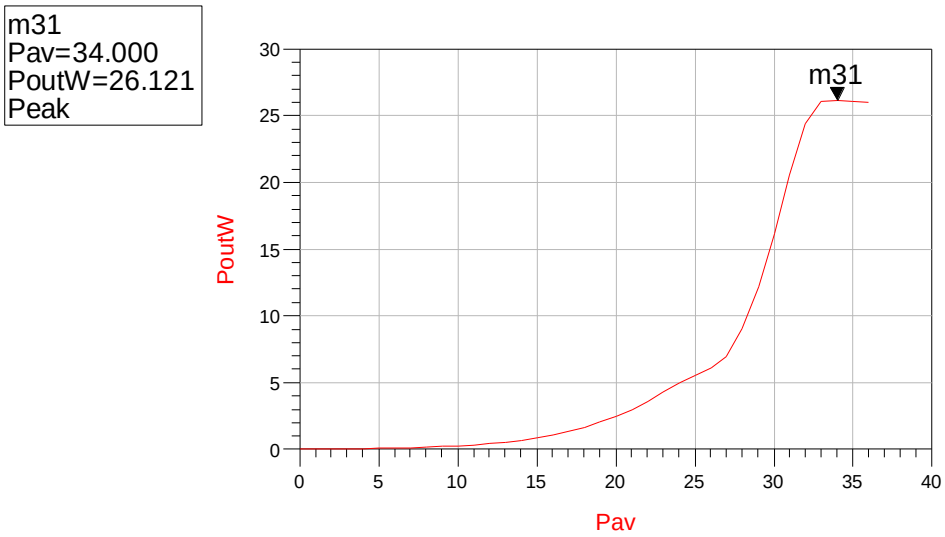

Fig. 26: Output power with the threshold chosen.

3.4 2-tone simulation

2-tone simulation offers a way to see the distortion produced by intermodulation products. The two frequencies taken, are separeted from the RF frequency (3.5 GHz) a certain delta value. Three simulations are made according to different values of delta, 28 MHz, 7 MHz and 1 MHz. The CIMD3 (intermodulation distortion of third order) is the difference between the carrier and the first intermodulation component, the way to calculate it is the one seen in ecuations 3 and 4.

$$f_1 = f_{RF} + \Delta \quad [1]$$

$$f_2 = f_{RF} - \Delta \quad [2]$$

$$CIMD3 = dBm(P_{out}@f_{RF}) - dBm(P_{out}@2f_1 - f_2) \quad [3]$$

$$CIMD3 = dBm(P_{out}@f_{RF}) - dBm(P_{out}@2f_2 - f_1) \quad [4]$$

Pouttotal	CIMD3
16.669	141.748
17.671	137.775
18.672	133.816
19.674	129.875
20.677	125.964
21.679	122.093
22.683	118.280
23.686	114.538
24.690	110.865
25.692	107.191
26.692	103.234
27.686	98.159
28.666	90.224
29.613	78.750
30.523	69.268
31.409	63.209
32.278	59.331
33.124	56.345
33.917	52.705
34.623	47.855
35.230	42.704
35.748	38.076
36.184	34.217
36.611	32.013
37.225	32.859
38.176	35.911
39.322	38.420
40.459	38.335
41.440	36.161
42.149	33.278
42.542	30.301
42.730	27.767
42.833	25.863
42.895	24.493
42.927	23.641
42.934	23.286
42.917	23.341

Pouttotal	CIMD3
17.185	137.149
18.186	133.225
19.188	129.331
20.190	125.482
21.193	121.696
22.196	118.004
23.200	114.446
24.204	111.074
25.207	107.947
26.210	105.075
27.209	102.213
28.202	98.125
29.175	89.694
30.110	77.759
31.011	69.142
31.890	63.718
32.749	59.955
33.571	56.084
34.321	51.015
34.976	45.584
35.540	40.769
36.018	36.835
36.422	33.664
36.797	31.526
37.323	31.896
38.259	35.835
39.437	40.446
40.599	42.649
41.569	40.514
42.248	35.274
42.636	29.726
42.852	25.589
42.974	22.854
43.032	21.222
43.045	20.377
43.028	20.040
42.987	19.982

Pouttotal	CIMD3
17.220	135.751
18.222	131.855
19.223	127.997
20.226	124.196
21.229	120.477
22.232	116.877
23.236	113.451
24.240	110.278
25.244	107.463
26.247	105.119
27.247	103.203
28.240	100.623
29.215	93.087
30.152	80.616
31.055	71.585
31.934	65.926
32.794	61.931
33.615	57.711
34.360	52.306
35.012	46.684
35.572	41.782
36.048	37.799
36.449	34.588
36.818	32.306
37.336	32.312
38.267	36.110
39.441	41.231
40.601	44.451
41.576	42.881
42.263	37.179
42.665	30.916
42.889	26.084
43.004	22.836
43.043	20.853
43.034	19.642
42.988	18.858
42.913	18.330

Fig. 27: CIMD3 for delta 28Mhz 7MHz and 1MHz, respectively.

As seen in figure 27 the lowest CIMD3 value is 18.33dB for an intermodulation separation of 1MHz and the maximum output power.

3.5 The most linear gain

A study is made to calculate which values of Vgs make the gain as flatter as possible; it is taken a separation of 5dB in Pav. The result can be seen in figure 28. This result is convenient in gain, but makes the efficiency drop, and lead to a function that is very difficult to implement. Also, if the current supplied by the main amplifier changes, the function also changes.

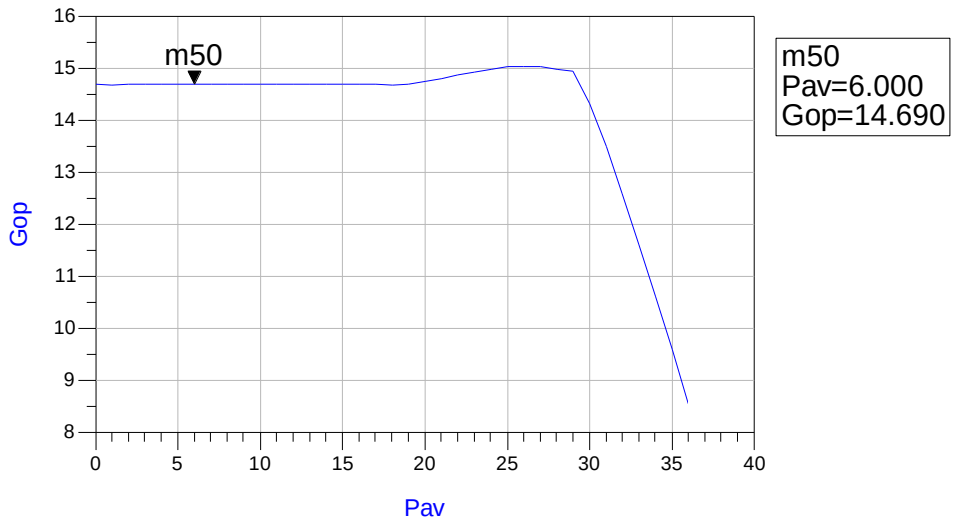

Fig. 28: Gain applying the point to point function.

3.6 Bias tee

Another important step is to design and check the bandwidth of the bias tee, which is going to be set in the Vgs feeding port. The way to measure it, is to compare the signal injected into the bias tee and the signal seen at the peak's gate. To obtain a more realistic and a no resonances result in the simulation, it is necessary to add the generator internal resistor. With this configuration the bandwidth is 13.5MHz. One way to increase this value is to put a parallel resistor, taking into account that the signal is attenuated. For example, with a parallel resistor of 50Ω, the bandwidth is 25.6MHz, and the attenuation is 6dB.

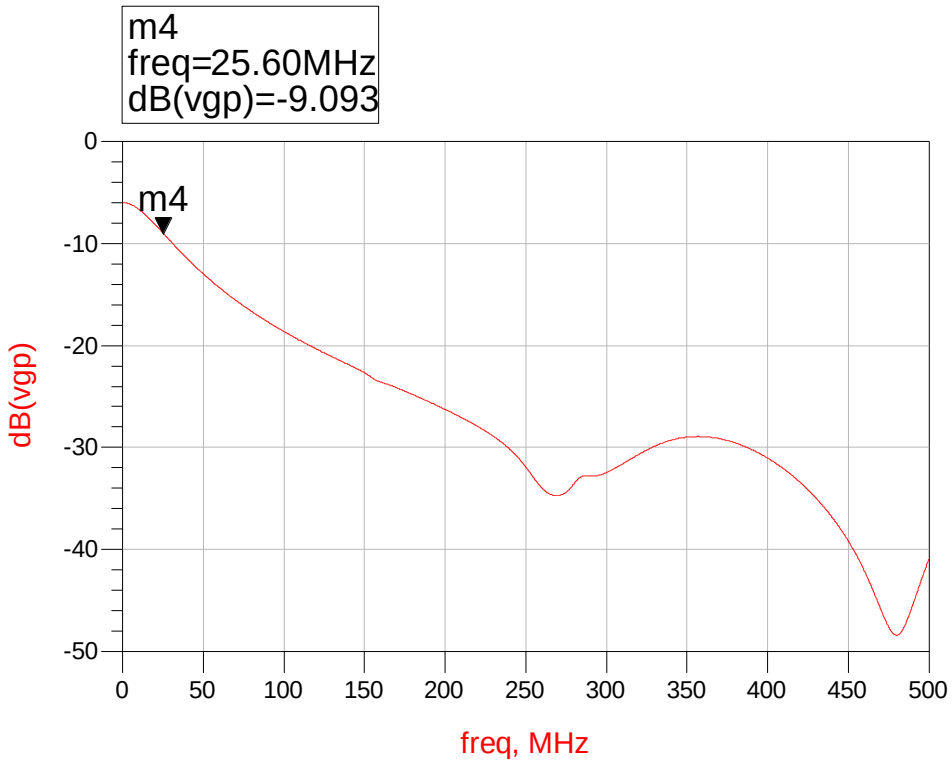

Fig. 29: Signal seen at the gate with a resistor in parallel.

3.7 Stability

The K factor (Stabfact1) allows obtain how far the circuit is from behaving unstable, if k>1 the circuit is in the stability zone.

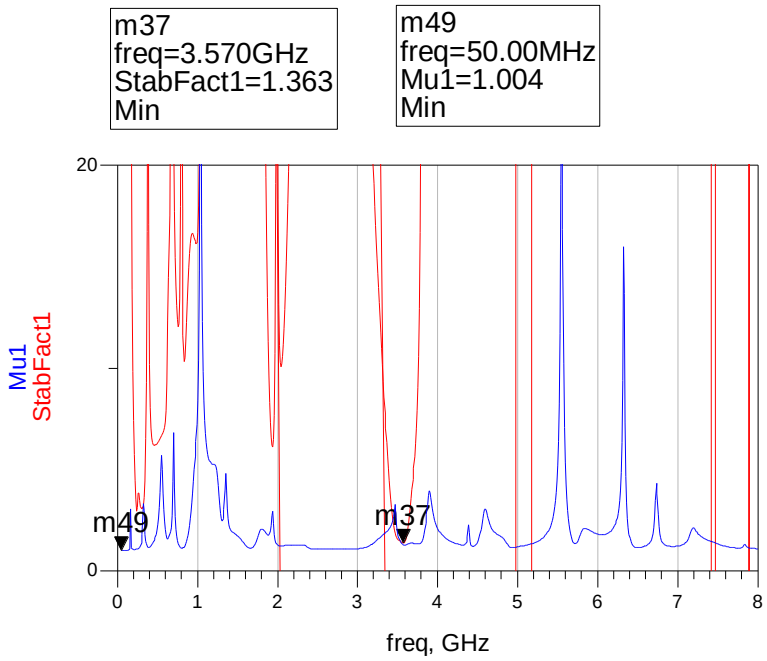

Fig. 30: K factor from 50 MHz to 8 GHz.

Another way to check which Γ_S and Γ_L values lead to instability, are the stability circles. The figure 31 shows that any value of Γ_S and Γ_L makes the circuit stable.

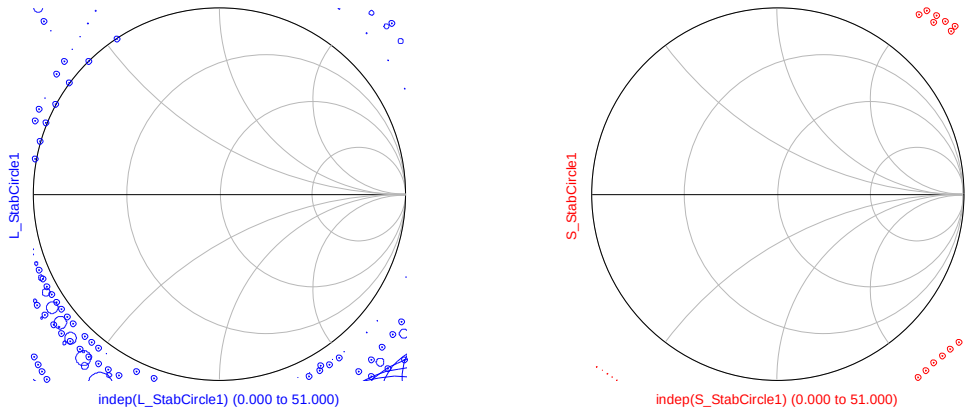

Fig. 31: Stability circles.

3.8 Matching networks

Both input and output must be adapted in order to obtain the best performance at the central frequency (3.5 GHz). The original design was already adapted, and with the changes made, the hybrid, it is only necessary to adjust a little bit the input lines.

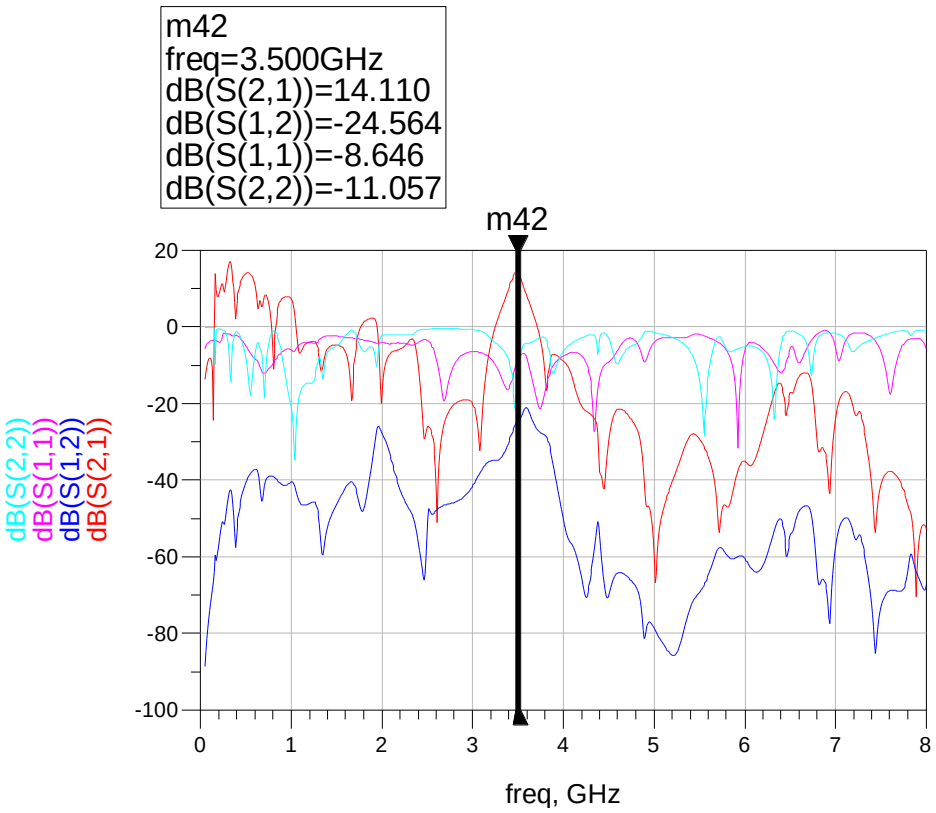

Fig. 32: S parameters.

3.9 Layout

Once all the designs and simulations are done, it is time to do the layout. One thing changed from the design is the dual feed in the peak and main's bias gate. This must allow feed the gate with a SMA connector or with soldered microstrip paths, as seen in figure 33.

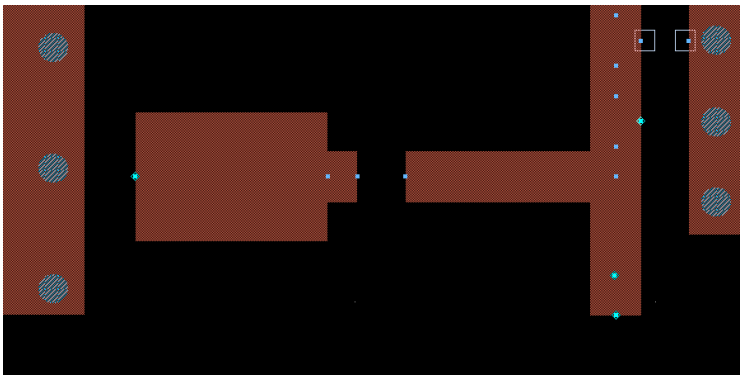

Fig. 33: Detailed view of the peak's bias.

The microstrip circuit used is a Taconic substrate with copper metallization (RF35 with εr=3.5, H=0.76mm and T=0.035 mm).

The size of the final circuit is 105x129 mm (Figure 34).

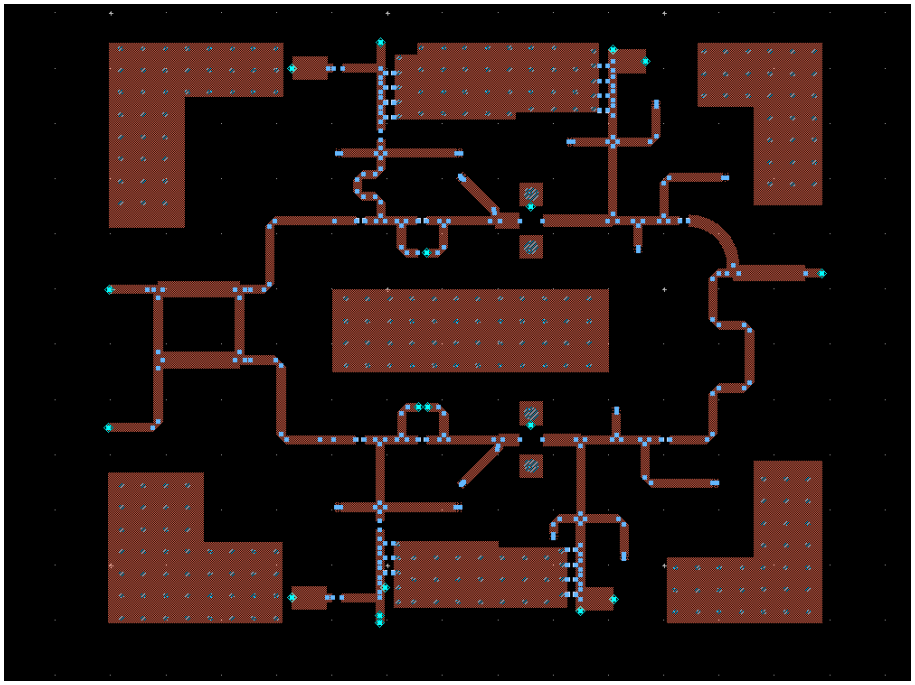

Fig. 34: Complete layout.

3.10. Momentum Simulations

The changes made in the original design show the necessity of being checked whit momentum, the electromagnetic simulator of ADS. The most critical parts are the hybrid (figure 35) and the line set in the input second harmonic tuner of the main (figure 37).

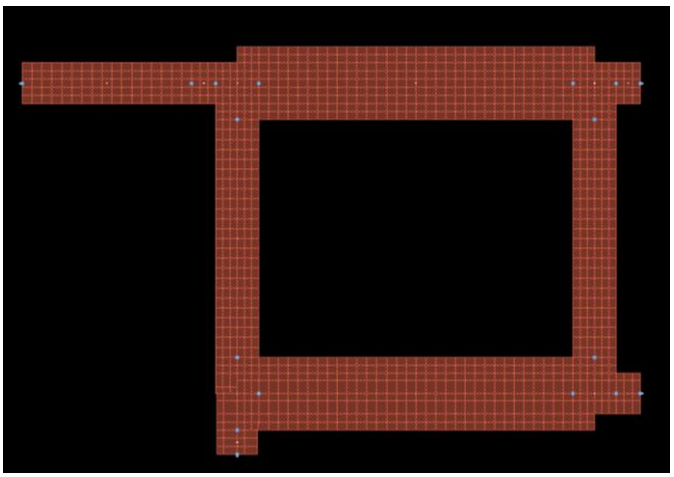

Fig. 35: Hybrid layout's.

A mesh frequency of 21GHz is taken and a mesh density of 20 cells/wavelength. It is made adaptive S-parameters simulation, the band taken is from DC to 21GHz with 30 points/step.

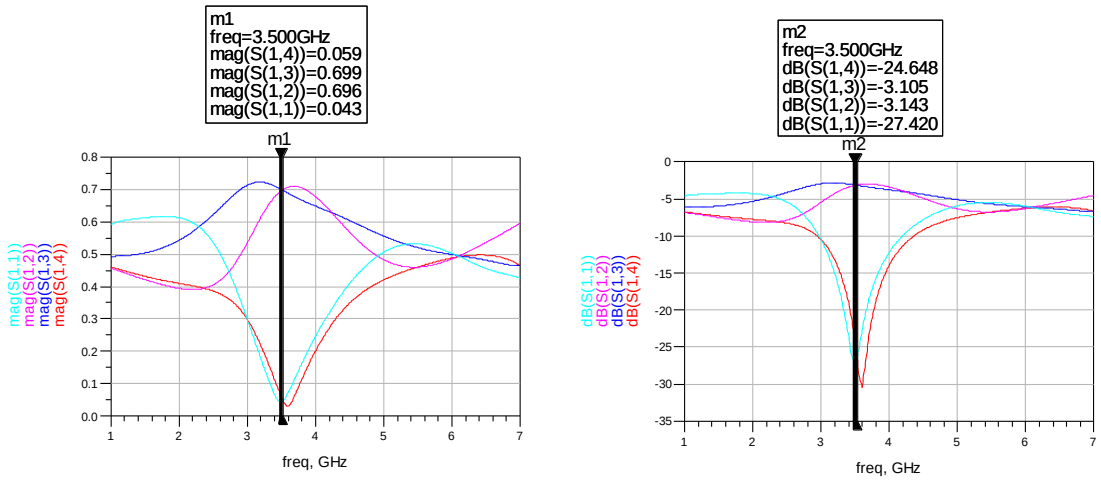

Fig. 36: Results of the hybrid using momentum.

The momentum simulation shows that the power delivered to the main and peak falls in 0.1dB, which is not a significant decrement.

The other electromagnetic simulation done is the line set in the input second harmonic tuner of the main.

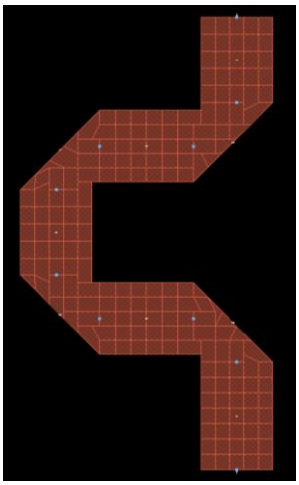

Fig. 37: Line's layout.

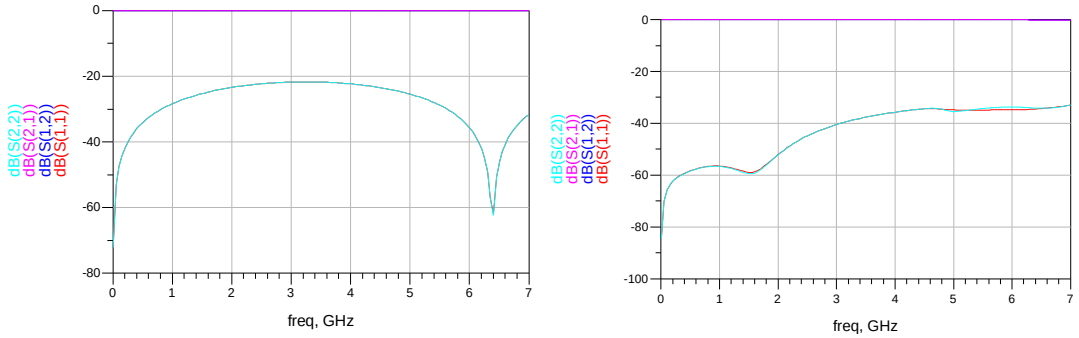

Fig. 38: Simulation of the original line vs. momentum simulation

The results do not change so much, S21 and S12 remain at a 0dB level and S11 and S22 below -20dB.

4. Comparison between both designs

In order to adapt the design made by Jorge Moreno Rubio for its Ph.D. thesis to a bias tuning configuration, some changes are made. In this section we are going to make a deeper analysis to all this changes.

4.1 Hybrid

The optimized input divider ratio of the original hybrid was found to be 42% for the main, and 58% for the peak. Nevertheless, the hybrid used for bias tuning delivers the same power to both amplifiers. To achieve this all the lines that compose the hybrid were changed.

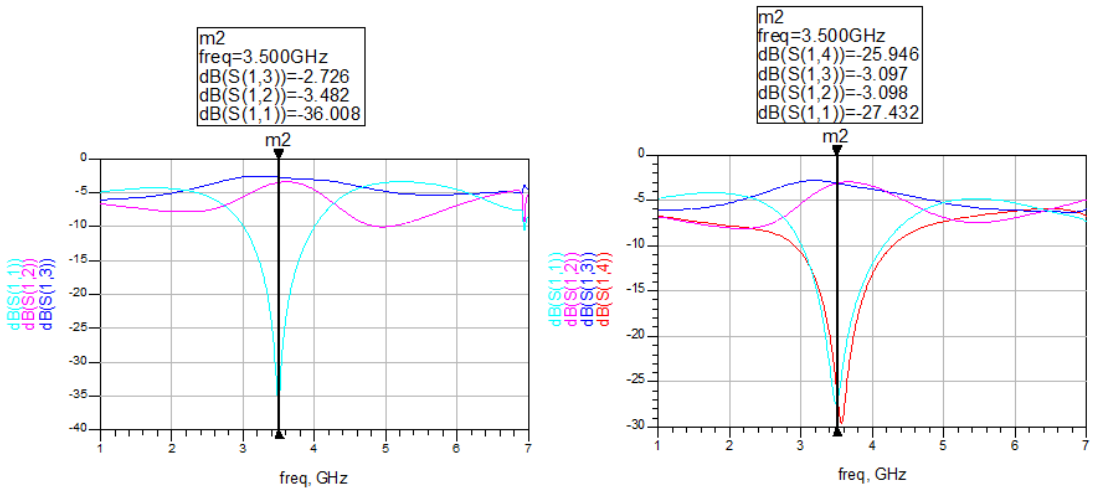

Fig. 39: Original results vs. bias tuning results.

4.2 Bias tee

As has been mentioned before, the bias tuning configuration has of two ways of feeding in the peak and main's bias gate. This must allow feed the gate with a SMA connector or with soldered microstrip paths. The original DPA design only allows feed through soldered paths.

To obtain a higher bandwidth on the bias tee at the peak amplifier, the capacitor with the highest value was removed; also the two 50 Ω resistors were changed with a 20 Ω resistor.

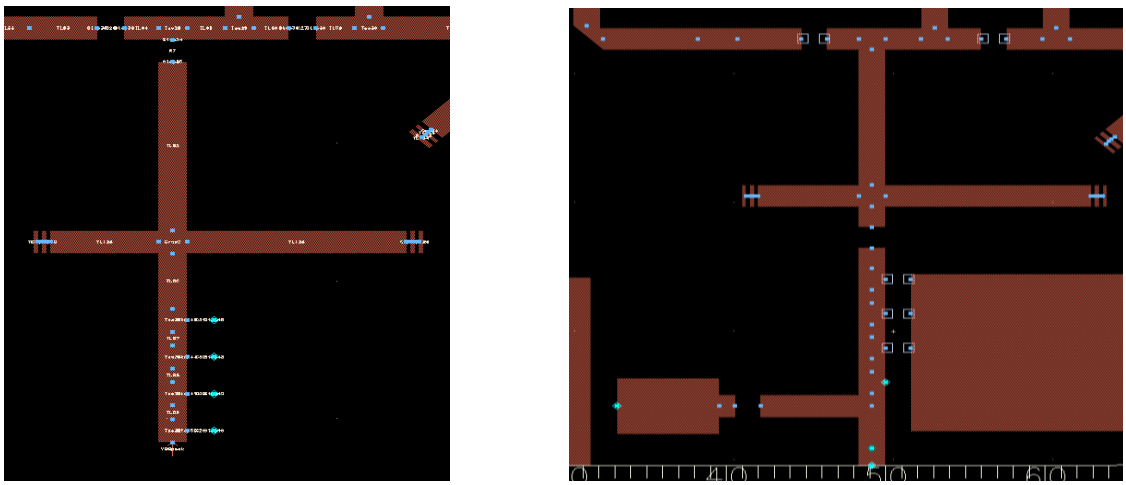

Fig. 40: Original layout vs. bias tuning layout.

4.3 Second harmonic tuning

Due to the changes made in the hybrid and the bias tee, the length of the input lines in the second harmonic closers (Figure 41), were adapted to obtain the same circuit size in both designs and having a good matching and power performance.

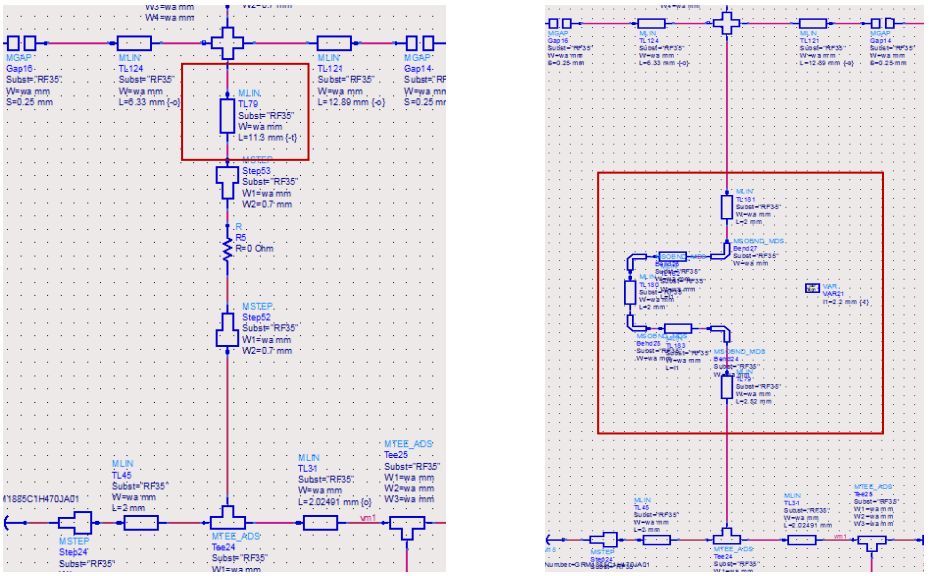

Fig. 41: Original main's input line vs. bias tuning main's input line.

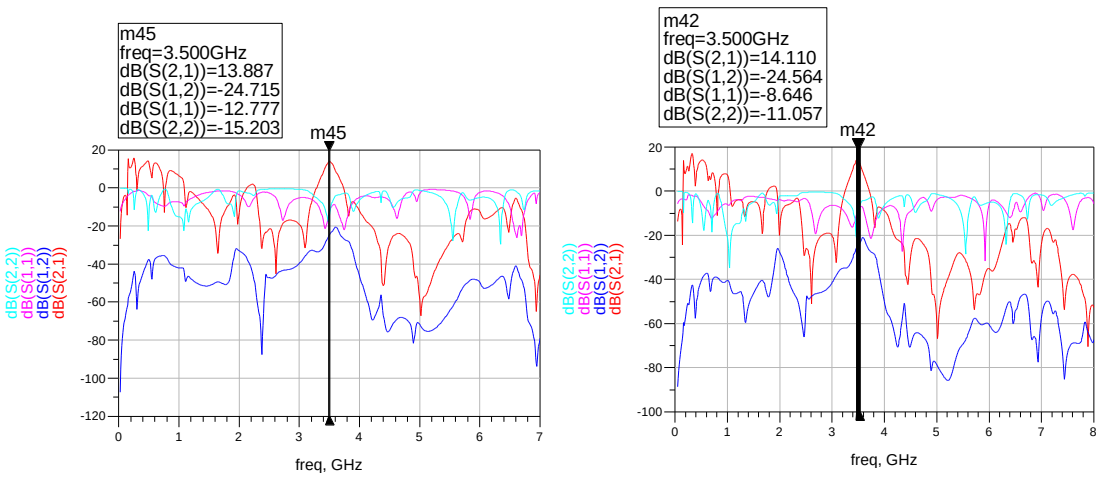

Fig. 42: Original s-parameters vs. bias tuning s-parameters.

5. Measurement

5.1 First measures

The first step on the measurement is to see if the transistors are working fine, and set the bias working point. It is used a DC power source with four channels, channel one for the main's Vgs, channel two for the peak's Vgs, channel three for the main's Vds and channel four for the peak's Vgs. Two amp meters measure the Ids from the main and peak and four voltmeters to measure the different Vgs and Vds.

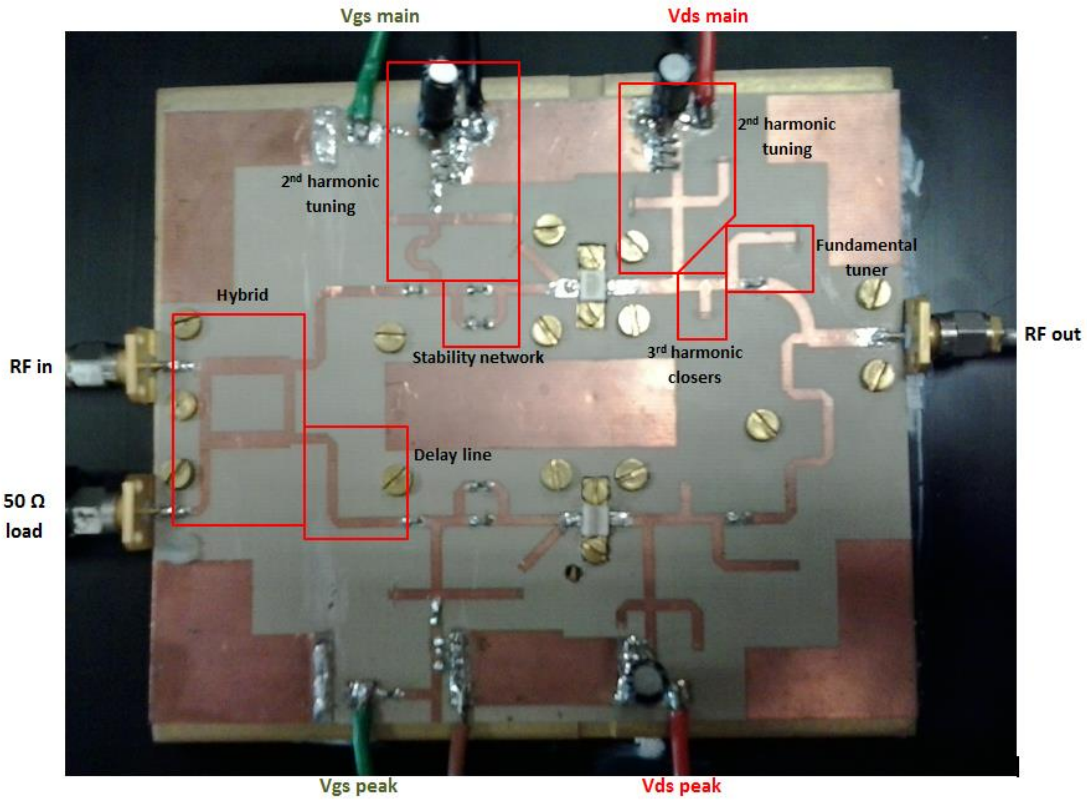

Fig. 43: Picture of the fabricated DPA with the most important parts highlighted.

Setting the Vds at 28V, and varying the Vgs, the results obtained show the transistor starts to supply Ids current above a Vgs=-3.2V, so the value taken to set the transistor off is a Vg=-3.5V. The transistor reaches a Ids=200mA with a Vgs=-2.75V

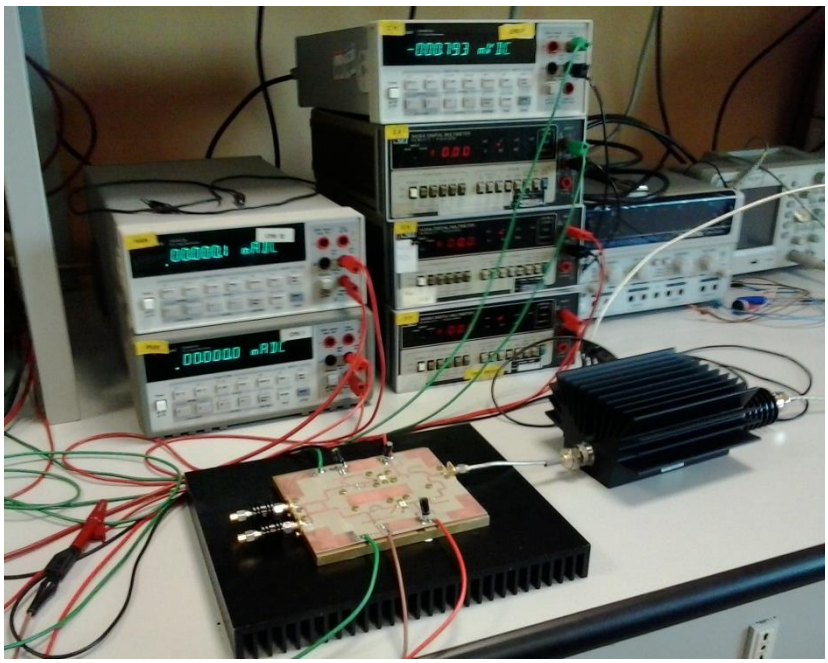

Fig. 44: DC work station

5.2 Spectrum analyzer measures

Next step is to connect the DPA to a RF signal generator and to a Spectrum analyzer and do all the power measurements. The measure bench is set as seen in figure 40, so to extract the Pin and Pout is necessary to calibrate first the work station. It is needed to set the value for the A, B and C parameters as seen on figure 46 and equations [5], [6] and [7].

$$P_{out\ VSA} = P_{out} + B \quad [5]$$

$$P_{in} = P_{in\ ESG} + A \quad [6]$$

$$P_{in\ VSA} = P_{in} + C \quad [7]$$

This is a first approach to see how the DPA is working, future measurements with the network analyzer will give a more accurate characterization of the behaviour of the DPA.

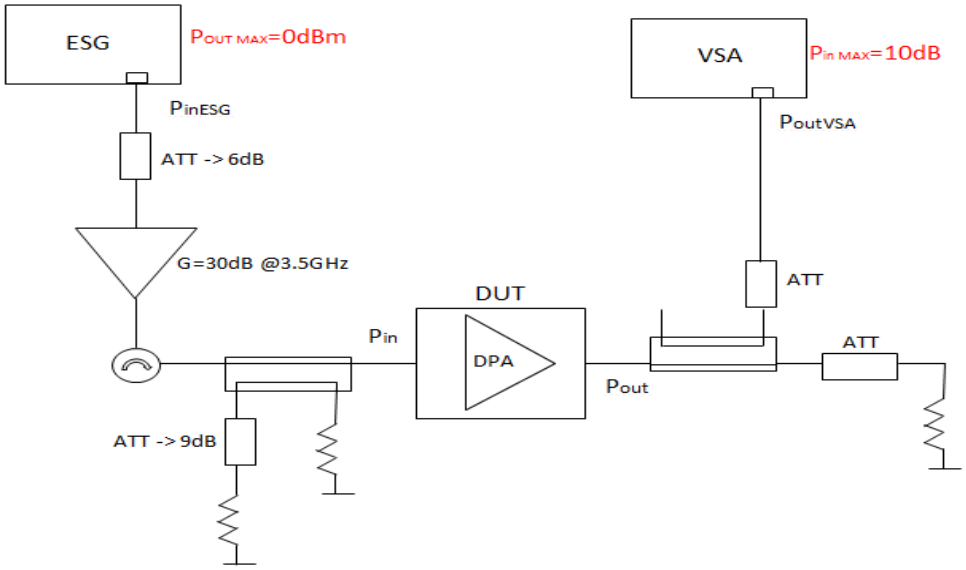

Fig. 45: Measure bench diagram.

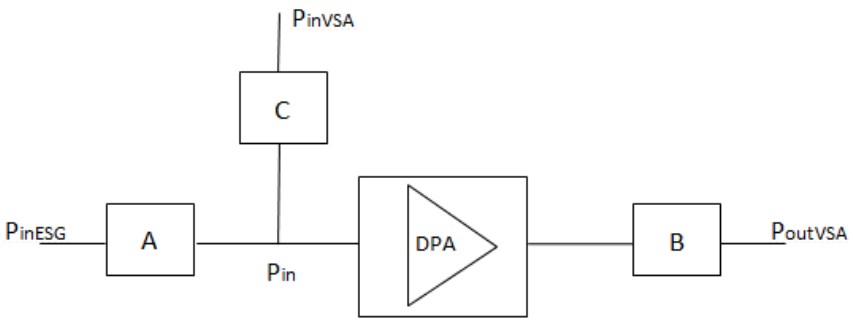

Fig. 46: A, B and C parameters diagram.

With a quick analysis it is noticed that the optimum frequency is shifted to 3.35 GHz (figure 47).

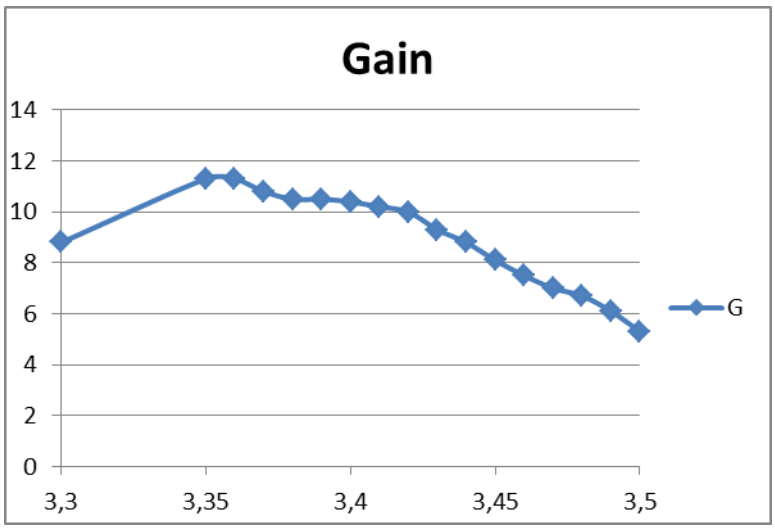

Fig. 47: Gain measure varying the frequency.

After setting this frequency value, it is time to understand how the polarization point changes the DPA performance.

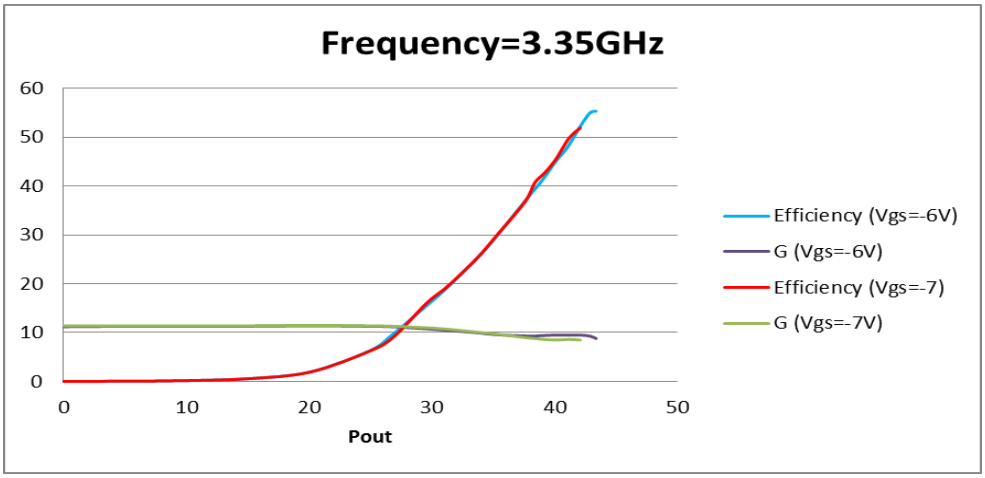

Fig. 48: Gain and efficiency with different peak's Vgs.

With a higher Vgs on the peak, the efficiency is higher and the gain is more linear, because the peak is set on with a lower Pin.

5.3 Network analyzer measures

The network analyzer allows us to make a deeper analysis of the system, after a previous accurate calibration.

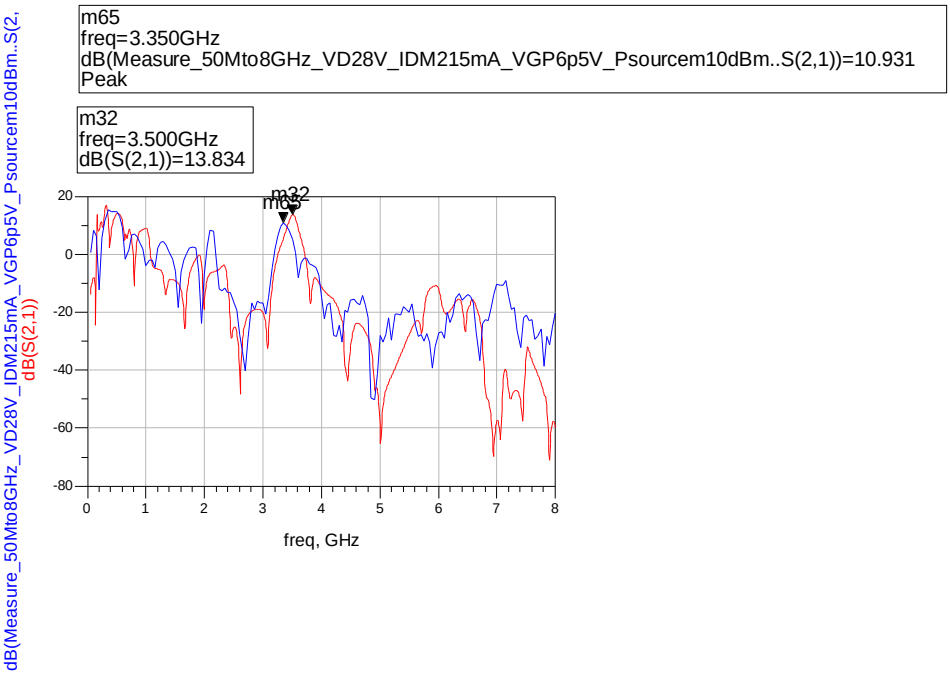

Fig. 49: S21 simulated (red) versus S21 measured (blue).

The S parameters measurements confirm the initial suspicion; the circuit is shifted in frequency, from 3.5GHz to 3.35GHz.

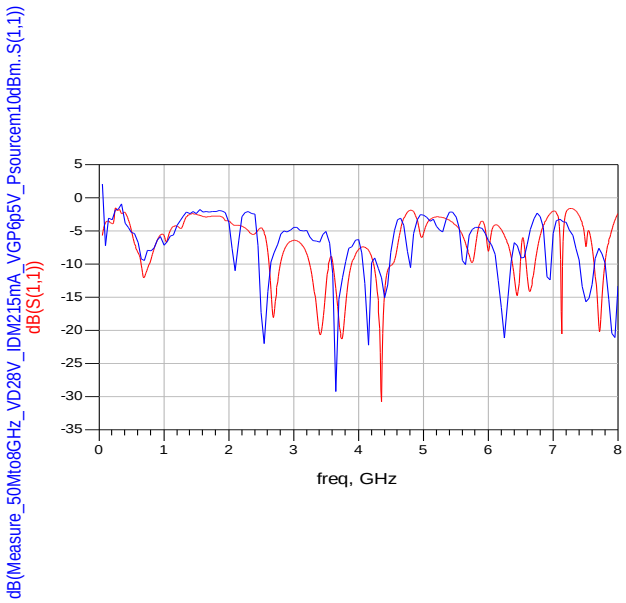

Fig. 50: S11 simulated (red) versus S11 measured (blue).

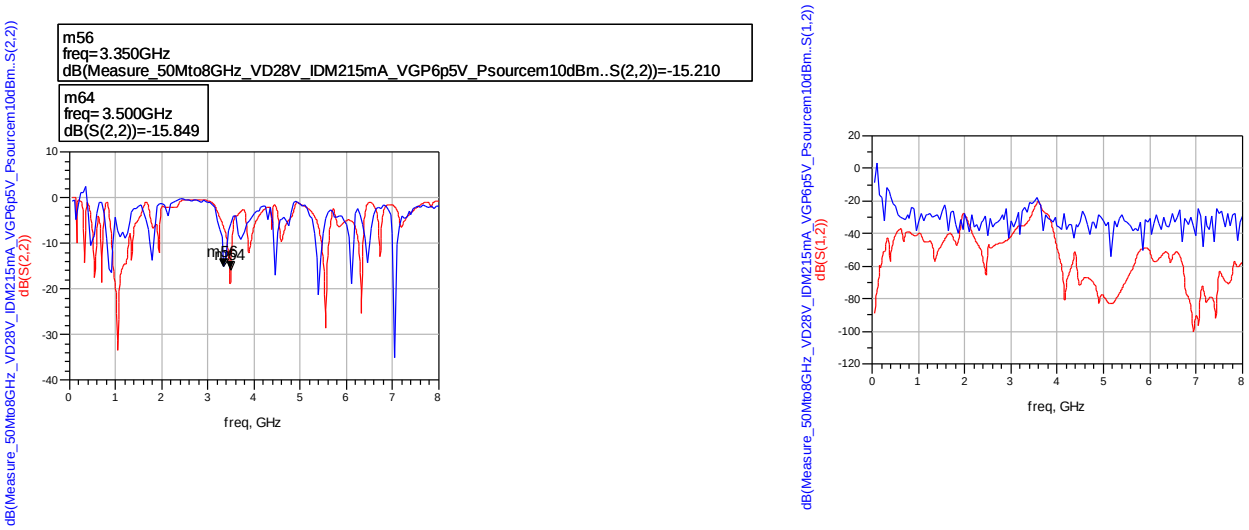

Fig. 51: S22 and S12 simulated (red) versus S22 and S12 measured (blue).

Once the S-parameter analysis is made, a power sweep measurement is performed.
The DPA has been characterized at different frequencies and bias conditions.

5.3.1 Frequency sweep

Setting a bias point of Vds=28V, Vgs_peak=-6.5V and Id_main=210mA, and sweeping the frequency.

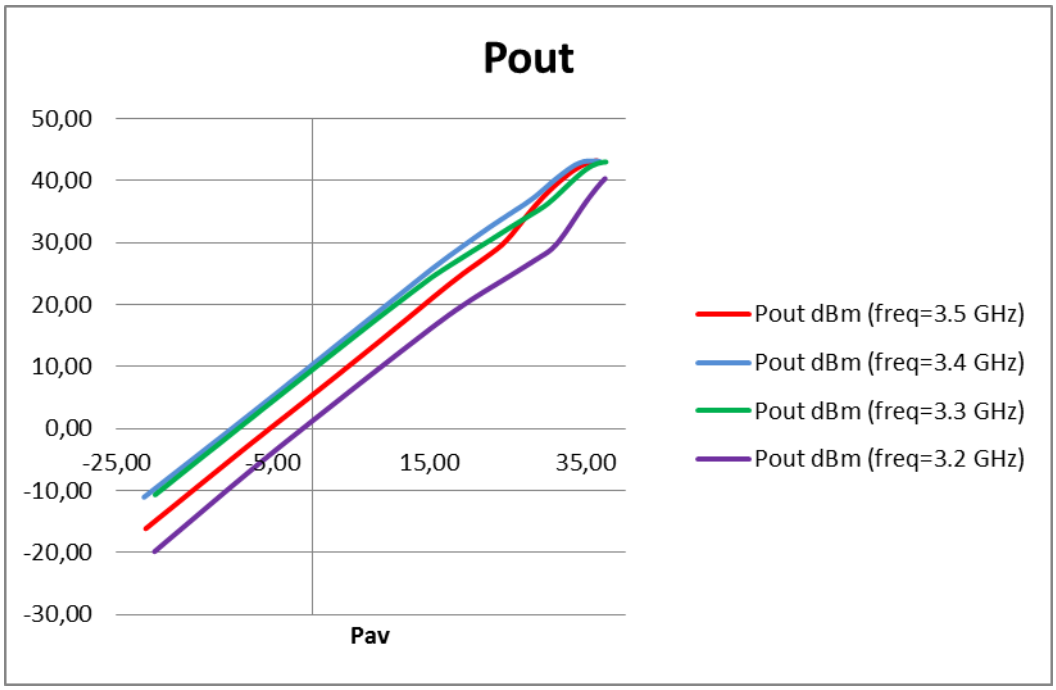

Fig. 52: Pout for the different frequencies.

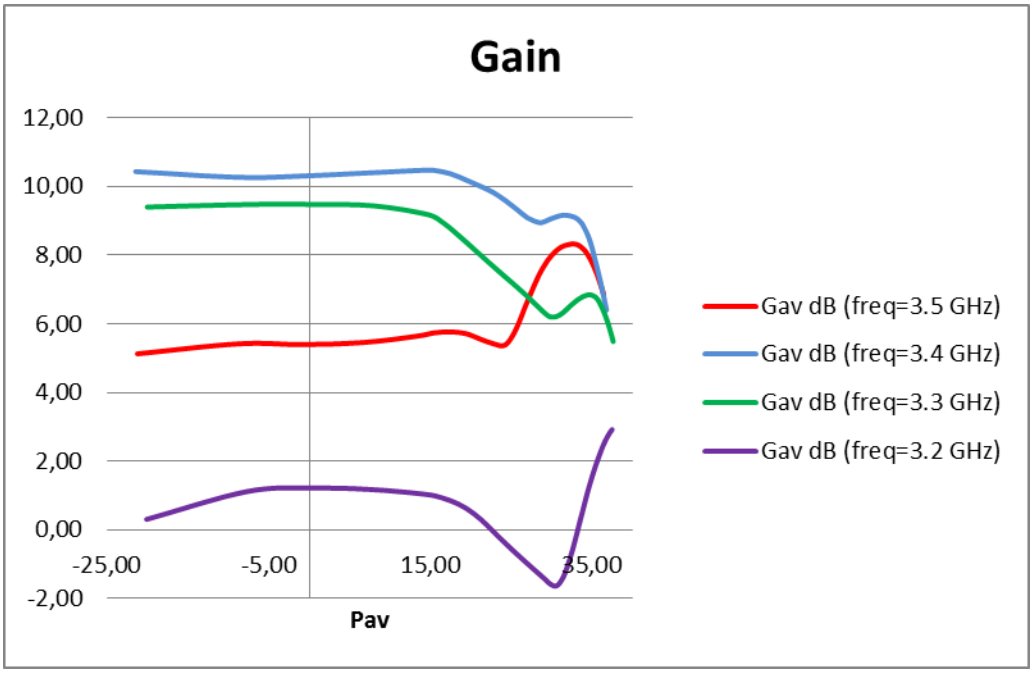

Fig. 53: Gain for the different frequencies.

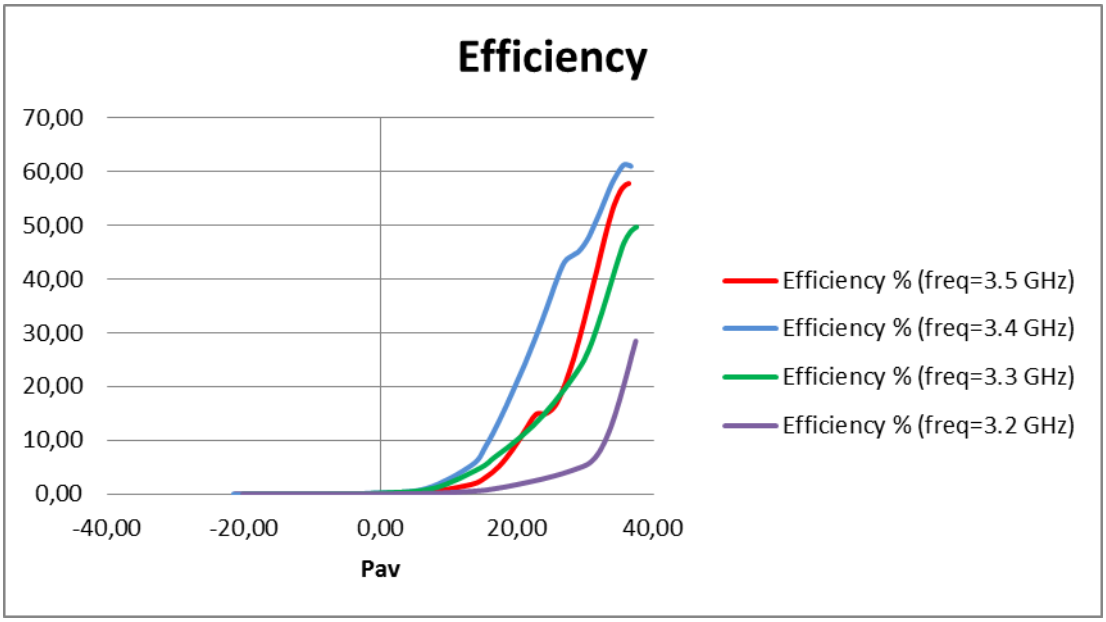

Fig. 54: Efficiency for the different frequencies.

The best performance measured is at 3.4 GHz, the output power is higher, the gain is higher and more linear and the efficiency is higher: moreover, the Doherty effect at back off is noticeable.

5.3.2 Frequency 3.5 GHz

Setting a bias point of Vds=28V, Id_main=210mA and changing the values of Vgs_peak, -6.5V, -8V and -10V.

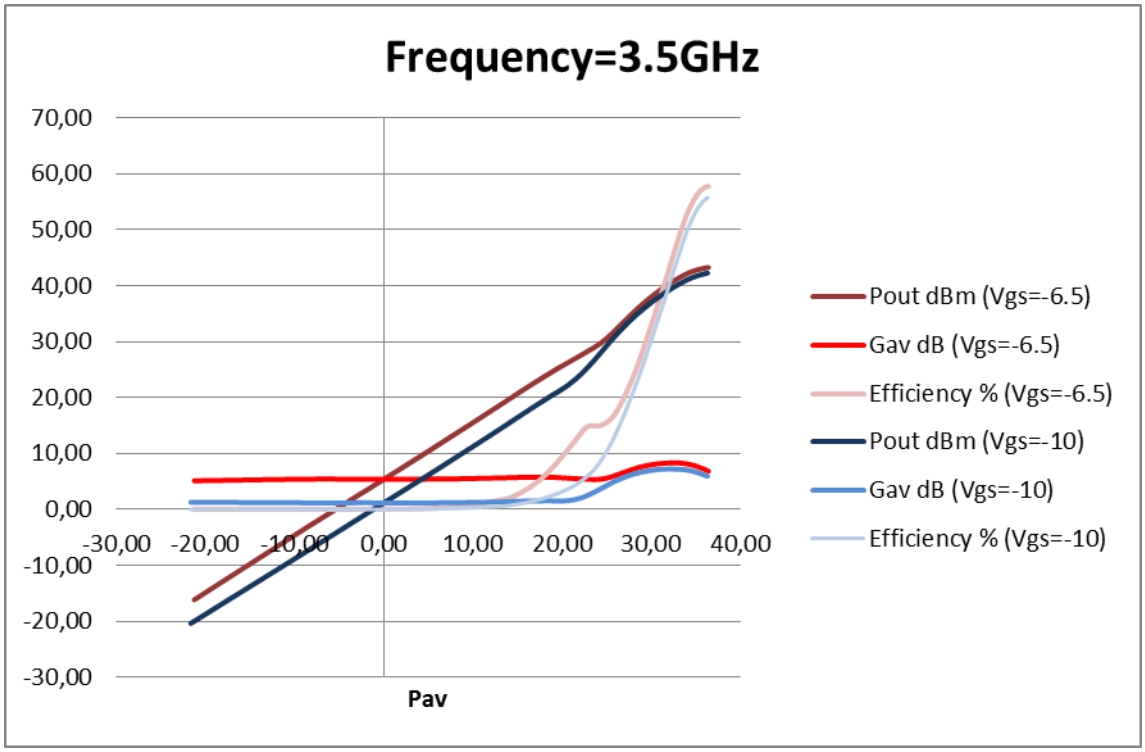

Fig. 55: Results for the different Vgspeak.

5.3.3 Frequency 3.45 GHz

- Setting a bias point of Vds=28V, Vgs_peak=-6.5V, and changing the values of Id_main 210mA and 50mA.

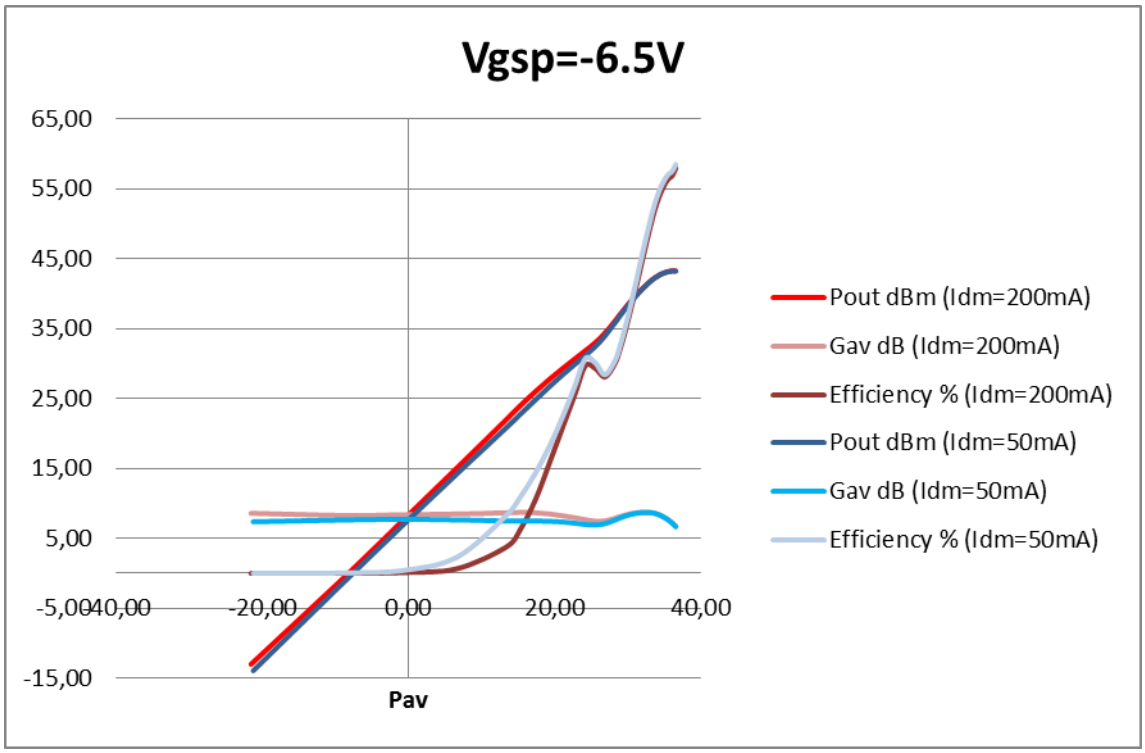

Fig. 56: Results for the different Idmain.

- Setting a bias point of Vds=28V, Id_main=210mA and changing the values of Vgs_peak, -6.5V, -8V and -10V.

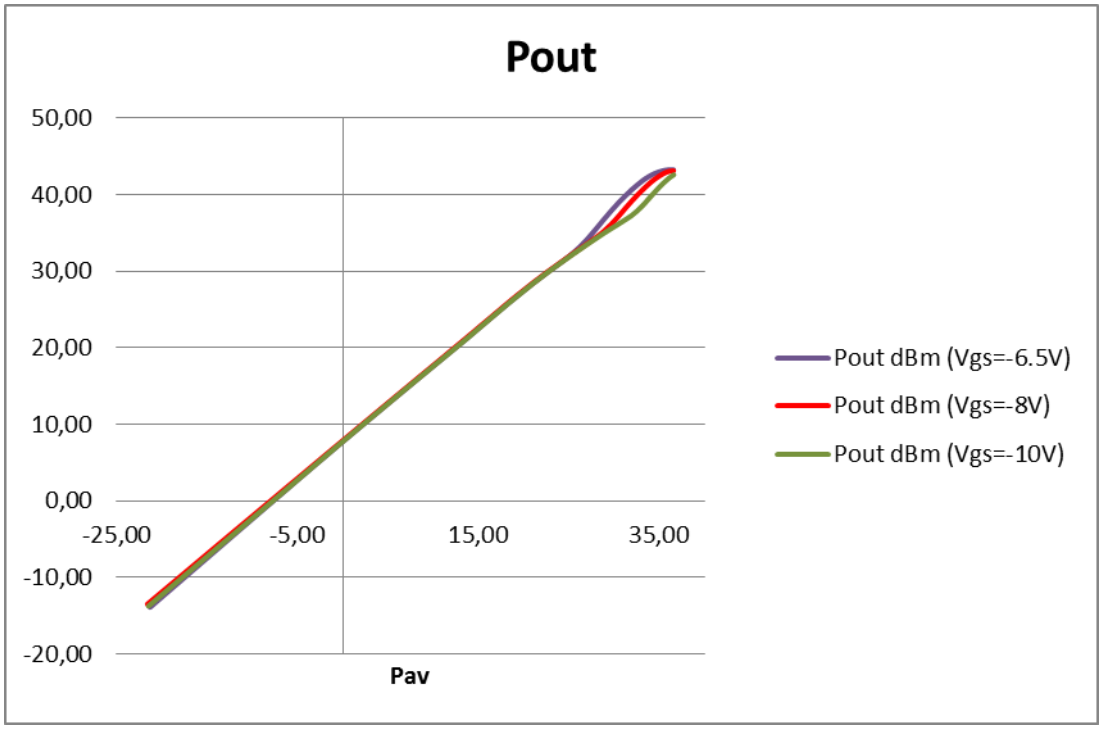

Fig. 57: Output power for the different Vgs.

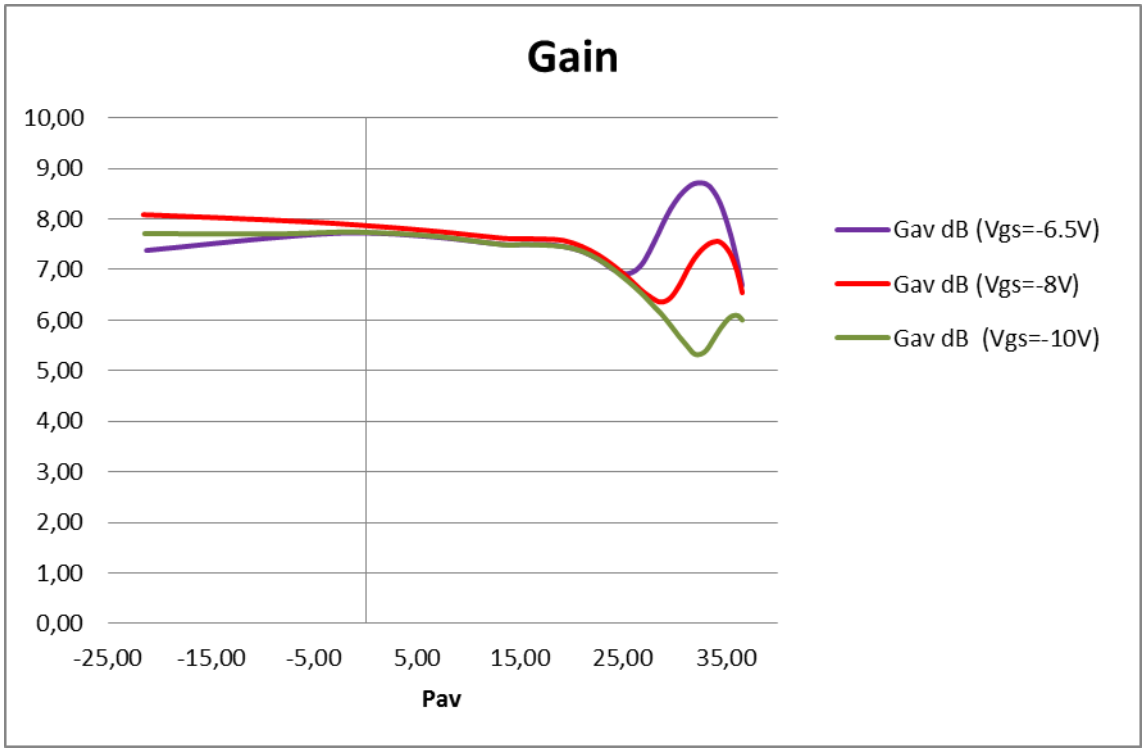

Fig. 58: Gain for the different Vgs.

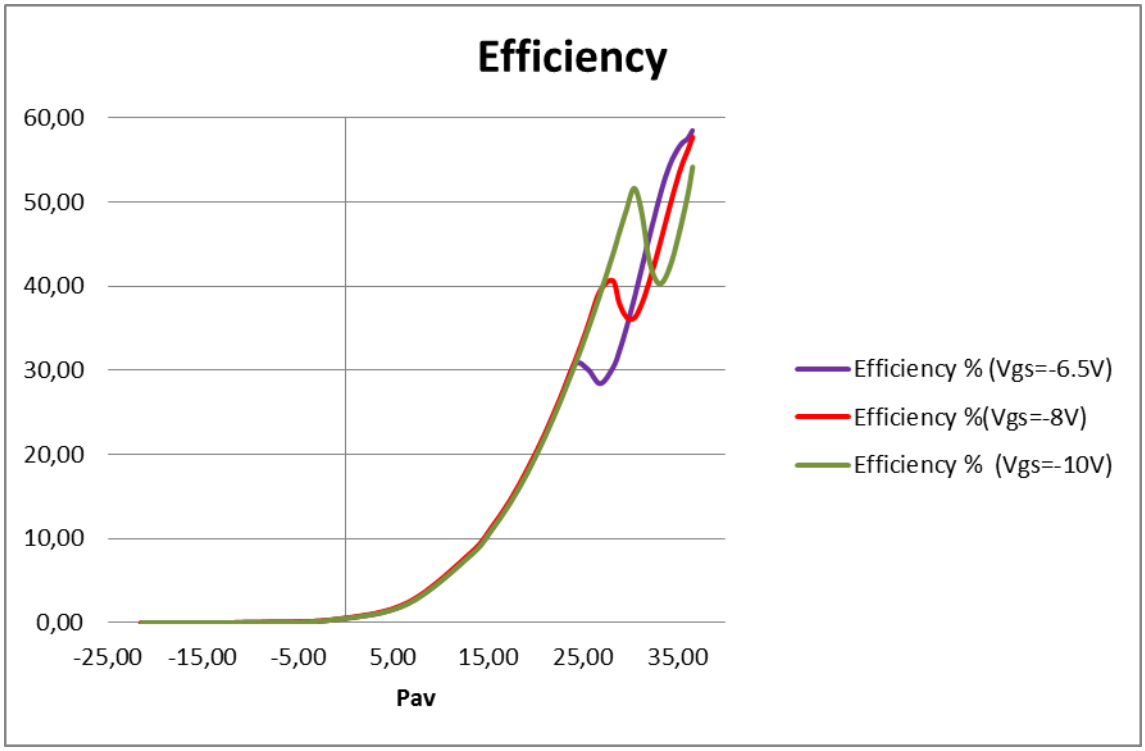

Fig. 59: Efficiency for the different Vgs.

5.3.4 Frequency 3.35 GHz

Setting a bias point of Vds=28V, Vgs_peak -6.5V and -8V, and Id_main 210mA and 50mA.

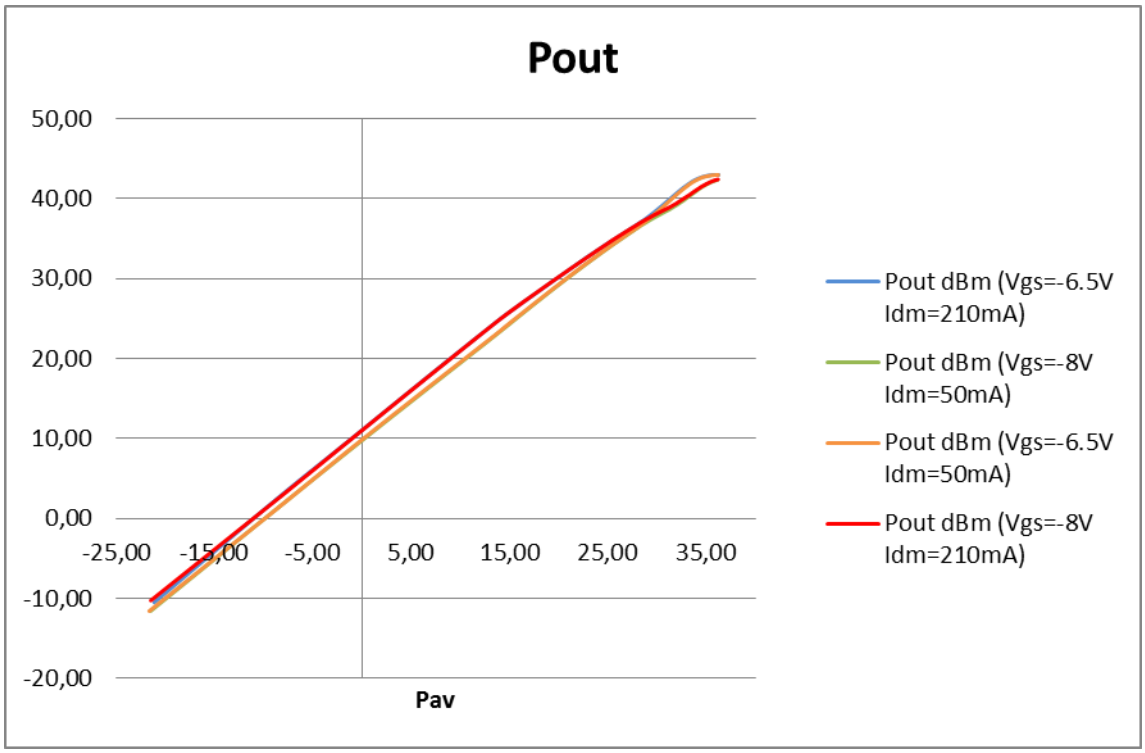

Fig. 60: Pout for the different bias.

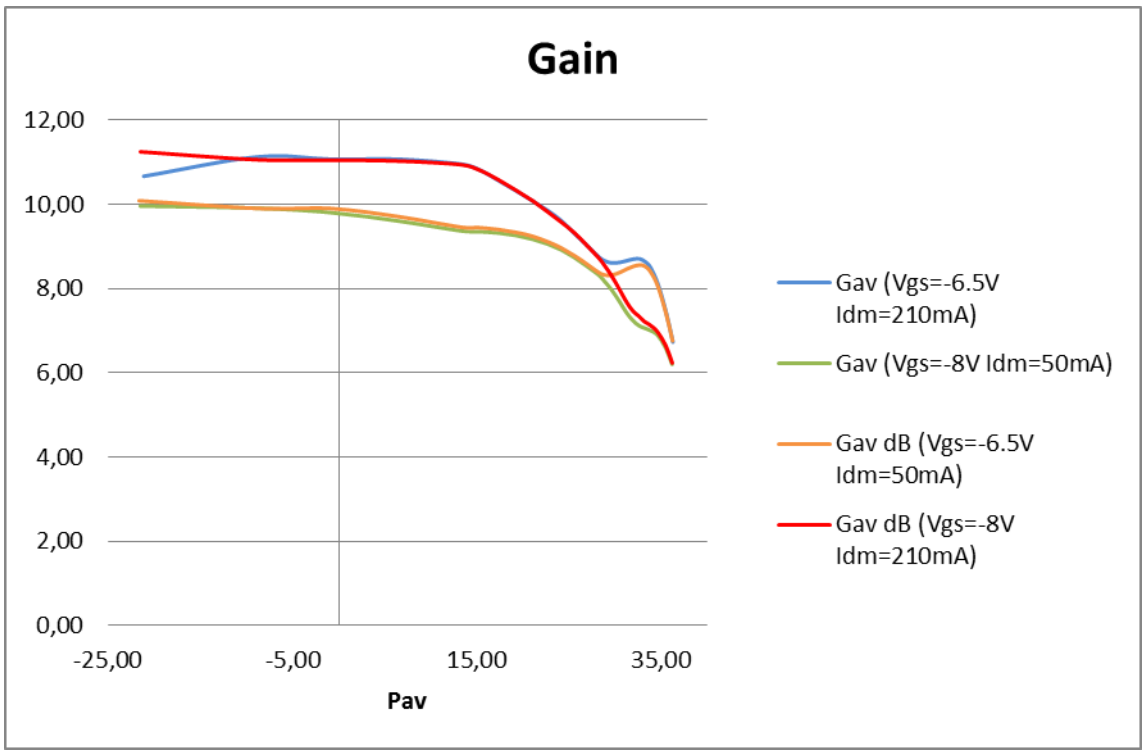

Fig. 61: Gain for the different bias.

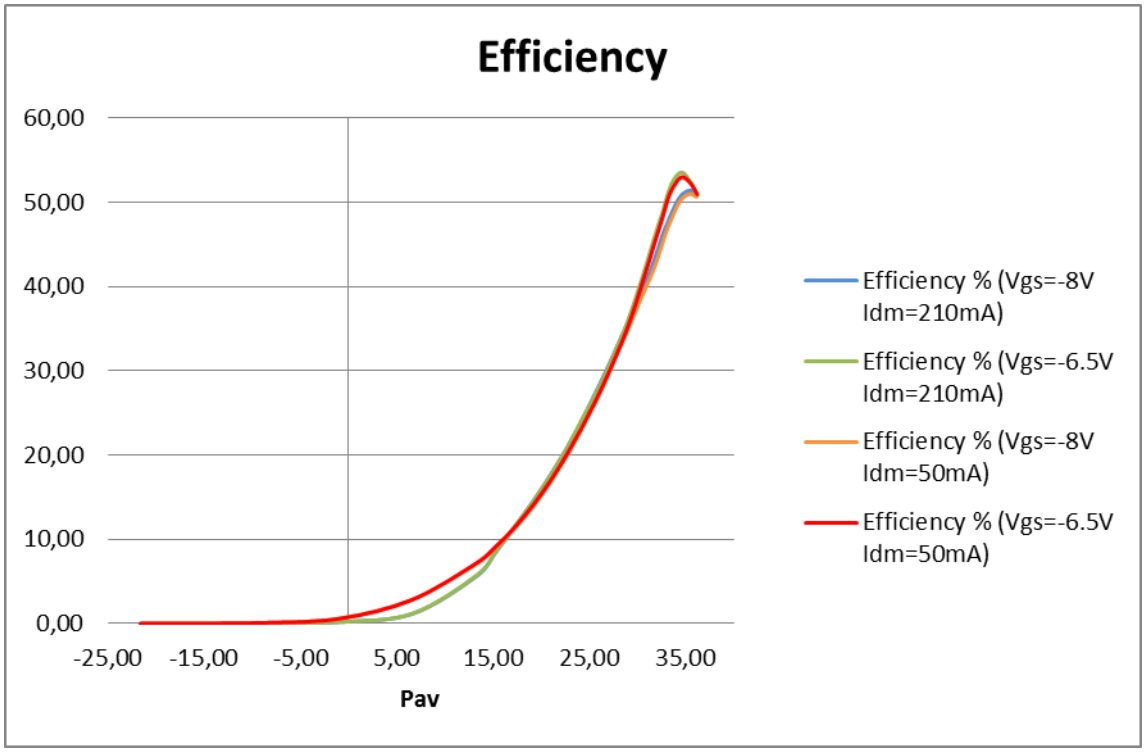

Fig. 62: Efficiency for the different bias.

6. Conclusions

The design in ADS shows that a more linear phase and gain is possible without sacrificing efficiency using bias tuning.

The final microstrip realization has shown a frequency shift to 3.35 GHz. The best performance is obtained biasing with an Id_main=210mA, Vgs_peak=-6.5V and a Vds=28V, with a maximum output power of 43 dBm, a maximum gain of 11 dB and efficiency higher than 40 % at back off.

The bias tuning part cannot be tested because the baseband part of the setup is still uncompleted.

7. References

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[2] Y. Yang, J. Cha, B. Shin, and B. Kim," A Microwave Doherty Amplifier Employing Envelope Tracking Technique for High Efficiency and linearity", IEE microwave and wireless components letters, vol. 13, no. 9, September 2003.

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[5] S. C. Cripps, “RF Power Amplifiers for Wireless Communications.” Artech House Microwave Library.

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