Over 40W, X-Band GaN on SiC MMIC Amplifier

Charles A. Mjema[#], Benoît Haentjens[#], Erwan Fourn[*], M'Hamed Drissi[*],
Laura Diego Arroyo[#], Amparo Herrera Guarardo[^]
[#]VECTRAWAVE, 4 rue Ampère, 22300 Lannion, France
[*]Univ Rennes, INSA Rennes, IETR, UMR CNRS 6164, F-35000 Rennes, France
[^]UNICAN, University of Cantabria, 39005 Santander, Cantabria, Spain
{charles.mjema, benoit.haentjens, laura.diego}@vectrawave.com, {erwan.fourn, mhamed.drissi}@insa-rennes.fr

***Abstract* — In this paper we present the study and obtained results of a MMIC High Power Amplifier operating in X-band. The device is designed using 250nm GaN HEMT on SiC process. The targeted specifications include pulsed operation from 8 to 10.5GHz. In pulsed mode and 28V of drain voltage, an output power more than 40W with (37-40)% PAE has been achieved throughout the bandwidth, while remarkable 52.4W output power with associated 37% PAE has been recorded at 8.75GHz for a 32V of drain voltage. The HPA stability has been studied by considering the influence of external decoupling components and dedicated testing environment.**

***Keywords* — MMIC, Gallium Nitride (GaN), High Power Amplifiers (HPA), X-band, Radar.**

I. Introduction

Wide-band High Power Amplifiers (HPA) are key components in modern RADAR transceivers and point to point communication systems. Their design requires a trade-off among targeted frequency bandwidth, output power and power added efficiency (PAE). In addition, good reliability and high temperature operation must be considered during the design analysis. Gallium Nitride on Silicon Carbide process can offer a junction temperature higher than 200°C with more than one million hours of median time to failure which is far better compared to Gallium Arsenide [1]. Its ability to deliver high power density in a small area allows low payload transceiver structures and high level of module integration [2]. For that type of high output power devices, it becomes more challenging to design an efficient heat sink while preserving RF performance. This is why thermal management has to be taken into account from die layout design in order to improve heat dissipation in a more compact cooling system. In other cases, particular brazing materials can help to improve heat dissipation from the die backside to the heat sink [3].

In recent years, numerous works on GaN amplifiers at X-band have been reported, which show a promising improvement to obtain the desirable performances in terms of output power and PAE [4]–[10]. However, in a wide microwave frequency band is still a challenge to achieve simultaneously high level of output power and PAE at a low input drive. This work reports measured performance and design methodology of an X-band MMIC amplifier fabricated by using commercial available GaN on SiC technology. In order to reduce amplifier development time, combiners and dividers of each stage were designed separately, then after being integrated into the global architecture they were re-tuned by observing the evolution of output power for each stage. S-probes were inserted in each stage to control the matching condition between optimum source and load impedance obtained from load-pull analysis with their respective input and output transistor's impedance. The complete design is based on a compact three-stages amplifier topology.

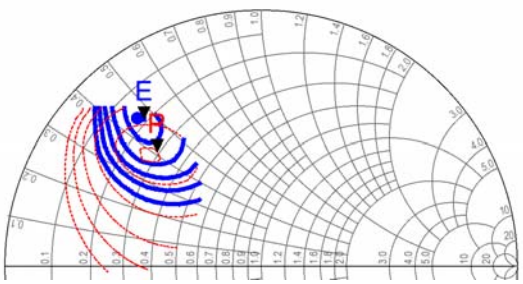
II. HPA Design

A. Transistor selection

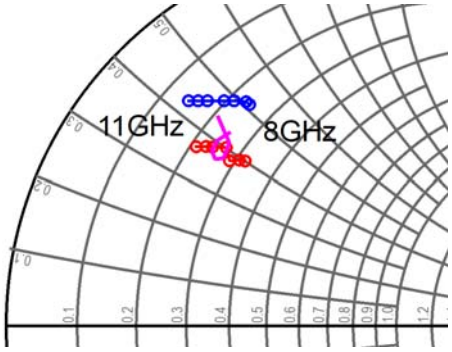
Our goal was to design an HPA that can deliver accross the bandwidth (8-10.5GHz), an output power more than 46.1dBm (40W), with more than 35% of associated PAE, at an input power less than 25dBm. Transistor baredie samples of different size from our foundry were characterized and load pull simulation was also done using the foundry PDK. From above mentioned analysis, a unit power cell of 170μm gate width was selected for the output stage. It gives a maximum output power of 38.3dBm (6.5W) and peak PAE of 55% at 10GHz for an optimum load and source impedance of (14+j21)Ω and (2+4j)Ω respectively as shown in Fig.1a.

Fig. 1b shows fundamental load impedance for output power (red) and PAE (blue), from 8 to 11 GHz simulated from drain and gate plane of the selected output cell for an input power of 27dBm and source impedance of (2+4j)Ω. Load pull study has been conducted for second harmonic and third harmonic frequency range in order to gives us a scope on how we can minimize those harmonics by using appropriate matching elements [11], [12].

In Fig. 2 we show analysis which has been done on a unit cell of output stage at 10GHz for fixed optimum source impedance of (2+4j)Ω. Blue curves from graphs (a) to (c) represent small and large signal performance when the transistor is matched to the load impedance that gives maximun power (14+j21)Ω, while red curves represent small and large signal performance when transistor is matched to its output impedance (7-j28)Ω. We can conclude that the impedance to obtain maximum power is not close to the output impedance of the transistor. Hence, this increases the difficulty to achieve simultaneously high output power, high PAE and large bandwidth with good output return loss.

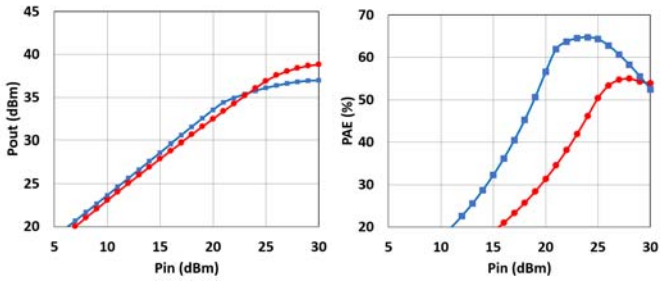


(a)

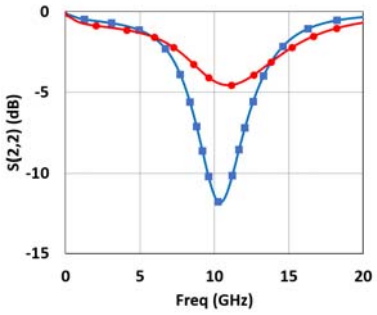


(b)

Fig. 1. Simulated unit output power cell. (a): Load-pull contours at 10GHz, Pout (red dot), PAE (blue bold). (b): Load impedance at fundamental frequencies [8-11GHz], Pout (red), PAE (blue) and load impedance for optimized output combiner (pink) (Pin=27dBm, V_{DS}=28V, I_{dq}=30mA).



(a) Pout vs. Pin **(b)** PAE vs. Pin



(c) S(2,2) vs. freq

Fig. 2. Impedance matching conditions for a unit cell at 10GHz using 2 different loads at constant optimum source impedance (2+j4)Ω. (blue square curves: performance at optimum impedance for maximum power, red dot curves: performance at output impedance for best output return loss, V_{DS}=28V, I_{dq} =30mA).

B. HPA architecture selection

In order to meet our design goals mentioned at the beginning of section II, a three stages amplifier topology has been adopted in order to give high linear gain above 30dB which will helps to use low output power external drivers. Eight transistors with total gate width of 1.36mm each are used for the output stage in order to deliver the desired output power. Each stage was biased in class AB with drain voltage of 28V and total quiescent current of 200mA. The ratio between the third and second stages is around 3:1. Fig. 3 shows the proposed amplifier synoptic. Our MMIC is comprised of two identical structures, north and south, combined together. Each structure includes three stages amplifier chain with independent decoupling circuits.

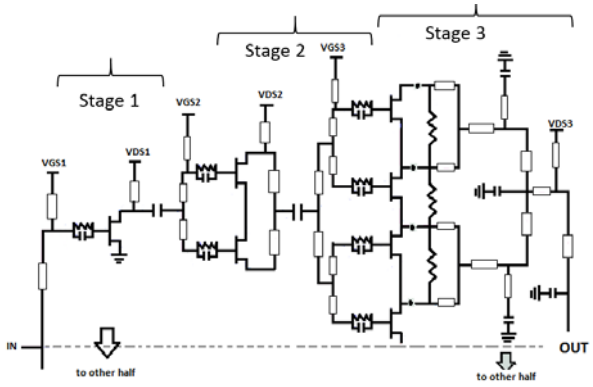


Fig. 3. Proposed amplifier synoptic.

On the die, after decoupling location, we have decided to link gate and drain accesses of stages 1 and 2 together. Such configuration helps users to minimize the number of external decoupling components.

RC circuits in series at each gate were used to minimize the occurrence of low frequency oscillations which linked to low frequency high gain value of FET transistor. The odd-mode oscillation has to be suppressed by inter-drain resistors whose values were chosen after STAN analysis [13]. In order to preserve enough gain at second and third stages, RC circuits were optimized to ensure a trade-off between K factor and the maximum available gain. Their values are set to be high compared to those located at the input driver.

C. Matching Network Strategy

From the selected optimum load impedance, an eight-to-one port combiner is designed. Reactive matching elements required to transform the selected impedance to 50 ohm were directly incorporated to this combiner. Using series of T-mode LC elements in distributed and lumped form, it has been possible to match the impedance and reach the targeted bandwidth ratio of 27%. The insertion loss of designed output combiner was less than 0.7dB throughout the bandwidth. The same technique was used for inter stages combination and division as well as input divider.

When all combiners/dividers and active devices are integrated together, S-probes were used to read the impedance

presented by those matching network against the input/output impedance of transistor. The current probes help to trace the evolution of output power from input stage to the last stage. By doing so, it has been possible to re-optimize the structure and to achieve good trade off between output power and return losses despite the difference observed between transistor's optimum load impedance and output one see (Fig. 2). In Fig. 1b, we show the optimized load impedance of a designed output combiner (pink curve), which is between the load for maximum power (red) and maximum PAE (blue) but closer to the first in order to achieve the targeted output power. The width of drain lines for output stage is directly linked to the peak biasing current reached during high power operations.

D. Stability Analysis

To ensure the stability performance for this amplifier, both external and internal stability analysis were carried out by using existing trust tools such as the Rollet factor (K) and STAN study. Using K-factor tool, only external small-signal stability analysis is performed and simulation results show that the amplifier is unconditionally stable. For internal stability of each active device, a current source has been applied at the drain and gate location of each stage in order to introduce perturbing signal and see its response. Linear and nonlinear pole-zero identification methods were performed to ensure amplifier stability during small-signal and large-signal operations. The variation of gate voltage toward internal oscillation has been also analyzed. Poles and zeros show to be on negative side to all analyzed nodes, which implies that our amplifier was stable toward the odd-mode oscillations [14].

III. RESULTS

Fabricated amplifier was brazed on a copper carrier and appropriate biasing networks were included on both sides of the MMIC. The carrier was mounted to the dedicated heat sink with radiator which helps to improve heat dissipation. Fig. 4 presents under probes measurement setup for the proposed amplifier.

Small-signal measurement was done at 28V of drain voltage with a quiescent current of 200mA. We observe a good agreement between the measured and simulated results. in the full operating bandwidth an input and output matching levels are lower than -10dB and -8dB respectively as shown in Fig. 5.

Large signal measurements were taken for pulse width of 10μs and duty cycle of 10%. Fig. 6 illustrates the results when the device was biased at 28V and 200mA of quiescent current. More than 46.1dBm (40W) of output power with a PAE of (37-40)% from 8GHz to 10.5GHz frequency range have been measured at 24dBm of input power, which is in good correlation with our targeted application. More precisely, for that range of input power, a GaAs amplifier device can be used as an external input driver for this type of GaN/SiC HPA, offering a higher linearity regime to the system chain.

The MMIC was then tested under same pulsed condition with drain voltage of 32V. At this voltage the MMIC delivers an output power of 47.2dBm (52.4W) with a maximum PAE of 37% at 8.75GHz for 24dBm of input power as shown in Fig. 7.

Fig. 4. Fabricated MMIC on Test fixture.

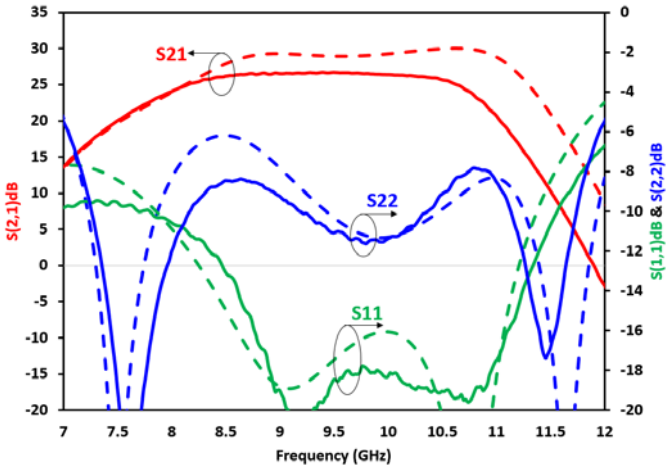


Fig. 5. Under-probes measured (solid line) and simulated (dotted line) linear gain, input and output return losses versus frequency for the proposed amplifier, (V_{DS}=28V, I_{dq}=200mA).

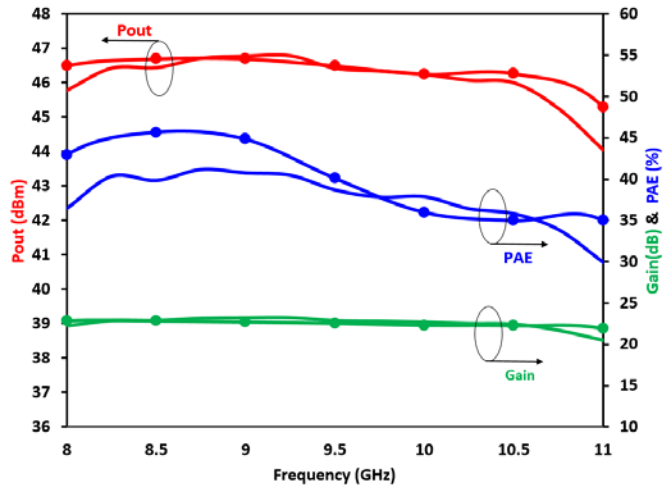


Fig. 6. Measured (solid line) and simulated (solid dotted line) Pout, Gain and PAE versus frequency for the proposed amplifier, (Pulse width= 10μs, Duty cycle= 10%, Pin=24dBm, V_{DS}=28V, I_{dq}=200mA).

Table 1. Comparison with other state-of-the-art 250nm AlGaN/GaN X-band HPA

Ref	Freq (GHz)	Pulse/Duty (µs/%)	Pout (W)	PAE (%)	Power Gain (dB)	VDS (V)
This work	8-10.5	10/10	40-45	37-40	>22	28
This work	8-10.5	10/10	42-52	33-37	>22	32
[4]	8.8-10.8	100/10	30-40	38-44	18	28
[5]	8.5-10.5	10/1	50-58	30	13-15	35
[6]	9-11	20/10	35-45	40-52	16.3	25
[7]	7.8-8.8	CW	22.5	50	19.53	28
[8]	8.8-10.4	50/15	14	38-44	18	26
[9]	8-12	100/10	56-74	40-45	21.5-22.7	28
[10]	9	20/1	58	38	14.6	32

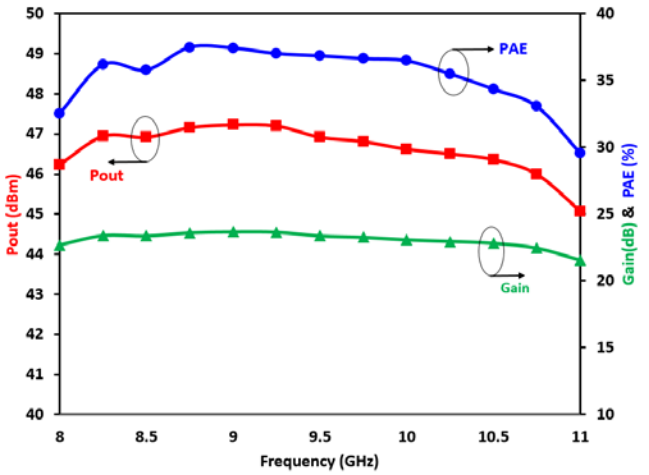


Fig. 7. Measured Pout and PAE versus frequency for the proposed amplifier, (Pulse width= 10μs, Duty cycle= 10%, Pin=24dBm, V_{DS}=32V, I_{dq}=220mA).

IV. Conclusion

In this paper, we have presented the design methodology and the results obtained for a High Power Amplifier MMIC operating from 8 to 10.5GHz. Different analysis and strategies have been presented in order to ensure better performances and best trade-off in terms of output power, PAE and bandwidth. Under pulsed measurements the device demonstrates an output power higher than 46.1dBm (40W) with more than 37% of associated PAE. The performances of this MMIC put its self in a good position compared to other state-of-the arts works previously reported (Table 1).

References

[1] L. B. Walker et al., "Handbook of RF and Microwave Power Amplifiers," *Cambridge University Press*, pp. 305, 424, 530, 2012.

[2] M. van Heijningen, G.C. Visser, J. Würfl, and F.E. van Vliet, "S-Band AlGaN/GaN Power Amplifier MMIC with over 20 Watt Output Power," *2008 Proceedings of the 3rd European Microwave Integrated Circuits Conference*, Oct. 2008.

[3] Raymond S. Pengelly, Simon M. Wood, James W. Milligan, Scott T.Sheppard and William L. Pribble, "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, Jun. 2012.

[4] Dong-Hwan Shin, In-Bok Yom, and Dong-Wook Kim, "X-band GaN MMIC power amplifier for the SSPA of a SAR system," *IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, pp. 93–95, 2017.

[5] C. Costrini, A. Cetronio, P. Romanini, G. Breglio, A. Irace, and M. Riccio, "50W X-band GaN MMIC HPA: Effective Power Capability and Transient Thermal Analysis," *Proceedings of the 5th European Microwave Integrated Circuits Conference*, pp. 408–411, 2010.

[6] S. Piotrowicz, Z. Ouarch, E. Chartier, R. Aubry, G. Callet, D. Floruit, J.C.Jacquet, O. Jardel, E. Morvan , T. Reveyran , N. sarazin, and S.L. Delage, "43W, 52% PAE X-Band AlGaN/GaN HEMTs MMIC Amplifiers," *IEEE MTT-S International Microwave Symposium*, pp. 505–508, 2010.

[7] A.M. Couturier, N. Poitrenaud, V. Serru, R. Dionisio J.J. Fontecave, and M. Camiade, "50% High Efficiency X-Band GaN MMIC Amplifier for Space Applications," *48th European Microwave Week Conference*, pp. 352–355, Sep. 2018.

[8] Davide Resca, Antonio Raffo, Sergio Di Falco, Francesco Scappaviva, Valeria Vadalà, and Giorgio Vannini, "X-Band GaN Power Amplifier for Future Generation SAR Systems," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 4, pp. 266–268, Apr. 2014.

[9] Hong-Qi Tao, Wei Hong, Fellow, IEEE, Bin Zhang, and Xu-Ming Yu, "A Compact 60W X-Band GaN HEMT Power Amplifier MMIC," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 1, January 2017.

[10] S. Piotrowicz et al., "State of the art 58W, 38% PAE X-band AlGaN/GaN HEMTs microstrip MMIC amplifiers," *2008 IEEE Compound Semiconductor Integrated Circuits Symposium*, Oct. 2008, pp. 1–4.

[11] Jangheon Kim, Junghwan Moon, Jungjoon Kim, Slim Boumaiza, and Bumman Kim, "A Novel Design Method of Highly Efficient Saturated Power Amplifier based on Self-Generated Harmonic Currents," *European Microwave Conference (EuMC)*, pp. 1082–1085, 2009.

[12] Ji Lan, Jianyi Zhou, Zhiqiang Yu,and Binqi Yang, "A broadband high efficiency Class-F power amplifier design using GaAs HEMT," *IEEE International Wireless Symposium (IWS)*, pp. 1–4, 2015.

[13] Natanael Ayllon, Juan-Mari Collantes, Aitziber Anakabe, Ibone Lizarraga, Geoffroy Soubercaze-Pun, and Stephane Forestier, "Systematic Approach to the Stabilization of Multitransistor Circuits," *IEEE transactions on microwave theory and techniques*, pp. 2073–2082, Aug. 2011.

[14] A. Anakabe, S. Mons, T. Gasseling, P. Casas, R. Quere, 1.M. Collantes and A. Malet, "Efficient nonlinear stability analysis of microwave circuits using commercially available tools," *European Microwave Week Conference*, pp. 1017–1020, 2002.