1phi SOGI Phase Locked Loop with Secondary Control Path in Grid-Connected Power Converters

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***Abstract*—The performance of digitally controlled grid-connected power converters depends to a large extent on the synchronization strategy. Single-phase phase locked loops (PLL) with a second-order generalized integrator (SOGI) as quadrature signal generation subsystem provide proper grid synchronization in the case of harmonically distorted grid voltage. The SOGI-PLL transient performance can be improved by replacing the PLL by a frequency locked loop (FLL). However, compared with SOGI-PLLs, SOGI-FLLs perform poorly in steady-state. This work proposes to include a secondary control path (SCP) to improve the dynamics of SOGI-PLLs, while maintaining the steady-state performance. Simulation and experimental results are provided to validate the proposal.**

Keywords—Second-order Generalized Integrator, Phase Locked Loop, Synchronization, Digital Control, Bidirectional bridge.

I. INTRODUCTION

Synchronization strategies play a key role in digital controllers used in grid-connected power converters [1]. They track the grid voltage phase θ_g to obtain the appropriate reference signals in current-controlled voltage source power converters (VSCs), improving the controller performance by decoupling the *dq* terms in current controllers [2] and facilitating the implementation of certain high-level functions required by the distribution system operators (DSOs), e.g. anti-islanding protection [3]. Besides, recent researches show that the synchronization strategies are also relevant to achieve a proper power converter operation in weak electrical grids [4], [5].

Among other well stablished synchronization strategies in 1φ grid-connected power converters, those based on second-order generalized integrators (SOGIs) are effective solutions [6]–[11]. 1φ phase locked loops (PLL) based on the Park transform as phase detector require two pure sinusoidal signals, in-phase and in-quadrature, to synchronize with the grid voltage at the fundamental. The grid voltage harmonics are filtered out by the SOGI and it also provides the in-quadrature signal. The gain K_{SOGI} adjusts its harmonic filtering capability and performance. Design recommendations for SOGIs are found in [1] and [12]. When embedded within the 1φ PLL, the resonant frequency of the SOGI is provided by the loop filter, typically a PI controller (Fig. 1.a). In order to speed up the dynamics of the SOGI-PLL, the phase detector, the loop filter and the controlled oscillator can be replaced by a frequency locked loop (FLL), resulting in a SOGI-FLL [12]. The FLL structure is shown in Fig. 1.b. Basically, the FLL consists of a gradient descent strategy to minimize the error signal, *e*, due to the difference between α and the input signal, v_g. The FLL stiffness is adjusted by means of λ_{SOGI}.

In order to improve the dynamics of the SOGI-PLL this paper proposes to include a secondary control path (SCP) within the SOGI-PLL structure to balance the transient and steady-state performances. The SOGI-PLL with SCP is described in section II, section III and IV provide simulation and experimental results evaluating the proposal in

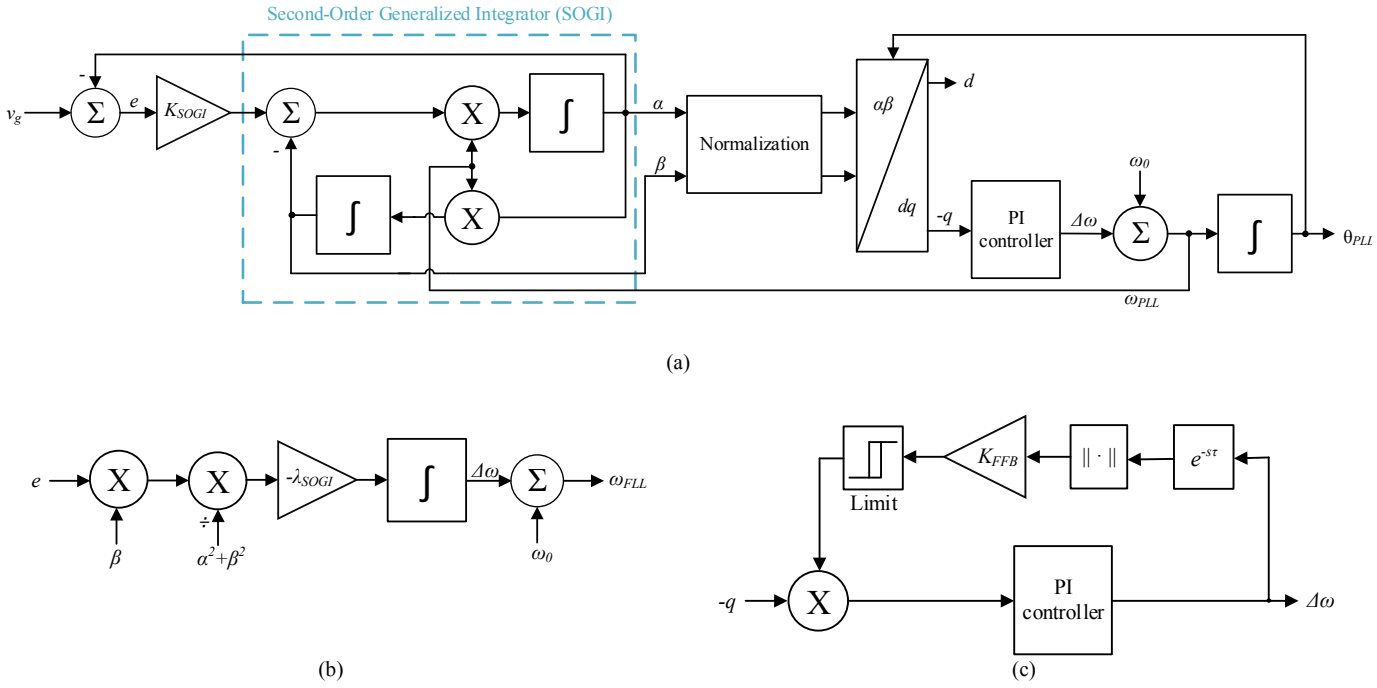

Fig. 1. Main functional blocks of the analyzed 1ϕ synchronization strategies. a) SOGI PLL, b) FLL and c) FFB.

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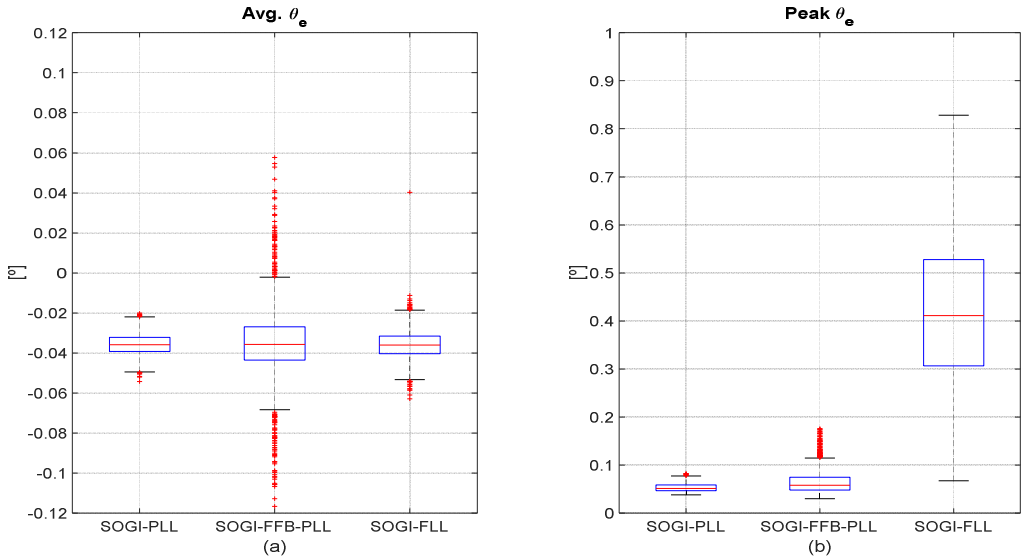


Fig. 2. Steady-State synchronization errors θ_e with SOGI-PLL, SOGI-FFB-PLL and SOGI-FLL. a) average value and b) peak-to-peak amplitude of the ripple. Red line: median, blue square: region delimited by *1st* and *3rd* quartils, black segments: region with *99.3 %* of the PDF, red crosses: outliers .

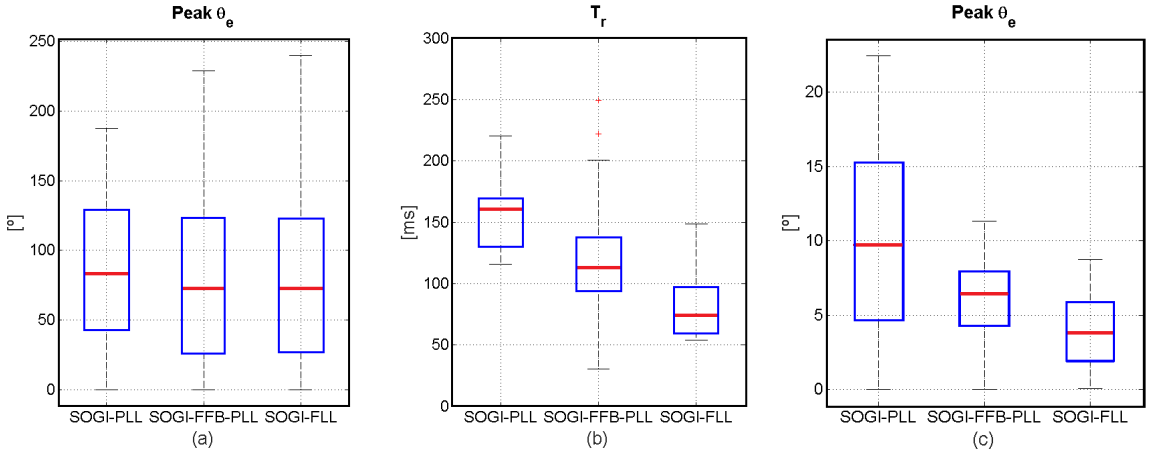


Fig. 3. Responses of SOGI-PLL, SOGI-FFB-PLL and SOGI-FLL to a frequency steps and ramps. a) peak phase error (θ_e) after the frequency step, b) response time (T_r) of the synchronization strategy to the frequency step and c) peak phase error (θ_e) during the frequency ramp. Red line: median, blue square: region delimited by *1st* and *3rd* quartils, black segments: region with *99.3 %* of the PDF, red crosses: outliers.

comparison with SOGI-PLL and SOGI-FLL strategies. Finally, the conclusions are given.

II. SOGI-PLL WITH SCP

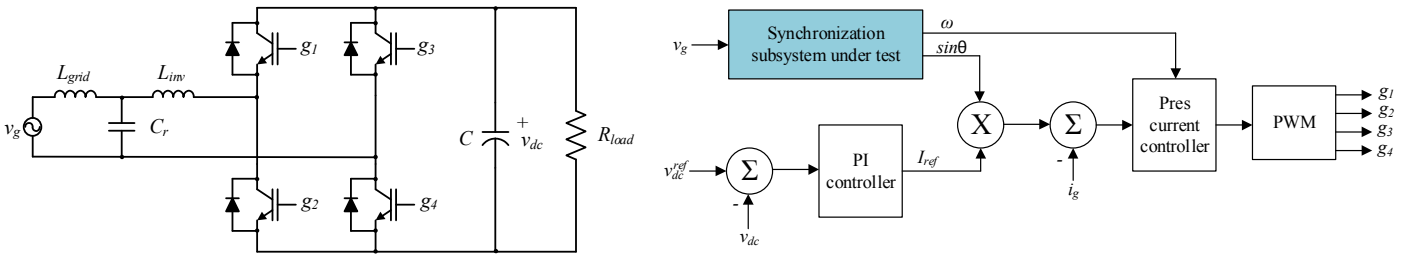
Secondary control paths (SCP) have been used in some PLLs [13]–[16] to improve their dynamics. The approach with SCP is adjusting the loop filter gains to change the dynamics depending on the error signal.

The proposed SOGI-PLL with SCP is obtained by replacing the PI controller in Fig. 1.a by the configuration shown in Fig. 1.c, which consists of a frequency feedback (FFB) loop applied to the PI controller of the PLL. The FFB loop, selected as SCP in [16], adjusts the proportional gain of the PI controller depending on its output, which speeds up the controller in the case of frequency variations. More details about the selection of K_{FFB} are found in [16]. The FFB action shown in Fig. 1.c. is limited to the range *1* to *20* to avoid PLL instability and while achieving a fast enough transient response.

III. SIMULATION RESULTS

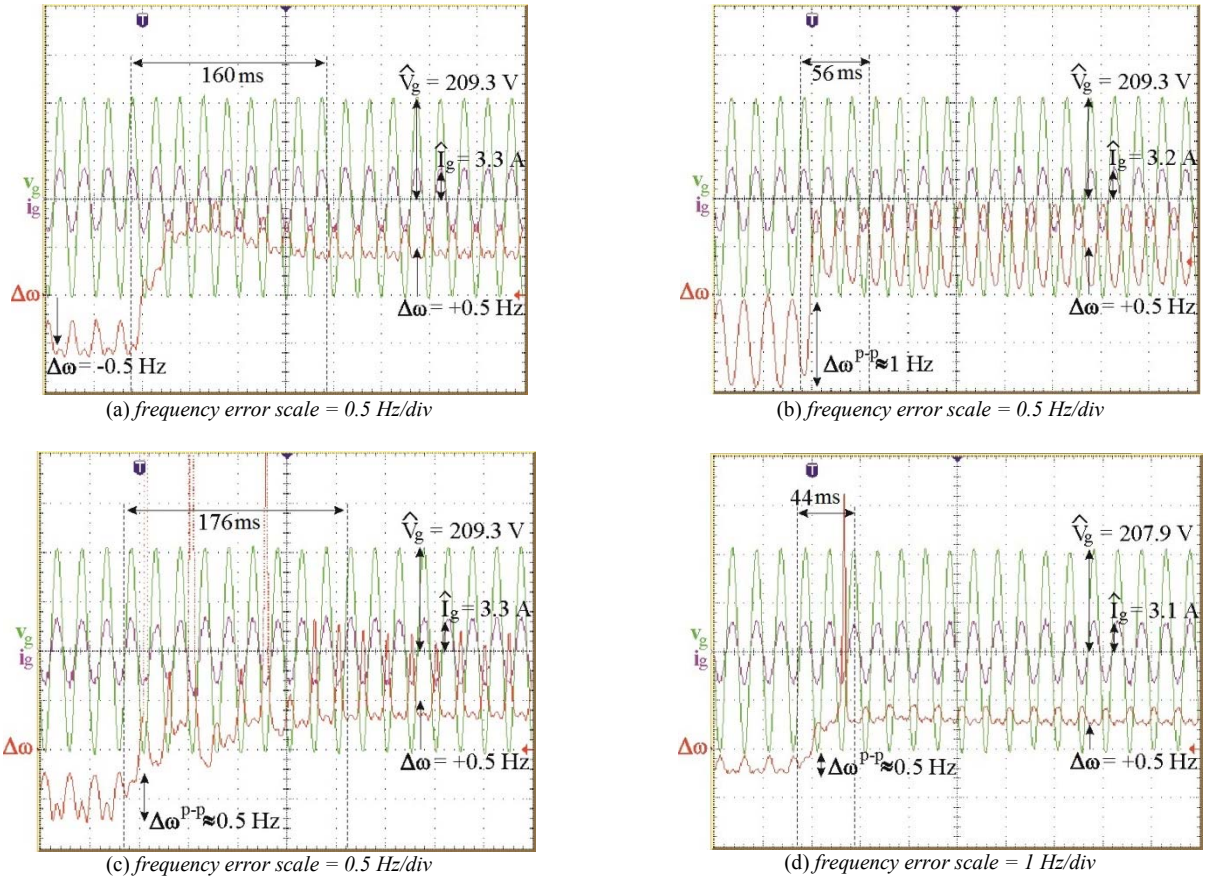
The steady-state and dynamics of the PLL structures shown in Fig. 1 are evaluated with Monte Carlo (MC) analysis [15].

The steady-state test consists of a combination of harmonically distorted grid voltages -odd orders in [*3, 7*], relative phases in [*0,2π*) rad, relative amplitudes in [*0, 0.05*] pu-, accomplishing the allowable levels in IEEE 519-2014 [16], and grid frequencies in [*49, 51*] Hz. The obtained probability density functions (PDFs) for both average and peak-to-peak values of phase error, θ_e, are compared in Figs. 2.a and 2.b respectively. The medians of the average errors are similar (Fig. 2.a), while the proposed SOGI-FFB-PLL results in the widest PDF, with variance σ=*0.093* ° and the highest number of outliers (*120* outliers). However, as it is shown in Fig. 2.b, the peak-to-peak ripple amplitude of the phase error associated to the SOGI-FLL is the worst one with mean μ=*0.4111* ° and σ=*0.173* °. SOGI-PLL and SOGI-FFB-PLL perform almost one order of magnitude better than the SOGI-FLL.



(a) (b)

Fig. 4. (a) Full-Bridge AC-DC converter and (b) digital controller used in the experimental tests.



(a) *frequency error scale = 0.5 Hz/div*

(b) *frequency error scale = 0.5 Hz/div*

(c) *frequency error scale = 0.5 Hz/div*

(d) *frequency error scale = 1 Hz/div*

Fig. 5. Response to a frequency step from *49.5 Hz* to *50.5 Hz*. a) SOGI-PLL, b) SOGI-FLL, and the proposed SOGI-FFB-PLL with c) K_{FFB}=*0.5* and d) K_{FFB}=*0.2*. Green, grid phase voltage, [*100* V/div], purple, line current [*5* A/div], red, frequency error and time scale [*40* ms/div].

The responses to frequency steps are evaluated using diverse initial and final grid frequencies in the *49* to *51* Hz range, therefore resulting in frequency steps of up to ±*2* Hz, applied at diverse grid phase angles. The obtained PDFs for the maximum phase error and the response time are shown in Figs. 3.a and 3.b respectively. The response time of θ_e is measured from the step beginning to the time instant where θ_e reaches a *3 %* of the peak θ_e. Comparing the obtained PDFs for the peak θ_e during the frequency step (Fig. 3.a), the SOGI-PLL reaches the worst results (μ=*83.8* º and σ=*67.3* º) while SOGI-FFB-PLL and SOGI-FLL perform better and achieve similar results (μ=*73.0* º / σ=*74.4* º and μ=*72.8* º / σ=*74.3* º respectively). The measured response times (Fig. 3.b) is the parameter that shows the largest differences among the considered synchronization strategies. The SOGI-PLL is the worst performing, with μ=*160.8* ms and σ=*28.9* ms, the FFB action improves the response times, resulting in μ=*112.9* ms and σ=*32.8* ms. The best response times are achieved with the SOGI-FLL, with μ=*74.7* ms and σ=*27.8* ms. The consistency of all the synchronization strategies to the random tests is similar (similar standard deviation values) and the proposed SOGI-FFB-PLL achieves an intermediate performance.

The synchronization strategies are also evaluated with frequency ramps up to ±*2.5* Hz and a duration less than *200* ms. The initial and final grid frequencies are selected within the *49* to *51* Hz range. Fig. 3.c shows the PDFs for the maximum phase error during the frequency ramp. In comparison with the peak θ_e due to the frequency step, the measured errors are lower. The SOGI-FLL results in the best

performance in the case of grid frequency ramps, with $\mu=3.81$ º and $\sigma=2.96$ º. Again, the worst performance corresponds to the SOGI-PLL, with $\mu=9.76$ º and $\sigma=7.88$ º, while the proposed SOGI-FFB-PLL reaches $\mu=6.40$ º and $\sigma=2.78$ º.

IV. Experimental Results

The effect of SOGI-PLL, SOGI-FFB-PLL and SOGI-FLL synchronization strategies within a digital controller has been evaluated experimentally, with a Full-Bridge AC-DC bidirectional converter (Fig. 4.a). The power converter, working as an active rectifier, supplies *320* W to a DC load. The output voltage is filtered out with a *500* uF capacitor. The AC current is filtered out by a LCL filter (L_{grid}= *1* mH, L_{inv}=*2* mH, C_f=*7* uF). A power generator emulates the grid source *150* V, *50* Hz. The active rectifier is controlled by means of a digital control loop, being executed by a DS1103 control board from dSpace, and corresponds to the block diagram in Fig. 4.b including both an inner AC-current and an outer DC-voltage control loops. The switching frequency is $f_{sw}=6.4$ kHz. Unipolar pulse width modulation is used. The inner AC-current loop is built with a proportional-resonant controller ($K_p=6$ and $K_r=10^3$) plus a harmonic compensator for the 3^{rd}, 5^{th} and 7^{th} harmonics ($K_3=K_5=K_7=200$). The resonance frequencies of the current controller are provided by the synchronization schemes. The outer DC-voltage loop is a PI controller ($K_p= 2{,}4 \cdot 10^{-2}$ and $K_i= 1.1 \cdot 10^{-2}$) . The experiment consists on applying frequency steps from 49.5 Hz to *50.5* Hz to the pure sinusoidal grid voltage, v_g. Results are shown in Fig. 5. SOGI-PLL (Fig. 5.a) and SOGI-FLL (Fig. 5.b) perform as expected. The proposed SOGI-FFB-PLL, with a small $K_{FFB}=0.2$ (Fig. 5.c), results in a good trade-off between the steady-state and transient responses. By increasing K_{FFB} to *0.5* (Fig. 5.d), the FFB saturates and the PI controller oscillates trying to compensate for the frequency deviation, increasing again the response time.

V. Conclusions

A SOGI-FFB-PLL has been proposed for synchronization of the current reference in single-phase grid connected converters. Simulation and experimental results have compared the performance of the proposed circuit against the SOGI-PLL and SOGI-FLL options, stand-alone and embedded within a digital controller of a Full-Bridge AC-DC grid connected converter. The proposed SOGI-FFB-PLL provides a steady-state performance similar to the SOGI-PLL with a faster transient response, similar to the SOGI-FLL.

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