Third Harmonic Compensation in Bridgeless Current Sensorless PFC

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***Abstract*—Single-phase Bridgeless power factor correction converters (PFCs) improve the conversion efficiency in comparison with the conventional PFCs, where a diode bridge plus a DC/DC boost converter are used, due to the absence of the input rectifier, but current sensing complexity increases. Its efficiency can be further increased, and its cost reduced by avoiding the input current sensor. This paper proposes a control strategy applicable to Bridgeless PFCs, implemented in a digital device (*Field Programmable Gate Array*, FPGA), where the grid current is not sensed. To compensate for the effect of the non-ideal operation of the converter, which result in current control errors, a third harmonic dependent function is introduced. The converter model is presented. Simulation and experimental results are used to assess the performance of the proposed method.**

I. Introduction

Most home appliances (TV, desktop PC, battery chargers and so on) and low power industrial loads e.g. LED drivers and arc welding are DC loads. The need to comply with standards like IEC 61000-3-2 require the use of PFC stages in off-line power supplies [1]. To do so, several solutions are available, from the traditional bridge-diodes plus a DC/DC converter to more complex ones like full-bridge AC/DC converter. However, taking into account the adoption of bridgeless solutions is becoming important to meet the industry requirements.

However, one of the main problems of this topology is its common-mode noise occurring. To fix this issue, several solutions were proposed [2], [3]. Along this work, the one in Fig. 1 will be used due to its low complexity and good performance. Compare with the totem-pole counterpart, the main advantage is that the MOSFETs share the common ground, so there is no need to add a second power supply for the drive signal of the upper MOSFET driving circuit nor to use solutions based on bootstrap capacitors. Instead, two extra diodes are added to reduce the common-mode noise [4].

One of the drawbacks associated to the bridgeless topologies is the difficulty to measure the AC side variables (voltage and current), because they become differential measurements [4]. Therefore, the overall cost and complexity increases, not only because of the necessity of a differential/isolated current and voltage sensor but also due to the acquisition stage [5], [6], [7]. Comparatively, this issue is bigger with current than with voltage measurements [4]. Therefore, a current sensorless algorithm is proposed in this paper. Eventhough the proposed algorithm is valid for all of the single-phase AC/DC active rectifiers, the analysis and validation will be carried out along with bridgeless topology.

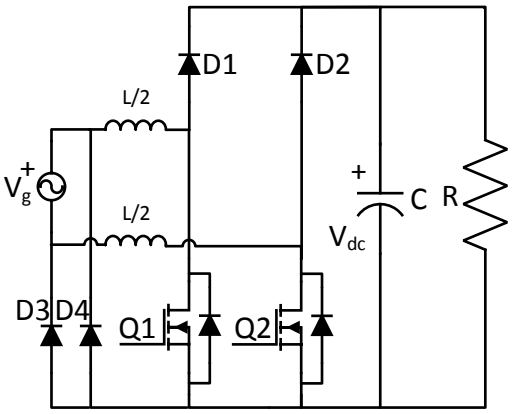

Fig. 1: Bridgeless topology used along this work

II. Analysis

Using a quasi steady-state analysis, the AC/DC boost rectifier is modeled around the grid frequency ω as shown in Fig. 2, where v_g is the grid voltage, i_g the grid current, L is the boost inductor, r_L the parasitic resistance of the boost inductor, v_L is the voltage across the input inductor and v_{conv} is the voltage at the input of the power converter.

The goal of a PFC solution is to obtain a grid current in phase with the grid voltage (low harmonic distortion is also a goal but it has no effect on the initial assumptions) and the right amplitude according to the power rate. Therefore, the phasor diagram shown in Fig. 3 is obtained.

$$v_g(t) = V_g \cdot \sin(\omega t) \tag{1}$$

$$i_g(t) = I_g \cdot \sin(\omega t) \tag{2}$$

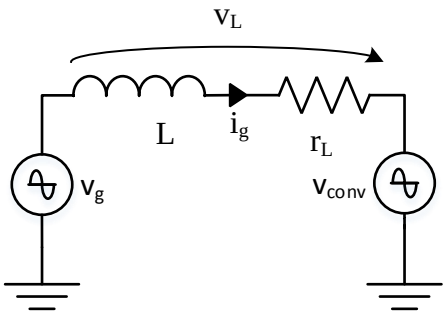

Fig. 2: Model of the analyzed topology working as PFC assuming CCM and no DC-link voltage ripple

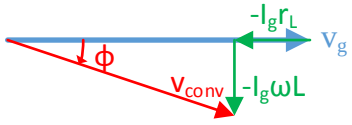

Fig. 3: Phasors diagram

The voltage v_{conv} is the product of the control signal, $u_m(t)$, divided by PWM sawtooth amplitude, V_R, and multiplied by the DC-link voltage, V_{DC}.

$$v_{conv}(t) = \frac{u_m(t)}{V_R} \cdot V_{DC} \tag{3}$$

In PFC application, to obtain a high power factor, v_g and i_g must be in phase, as shown in Fig. 3. Therefore, v_{conv} will result as expressed in (4), where ϕ is the angle between v_g and v_{conv}.

$$v_{conv}(t) = \frac{U_m}{V_R} \cdot \sin(\omega t + \phi) \cdot V_{DC} \tag{4}$$

The amplitude of the DC-link ripple depends basically on the capacitance value used in the DC-link and the power rate [8], as shown in (5). Since the nominal power converted and the grid frequency are given parameters, only the capacitance value is modifiable.

$$v_{DC}(t) = \sqrt{V_{DC}^2 - \frac{P_{load}}{\omega C} sin(2\omega t)} \tag{5}$$

If a large capacitance value is chosen, it clearly smooths out the DC-link ripple. Such solution could be mandatory in some applications where the PFC capacitor should meet the hold-up time (20 ms), or low output voltage ripple specification at the expense of increasing the cost. However, if that is not the case, a big capacitor is not justified, the DC-link ripple becomes not negligible and its effect must be included into (4).

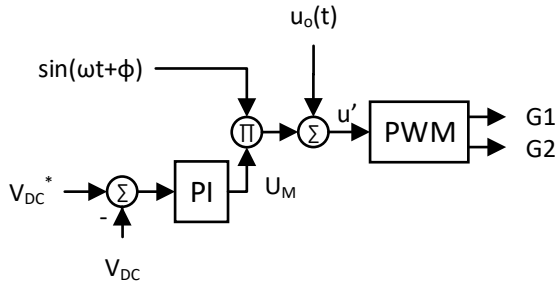

Fig. 4: Simplified diagram block of the proposed control scheme

III. Proposed Solution

The expression for the DC-link shown in (5) is approximated using only the DC component and a twice the line frequency component (6), where $\frac{I_{DC}}{2\omega C}$ is the amplitude of the DC-link voltage ripple, V_{pk}, I_{DC} is the DC output current and C is the DC-link capacitance value.

$$v_{DC}(t) = V_{DC} - \frac{I_{DC}}{2\omega C} sin(2\omega t) \tag{6}$$

Therefore, to obtain a sinusoidal current in phase with the grid voltage, the DC-link voltage ripple must be compensated. Introducing a predistortion, $u_0(t)$, the new control signal will be: $u'_m(t) = U_m sin(\omega t + \phi) + u_o(t)$. A simplified diagram block of the control scheme proposed is shown in Fig. 4. The main blocks are: outer voltage loop, non-compensated control signal $u_m(t)$ and the compensation signal $u_0(t)$.

Therefore, v'_{conv} becomes:

$$v'_{conv}(t) = (U_m \sin(\omega t + \phi) + u_o(t)) \cdot \frac{v_{DC}(t)}{V_R} \tag{7}$$

Replacing (6) into (7) and extending, the expression (8) is obtained.

$$\begin{aligned} v'_{conv}(t) \quad = \quad & \frac{U_m \sin(\omega t + \phi) V_{DC}}{V_R} \quad - \\ - \quad & \frac{U_m I_{DC}}{2\omega C V_R} \sin(2\omega t) \sin(\omega t + \phi) \quad + \\ + \quad & u_0(t) \frac{V_{DC} - \frac{I_{DC}}{2\omega C} \sin(2\omega t)}{V_R} \end{aligned} \tag{8}$$

As explained in the previous section, the condition for a PFC application is $v'_{conv} = v_{conv}$ and its expression is given in (4). Therefore, (8) becomes (9).

$$\begin{aligned} & \frac{U_m I_{DC}}{2\omega C V_R} \sin(2\omega t) \sin(\omega t + \phi) = \\ & u_0(t) \frac{V_{DC} - \frac{I_{DC}}{2\omega C} \sin(2\omega t)}{V_R} \end{aligned} \tag{9}$$

Solving for $u_o(t)$, an expression for the predistortion parameter is obtained in (10).

$$u_o(t) = \frac{\frac{U_m I_{DC}}{2V_R \omega C}\sin(\omega t + \phi) sin(2\omega t)}{V_{DC} - \frac{I_{DC}}{2\omega C}\sin(2\omega t)} \tag{10}$$

However, (10) for $u_o(t)$ contains a division, which make it complex to implement in a digital device. This fact is even more important for a device such as a FPGA that do not support floating point arithmetic or, if so, consumes a large amount of resources. Observing the denominator in (10), it can be approximated by a constant value, assuming that the DC-link voltage ripple is much smaller than its average value (e.g. 5 %). Doing so, (10) becomes (11),

$$u_o(t) = \frac{U_m I_{DC}}{2V_R \omega C V_{DC}}\sin(\omega t + \phi) sin(2\omega t) \tag{11}$$

Splitting it into the fundamental frequency and the third harmonic, (12) is obtained.

$$u_o(t) = \frac{U_m I_{DC}}{4V_R \omega C V_{DC}}\left(\cos(\omega t - \phi) - \cos(3\omega t + \phi)\right) \tag{12}$$

In (11), there are still parameters that are not directly obtained. Starting from the known ones, U_m is the power command given by the outer loop which includes the average DC-link voltage controller. V_{DC} is the average DC voltage, which is constant in steady-state operation and given for a certain application. C is the capacitance value, also known given the application.

The remaining terms need to be incorporated by the circuit. The grid frequency, ω, which is not constant but bounded. Its value is given by a digital PLL (*Phase-Locked Loop*). The terms $\sin(\omega t)$ and $\sin(2\omega t)$ are both obtained using the synchronization and ω of the PLL.

On the other hand, I_{DC} and ϕ need to be calculated or estimated separately. Firstly, ϕ can be obtained from Fig. 3 as follows:

$$\phi = \arctan\left(\frac{L\omega I_g}{V_g - I_g \cdot r_L}\right) \tag{13}$$

Simplifications can be adopted. Firstly, the denominator can be simplified because $I_g \cdot r_L << V_g$ and therefore (13) becomes (14).

$$\phi \simeq \arctan\left(\frac{L\omega I_g}{V_g}\right) \tag{14}$$

Moreover, in the same way, $L\omega I_g << V_g$, which transforms (14) into (15).

$$\phi \simeq \frac{L\omega I_g}{V_g} = \frac{L\omega I_{g,rms}}{V_{g,rms}} \tag{15}$$

Since the grid current is not being sensed, $I_{g,rms}$ must be estimated; it can be calculated from the DC-link voltage

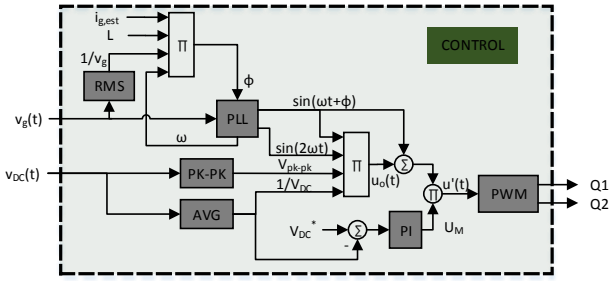

Fig. 5: Block diagram of the implemented control

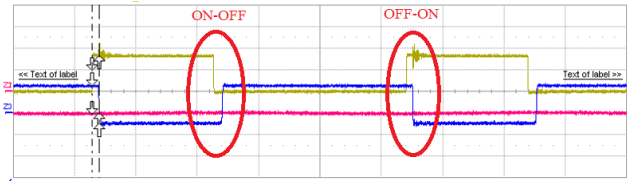

Fig. 6: Switching signals: *blue*, V_{DS} voltage in the power MOSFET, *yelow*, FGPA gate signal

information. Assuming 100% efficiency in the power converter, $V_{g,rms} \cdot I_{g,rms} = V_{DC} \cdot I_{DC}$. Moreover, the DC output current can be obtained from (6) resulting (16).

$$I_{DC} = V_{pk} \cdot 2\omega C \tag{16}$$

Therefore, the expression for the estimated RMS grid current $I_{g,rms_{est}}$ is shown in (17) and the expression for ϕ is obtained in (18).

$$I_{g,rms_{est}} = \frac{V_{DC} \cdot V_{pk-pk} \cdot \omega \cdot C}{V_{g,rms}} \tag{17}$$

$$\phi = \frac{LC\omega^2 V_{DC} V_{pk-pk}}{V_{g,rms}^2} \tag{18}$$

Figure 5 shows the block diagram of the implemented control.

IV. Effect of the Switching Delays

The switching delay is defined as the time between the ON-OFF or OFF-ON transition on the FPGA signal and the same transition in the power MOSFETs (V_{DS} or *drain* to *source* voltage), as seen in Fig. 6. This delay is different in a ON-OFF transition than on the OFF-ON, resulting in a different duty-cycle applied to the converter. As a consequence, the current is distorted.

Furthermore, these delays are not constant and depend on different parameters like the V_{DS} voltage, the I_D or (*drain* to *source* current), etc, as explained in [9]. The delays have been firstly measured along one grid semi-period, obtaining the results shown in Fig. 7, where ΔD represents the difference between the theoretical duty-cycle (FPGA signal) and the experimentally measured in the power MOSFET. Secondly, the same analysis has been carried versus the grid current

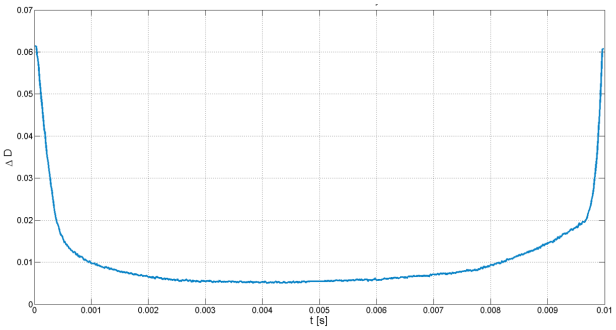

Fig. 7: Effect of the delays on the duty cycle along the grid semi-period

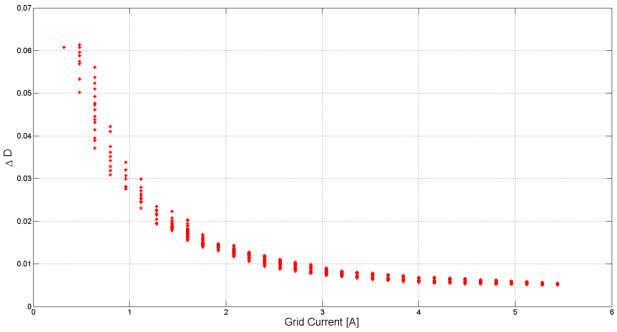

Fig. 8: Effect of the delays on the duty cycle when the grid current change

level, which is the switching current, since it also affects the switching delays, obtaining the results shown in Fig. 8.

It can be observed that the delays highly depends on the switched current and, what is more important, it is a non-linear dependecy, which complicates the compensation algorithm unless a sensor/detector is used. To overcome this issue, the compensation algorithm has been divided into two: firstly, around the zero-crossing point (A, in Fig. 9), the duty cycle was limited to 90%, assuring that the MOSFET is not in the ON-state for several duty-cycles provoking high-current spikes around this point. Secondly, a constant value is substracted from the theoretical duty-cycle to compensate the effect shown in B (Fig. 9 and manually adjusted since it depends on the load.

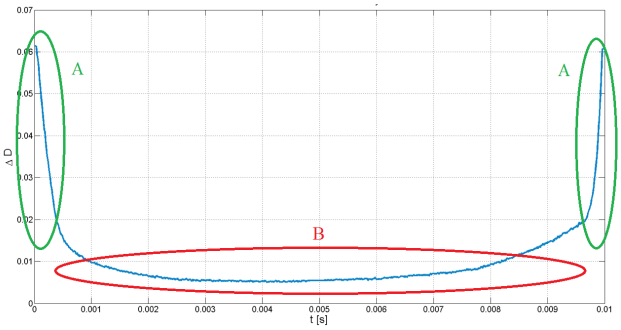

Fig. 9: Compensation of the delays experimentally measured

v_g	115 V_{rms}
V_{DC}	250 V
f	50 Hz
L	1.1 mH
C	550 μF
f_{sw}	98.5 kHz
R	200 Ω

TABLE I: Simulation and experimental conditions

V. Simulation and Experimental Results

In order to assess the proposed algorithm, firstly, a simulation was carried out under the conditions shown in Table I. PLECS has been used to simulate the power converter section and MATLAB/Simulink to simulate the control part (Fig. 5). It is worth mentioning that the delays are only compensated along the experimental section; the switching transitions are ideal (no delays) throughout the simulation section.

Since the results highly depend on the PLL algorithm, the beginning of the simulation was omitted because the PLL is not synchronized. Once the PLL is locked, the algorithm is fully operational. To validate the current control by the proposed circuit, the responses under grid voltage and load steps are demostrated. Firstly, Fig. 10 shows the obtained results before and after a voltage step from 115 V_{rms} to 125 V_{rms}.The conditions before the step are shown in Table I. At $t = 1.2$ s, a grid voltage step is applied. It can be seen that the grid current is highly distorted because the PLL loose synchronization. However, once the PLL is back locked, the obtained grid current is sinusoidal and in phase with the grid voltage.

Secondly, a load step is shown in Fig. 11. The conditions before the load step are shown in Table I. At $t = 1.2$ s, a load step from $R = 200$ Ω to $R = 167$ Ω is applied. In this case, since the PLL is not affected by the load step, the algorithm adapts to the new conditions instantaneously without any transition that distorts the grid current.

Finally, to experimentally evaluate the proposed solution, a laboratory setup was built (Fig. 12). It consist of the following elements:

- For easy of implementation, a Full-Bridge topology based on Vincotech Power MOSFET Modules V23990-P722-F64-PM, where the 2 upper MOSFETs are disabled, has been used.
- Power MOSFET drivers based on Scale cores (2SC0650P).
- Sensing Board. Used to measure the DC-link and the grid voltages needed to implement the proposed algorithm.
- Digilent Nexys 4 board (based on Xilinx 7 XC7A100T-1CSG324C) used to implement the digital control

The prototype is fed by a programmable Pacific AC source (AC Power Source 345-AMX) which allows the voltage steps to be applied.

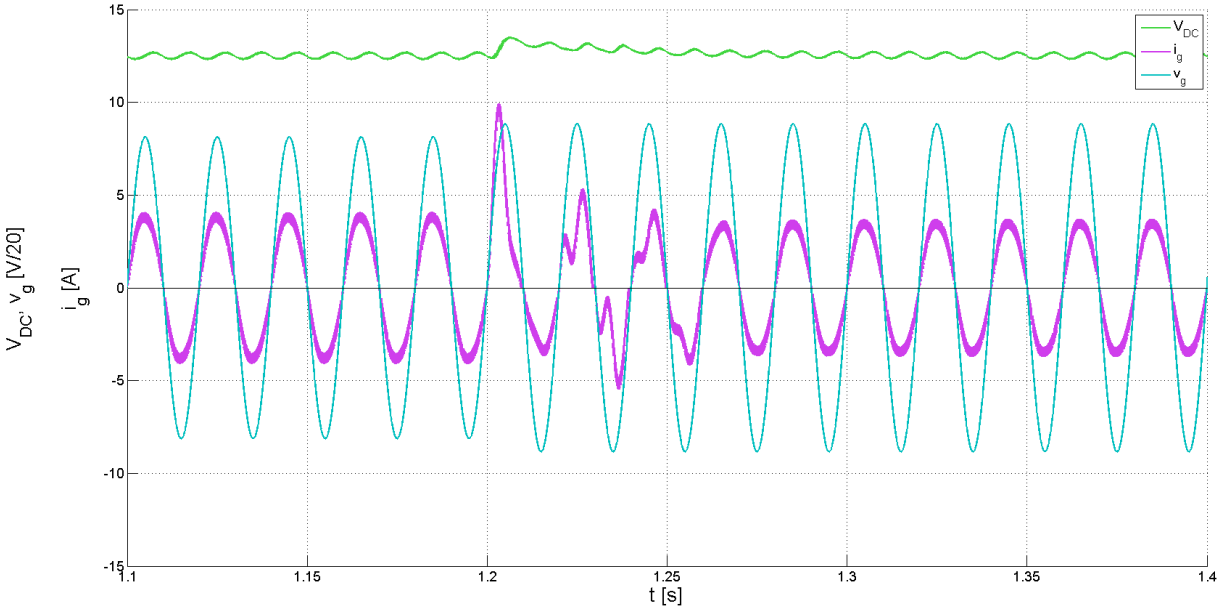

Fig. 10: Simulations results: DC-link voltage, line current and line voltage before and after a grid voltage step from 115 V_{rms} to 125 V_{rms}

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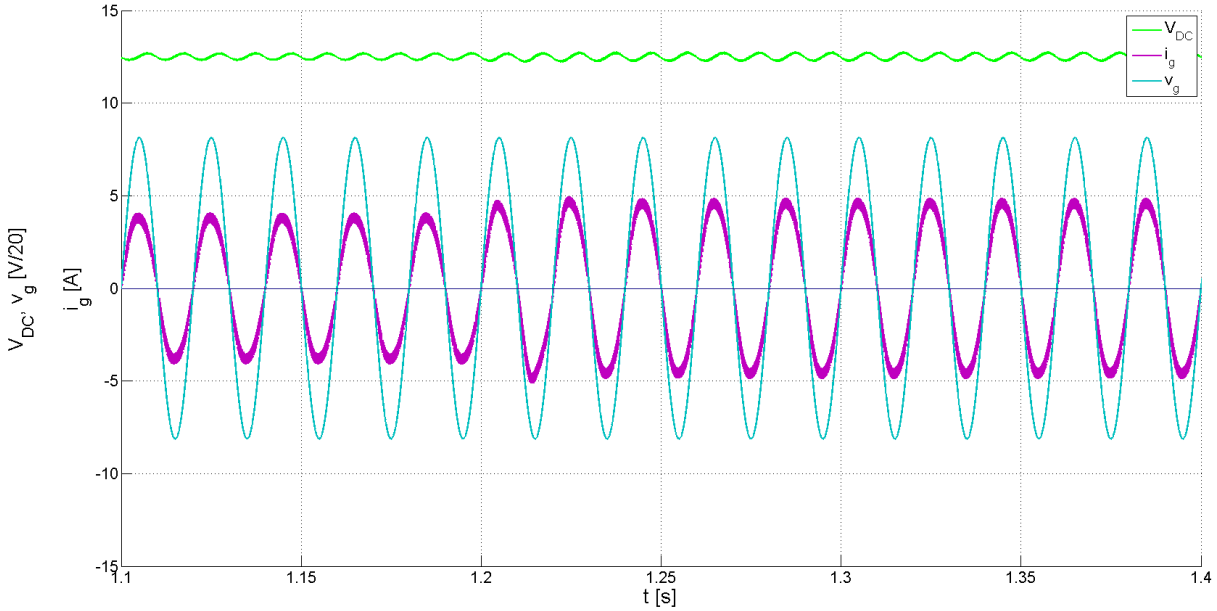

Fig. 11: Simulations results: DC-link voltage, line current and line voltage before and after a load step from $R = 200\ \Omega$ to $R = 167\ \Omega$

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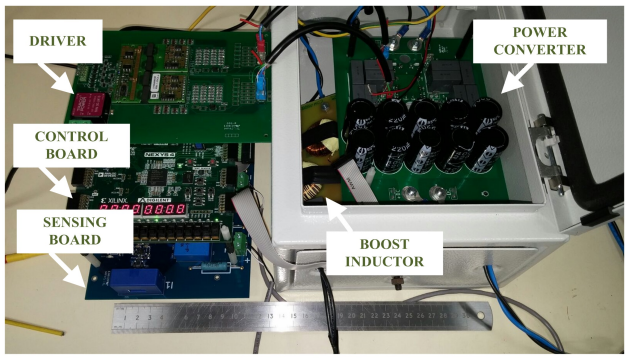

Fig. 12: Experimental setup

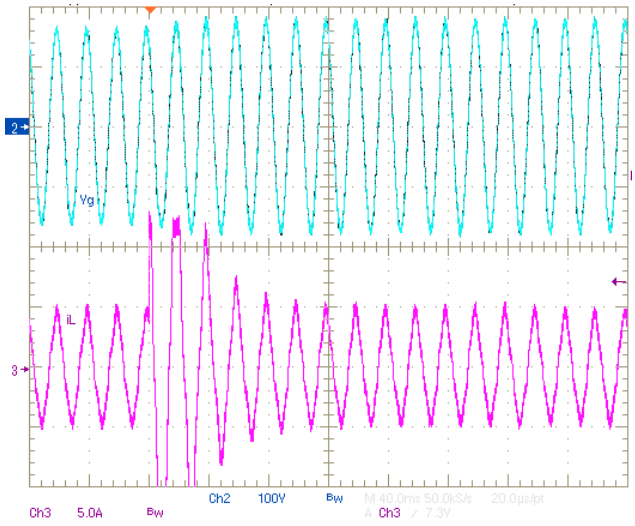

Fig. 13: Experimental results obtained before and after a grid voltage step: v_g, magenta, [50V/div], i_g, blue, [5A/div]

After the compensation was applied, the results obtained are shown below. Firstly, as in the simulation stage, a grid voltage step was applied, obtaining the results shown in Fig. 13. Before the step, the grid voltage is $115V_{rms}$, while after the step is $125V_{rms}$. It can be seen that because the PLL loose the synchronization, there is a transient resulting in a grid current distortion until the PLL recovers the synchronization, as predicted by the simulation. Secondly, a load step is applied in the same way as before, following the conditions used in the simulation: before the step, $R = 200\Omega$, which means that the output power will be appoximately $313W$ and the input power measured is $345W$, meaning that the efficiency is around 90.7%. After the step, $R = 167\Omega$ so the output power will be approximately $374W$ and the measured input power is $413\ W$ resulting in 90.6% of efficiency. The results are shown in Fig. 14. Finally, in steady state, the results obtained are shown in Fig. 15. The parameters obtained in steady state are: $THD_i = 6.3\%$ and $PF = 0.996$. Therefore, the grid current obtained fullfil the standard IEC 61000-3-2, Class C.

VI. Conclusion

A digital algorithm based on a third harmonic injection properly synchronized with a PLL has proven to be an efficient

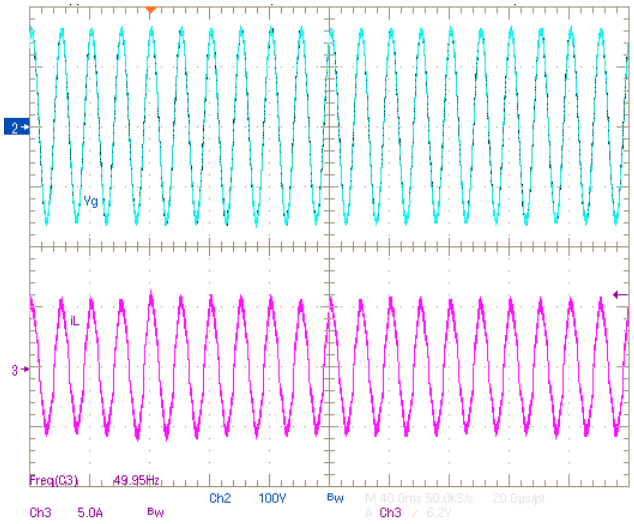

Fig. 14: Experimental results obtained before and after a load step: v_g, magenta, [50V/div], i_g, blue, [5A/div]

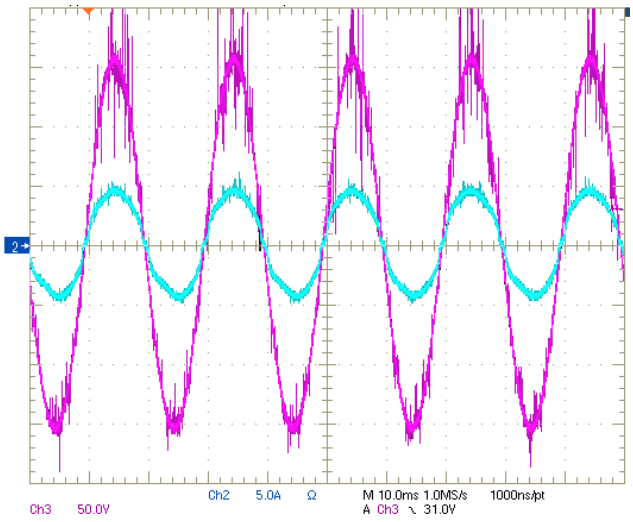

Fig. 15: Experimental results obtained in steady state: v_g, magenta, [50V/div], i_g, blue, [5A/div]

technique to compensate for the difference of the control signal that results from the current estimated in an ideal observer and the control signal required to meet with the power quality standards in a real converter. The error compensation technique makes the control of a PFC stage feasible. The concept has been proved in a common-ground bridgeless PFC converter avoiding the extra complexity of sensing the current in this type of converters. The controller has been validated, both in simulation and experimentally. The results obtained fulfill the standard IEC 61000-3-2 Class C, which is the most restrictive in between the ones that regulate single phase systems and less 16 A per phase. The compensation algorithm need to be completed to include also the switching delays. This would probably lead to an extra sensor/detector that measures the delay between the theoretical duty cycle and the real one. This task will be overcome in future works.

ACKNOWLEDGMENT

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