An Efficient FPGA Implementation of a Quadrature Signal Generation Subsystem in SRF PLLs in Single-Phase PFCs

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***Abstract*— Synchronization with the utility voltage is naturally carried out by a diode bridge stage in single phase active rectifiers, while an active synchronization is included in the control algorithms applied to modern bridgeless topologies. Sensorless line current rebuilding algorithms also need synchronization with the line voltage to compensate at least for part of the current estimation error. The PLL circuits employed in single phase AC-DC converters are reviewed and a new digital PLL algorithm, based on the synchronous reference frame, is proposed. It is implemented in a Field Programmable Gate Array (FPGA) to utilize the parallelism and superior time resolution. Considering a restricted frequency variation of the line voltage around the central frequency, the orthogonal signal is obtained by a discrete differential operator designed to ensure unity gain at the central frequency. Its performance, including the memory and computational cost, versus previously consolidated algorithms implemented in the same device is analyzed. Simulations and experimental results prove its suitable behavior in steady-state at different line frequencies and under line voltage and frequency transients.**

I. Introduction

The optimization of the grid infrastructure utilization and the harmonic reduction motivate the use of power factor correction (PFC) stages. Standards such as the EN 61000-3-2 and EN 61000-3-4 limit the harmonic content of the equipment connected to the utility, and the DO 160 F and MIL 461 F are applied to avionics. Lots of research effort has been put into defining PFC topologies and control techniques. Among them, the Boost converter, preceded by an AC to DC diode bridge rectifier is the most utilized topology for implementing single-phase front-end PFC stages in a range from hundreds W to a few kW, due to the higher switch utilization ratio and because the line current may not be interrupted during the whole switching period. In order to overcome the high output voltage imposed by the Boost topology, other alternatives based on direct or indirect converters are connected to the diode bridge. The off-line converter input current is shaped by an inner control action while the amplitude is set by the outer voltage control. Voltage and current phases are naturally synchronized by the diode bridge. Increasing the efficiency and the power density rate motivate the use of bridgeless topologies [1][2], with one converter for each line semiperiod, eliminating the previous diode bridge stage and, as a consequence, losing the natural grid synchronization.

Active adjustment of the current phase must be introduced with the elimination of the diode bridge to match the phase voltage and, as a consequence, the conversion system becomes more sensitive to phase and switching noises around the voltage zero crossing. Moreover, the quality of the phase adjustment has a large influence on the current sensing [3], [4] or estimation [5], [6] and control performance. An accurate zero-crossing detector with adequate noise immunity [7] helps to implement an effective compensation for the estimation errors in solutions that eliminates the current sensor. This fact has been proved in the current sensorless Boost converter operating in continuous conduction mode, in which the detection of the discontinuous conduction mode, close to the input voltage zero crossing instant is used to compensate for the current estimation errors [8].

Such inaccuracies due to grid voltage ZCD can be minimized by applying an appropriate synchronization method. Phase Locked-Loops (PLLs) have been extensively employed for synchronization of grid connected power converters under distorted operation conditions: harmonic distortion, voltage dips and unbalances among others [9]. The performance of single-phase PFCs has also been improved by the application of PLLs. This is the case of [10], where one PLL is employed to track the grid phase for generation of the reference current in linear controllers, and [11], where the estimated grid voltage is applied to the PLL input for synchronization of the sampling instants, minimizing of the low-frequency ripple in the output voltage. Another field of application within PFCs is closed-loop interleaved PFCs, where the phase difference between the parallelized stages is synchronized by means of PLLs [12], [13] and, more recently in [14] and [15], where the PLLs provide noise immunity to the digital controllers.

Phase Locked-Loops are well known subsystems, which allow one output and one input signals to be synchronized, maintaining the same frequency and phase once the PLL achieves synchronization [16]. Basically, the PLL consists of three basic building blocks: A phase detector (PD), which compares the phases of the input and output signals, providing an error signal whose mean value depends on the relative phase. A loop filter (LF), which filters out the error signal and provides a control reference for the third block, a volt-

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age/current controlled oscillator (VCO/CCO), which can be built as a trigonometric function and provides the in-phase output signal once the PLL is synchronized (locked). The characteristics of these building blocks determine the main characteristics of the PLLs (central frequency, pull-in and hold-in ranges, order...) and, hence, their performance and applicability to grid-connected converters.

Among the available PLL approaches in single-phase grid-connected power converters, such as the Enhanced PLL [17], the selective harmonics elimination [18] or the pq theory [19], the synchronously rotating reference frame (SRF) PLL is one of the most employed approaches. It applies the Park transformation and low-pass filter stage as PD and LF respectively. The common approach for the LF is a proportional-integral (PI) controller. The reference frame is rotated to align the input signal phasor and the d-axis. The general structure of the SRF-PLL is depicted in Fig. 1. The sampled grid voltage v_k is employed to define the in-phase (α_k) and the virtual in-quadrature (β_k) components of the grid voltage phasor in a stationary complex reference frame, accomplished through a quadrature signal generation (QSG) subsystem. The in-quadrature component β_k is conventionally obtained by a $T/4$ Delay (TD) block. These components must be normalized to avoid the effect of the grid voltage amplitude on the inner PI controller settings. Then, α_k and β_k are transformed into a rotating reference frame, $d-q$, which is synchronized with the grid by forcing the PLL phase (θ_k) to track the grid one. This is ensured by means of the PI controller, whose input is the q component, acting as the error signal. The component q_k is zero when the synchronization is achieved. The PI output is added to the nominal grid frequency, $2\pi f_0$, used as a PLL central frequency. In steady-state, the result is the actual grid frequency, ω_k. The grid voltage phase (θ_k) is obtained by integrating ω_k. The actual grid frequency ω_k can be employed to adjust the QSG frequency response by means of its feedback. The proposed QSG methods in Section III utilize both approaches.

The performance of QSG strategies in SRF-PLLs, and the required resources for their implementation in commercially available FPGAs, are evaluated in this work considering their application to the synchronization of a bridgeless PFC. Moreover, a new implementation approach of a QSG with reduced complexity is provided and evaluated both in simulation and experimentally versus other representative QSG subsystems. The paper is organized as follows: Section II will present the algorithms behind the QSGs based on the $T/4$ Delay, Inverse Park Transformation, Second Order Generalized Integration, Kalman Filter, Hilbert Transform and the proposed $T/4$ Delay using to samples. In section III the proposed PLL will be presented. In Section IV the performance of the PLLs based on the consolidated QSGs will be compared to the novel technique through simulations, showing the response in steady-state and under different transient conditions, such as harmonic distortion, frequency transients and voltage dips. Experimental verification of the proposed QSG using a constant number of samples and the comparison with the previous QSGs will be discussed in Section V, finalizing with conclusions.

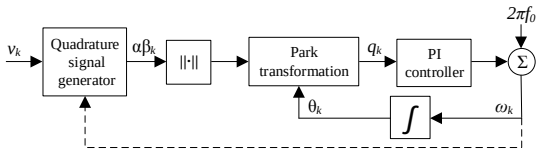

Fig. 1: General structure of a 1ϕ PLL based on SRF.

II. Consolidated Quadrature Signal Generation Subsystems in 1ϕ SRF-PLLs

Commonly employed QSG subsystems in discrete time SRF-PLLs are introduced and described in this section.

A. Delay based SRF-PLLs

The $T/4$ Delay (TD) is one of the first approaches employed for QSG implementation in SRF-PLLs. The input signal is delayed by an integer number of samples, matching a quarter of the fundamental period T and stored in a FIFO queue, to generate the in-quadrature signal. Its main drawback is due to the memory buffer employed. The buffer length depends on the sampling frequency, which must be high enough to minimize the effect of the current ripple caused by the PFC. Although the grid side filter helps in this task, the buffer and memory size are large. The PLL performance under grid voltage transients depends on the buffer length, so the overall PFC performance will be deteriorated by a slow response. Grid frequency deviation may result in an erroneous delay, generating an oscillation around the actual grid phase.

The effect of grid frequency variations can be partially compensated by means of variable delays, which increase the digital implementation complexity. An alternative approach, proposed in [20] and analyzed in detail in [21], is the Nonfrequency-dependent TD-PLL (NTD), where the QSG structure of TD is maintained but the effect of grid frequency variations is compensated through a new $T/4$ delay which replaces one of the trigonometric functions in the Park transformation. This modification increases the memory requirements but reduces the overall complexity by employing only one trigonometric function.

A different strategy for grid frequency variations is given in [22], again analyzed in detail in [21]. The compensation is applied to the PLL output, by adding/substracting a compensation phase (θ_k^{comp}), which depends on the integral action of the PI controller ($\Delta\omega_k$):

$$\theta_k^{comp}(\omega_k) = -\frac{T}{8}\Delta\omega_k \tag{1}$$

Again, two trigonometric functions are required for the implementation of the Park transformation and, in comparison to TD-PLL, a multiplication factor is added to the PLL output angle to correct its frequency response.

Two-Delay Signal Compensation (DSC) operators can be chained to obtain the in-quadrature signal [23]. The approach provides a better fundamental frequency negative-sequence rejection in the case of grid frequency variations, blocking

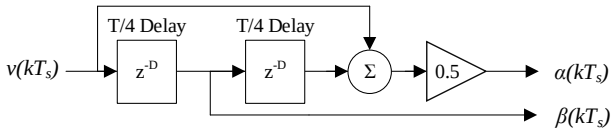

Fig. 2: Two-Delay Signal Compensation (DSC).

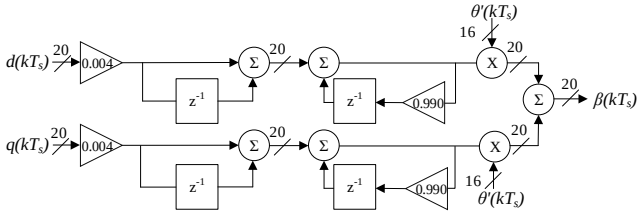

Fig. 3: Inverse Park (iPT).

odd harmonics of order $h = 4k - 1$ ($k = \pm 1, \pm 2, \ldots$) and slightly attenuateing even harmonics [21], [24]. Its harmonic blocking capabilities can be improved by adding new DSC operators before the PD and compensating the PLL output by adding a frequency-dependent phase, as is done in TD-PC PLL. However, as a consequence, the required resources for the digital implementation increases. The approach with two DSC operators, as shown in Fig. 2 and compared to TD-PLL, adds one additional multiplication and one memory buffer with length

$$D = \text{round}\left(\frac{N}{4}\right), \text{ with } N = \frac{T}{T_s} = \frac{2\pi}{T_s \omega_0} \tag{2}$$

where T_s is the sampling frequency.

B. Inverse Park (iPT)

The iPT can be applied to the PD output in order to obtain the in-quadrature signal if the PD is based on the Park transform [25], [26]. Firstly, the PD outputs must be filtered out to avoid high-frequency components and then, they can be transformed again into the stationary reference frame. The obtained β_k component can be employed as in-quadrature signal. Despite of being very simple, at least conceptually, the filtering stages must be properly selected to ensure a good balance between the dynamic and steady state responses. The recommendation in [9] for the first order low-pass filters' cut-off frequency is $\omega_f = 2\pi \cdot 70.7$ rad/s, which applying the transformation leads to a second-order system with $\xi = 0.707$ at 50 Hz. The approximate grid phase (θ'_k) is provided by the PLL stage. The analyzed implementation in this work is shown in Fig. 3.

C. Second-Order Generalized Integrator (SOGI)

Second order generalized integrators (SOGIs) are included within an active filter structure in [27], [28] for generation of the in-quadrature signal in single-phase SRF PLLs. The approach is based on two facts. Firstly, the SOGI structure

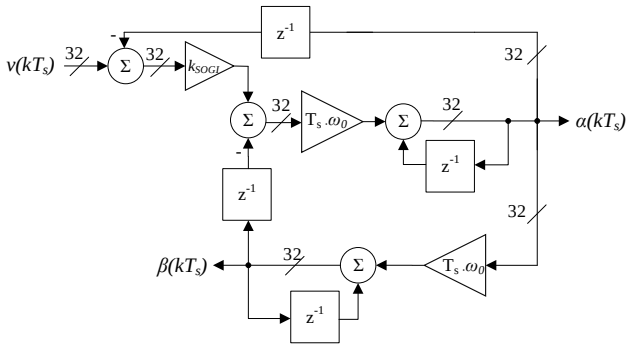

Fig. 4: Second-Order Generalized Integrator (SOGI).

provides a narrow notch at the resonance frequency (ω_r) which attenuates undesirable grid frequencies in the in-phase signal and, secondly, the SOGI structure can be optimized to generate the in-quadrature signal naturally. The SOGI transfer function

$$G_{SOGI}(s) = \frac{\omega_r s}{s^2 + \omega_r^2} \tag{3}$$

in a closed loop structure, operating as a QSG, is depicted in Fig. 4. The QSG behaves as an active filter where the notch width can be adjusted by means of gain (K_{SOGI} in Fig. 4) and ω_r can be provided by the LF in the PLL to follow the grid frequency. The balance between steady state performance and fast dynamical response is also adjusted through K_{SOGI} and depends on ω_r. The analysis carried out in [29] demonstrates that both the iPT and SOGI methods perform similarly by selecting $\omega_{LPF} = K_{SOGI}\omega_r$. From an implementation point of view, among the available approaches in literature [28], [30], the one shown in Fig. 4 has a minimal resources demand [28], [30], applying a constant $\omega_r = \omega_0$. The structure is very sensitive to PLL frequency oscillations due to the PD and LF employed. In order to overcome these limitations, the SOGI can be combined with a frequency locked loop (FLL) providing the resonance frequency and avoiding the PLL stage. This modification is explained in [9].

D. Kalman Filter (KF)

Kalman filters (KFs) provide an efficient computational algorithm to obtain an optimal estimation (in least squares sense) of the state of a certain process, linear (Linear KF) or non-linear (Extended KF), whose measurements are subjected to noise [31]. The real-time application of linear KFs allows the estimation of the state variables ($\mathbf{x}_k$) in a linear system to be refreshed each sampling instant k by balancing the available measurements (in vector $\mathbf{s}_k$) and the previous system states ($\mathbf{x}_k$) through certain filter gains, known as Kalman gains ($\mathbf{G}_k$), which are also updated each sampling interval. The system and measurement equations to be processed can be written as

$$\begin{cases} \mathbf{x}_{k+1} = \mathbf{A}_k \mathbf{x}_k + \mathbf{B}_k \mathbf{u}_k + \Gamma \xi_k \\ \mathbf{s}_k = \mathbf{C}_k \mathbf{x}_k + \mathbf{D}_k \mathbf{u}_k + \eta_k \end{cases} \tag{4}$$

where ξ and η are uncorrelated noise sequences with normal probability distributions, $\mathbf{A}_k$ and $\mathbf{C}_k$ are the state transition

and measurement matrices respectively and $\mathbf{u}_k$ is a deterministic input sequence, which can be avoided in electrical signals tracking [32]. The recursive Kalman filtering loop can be applied for optimal estimation of the system state vector but it requires matrix inversion. In order to reduce the computational burden the Limiting KF approach can be adopted if matrices $\mathbf{A}$ and $\mathbf{C}$ converge to certain steady-state values over time, which occurs in the case of application to QSGs due to the representation of electrical signals in a stationary reference frame [32], [33] and, hence, $\mathbf{A}_k$ and $\mathbf{C}_k$ matrices must be defined as

$$\mathbf{A}_k = \mathbf{A} = \begin{pmatrix} \mathbf{A_1} & 0 & \dots & 0 \\ 0 & \mathbf{A_3} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & A_n \end{pmatrix},$$

being

$$\mathbf{A_n} = \begin{pmatrix} \cos\left(n\frac{2\pi}{N}\right) & -\sin\left(n\frac{2\pi}{N}\right) \\ \sin\left(n\frac{2\pi}{N}\right) & \cos\left(n\frac{2\pi}{N}\right) \end{pmatrix} \tag{5}$$

and $\mathbf{C}_k = \mathbf{C} = (\ 1 \quad 0 \quad 1 \quad 0 \quad \dots \quad 1 \quad 0\ )$, where n is the maximum harmonic order considered. In [34], the approach employed is a limiting KF modeling the fundamental grid frequency. The recursive Kalman filtering loop to be evaluated each sampling interval $k = 1, 2, \dots$ is then reduced to the state-variable estimation prediction and the state-variables estimation update,

$$\begin{aligned} \hat{\mathbf{x}}_{k|k-1} &= \mathbf{A}_{k-1}\hat{\mathbf{x}}_{k-1|k-1} + \mathbf{B}_{k-1}\mathbf{u}_{k-1} \text{ and} \\ \hat{\mathbf{x}}_{k|k} &= \hat{\mathbf{x}}_{k|k-1} + \mathbf{G}_k\left(\mathbf{s}_k - \mathbf{C}_k\hat{\mathbf{x}}_{k|k-1} - \mathbf{D}_k\mathbf{u}_k\right) \end{aligned} \tag{6}$$

respectively. The initialization parameters are evaluated by $P_{0|0} = \text{Var}(\mathbf{x}_0)$ and $\hat{\mathbf{x}}_{0|0} = E(\mathbf{x}_0)$, the subindexes $k|k-1$ and $k+1|k+1$ denote the prediction and update of the variables and $\mathbf{G}_k$ becomes constant due to the signal representation employed. From an implementation point of view, it must be considered that *i)* the Limiting KF approach avoids matrix inversion and *ii)* increasing the number of states increases the number of registers and multiplications needed.

E. Hilbert transformers (HT)

The Hilbert Transform (HT) allows an analytic signal to be generated from a real signal with unity gain, except the DC component. Due to the fact that its frequency response extends across the whole spectrum, the digital realization requires an approximation. Three main approaches can be found in literature [35], [36]: complex filters, requiring hardware costly complex multipliers, the combination of two filters forming a 90° splitting network, commonly implemented as all-pass IIR filters with variable delays that deteriorate the PLL performance, and FIR filters, which requires the real part to be delayed to adjust the relative phases of in-phase and in-quadrature signals. The latter approach is the preferred method for PLLs in grid connected converters [37], [38], [39]. Both types III and IV FIR filters can be applied as Hilbert transformers for generation of the in-quadrature signal [40]

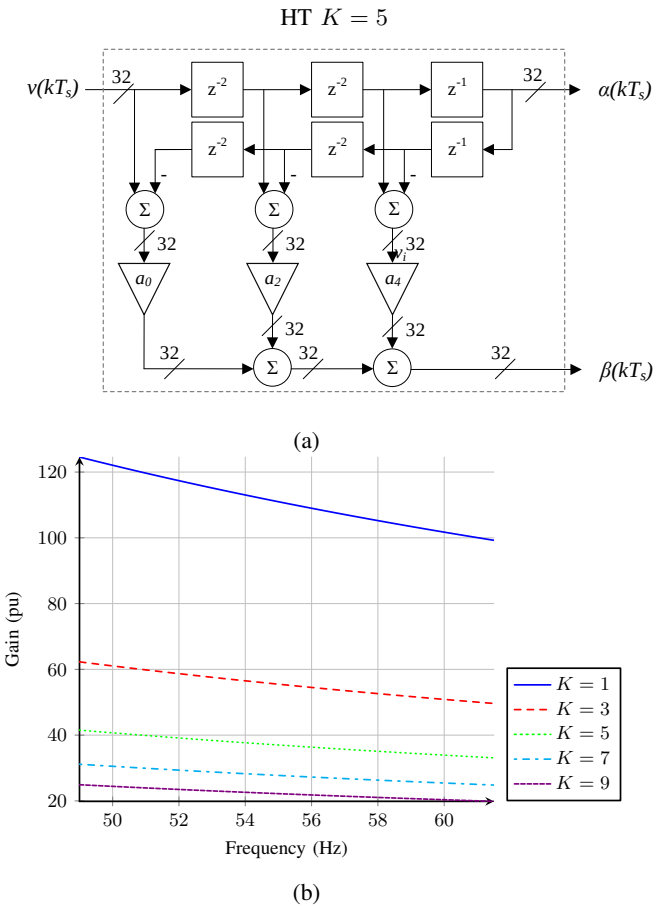

Fig. 5: Type III FIR Hilbert Transformer. a) Implementation and b) Required gain compensation ($f_s = 48.83$ kHz).

but type III requires half the number of multiplications [36]. In this case, the filter coefficients can be evaluated by applying

$$h(n) = \begin{cases} \frac{1-cos(\pi(n-K))}{\pi(n-K)} & n \text{ even}, \\ 0 & n \text{ odd} \end{cases} \tag{7}$$

where $1 \leq n \leq 2K-1$ and K is a positive even integer. Fig. 5.a shows the QSG implementation based on a type III FIR transformer. This implementation has two main issues: the gain of (7) at frequencies in the range $[49, 61.5]$ Hz varies (as is depicted in Fig. 5.b), which requires compensation at each operation frequency, and the constant delay z^{-K} must be compensated at the PLL output. An approach for the former issue is the adoption of multi-rate structures or look-up-tables, while for the latter a compensation term can be added in the PLL output.

III. Proposed Two-Samples ($2S$) Strategy

The proposed approach is oriented to improving the frequency tracking characteristics of the TD-PLL, while maintaining the design simplicity and reducing the memory requirements of the controller. The proposed subsystem considers a restricted frequency variation of the line voltage around the central frequency and utilizes signal variations within two consecutive sampling periods to generate the in-quadrature signal.

Ideally, the discrete in-phase (α_k) and in-quadrature (β_k) signals should be two pure sinusoidal signals with the same pulsation ($\frac{2\pi}{N}$), amplitude (A) and a relative phase of $-90°$:

$$\begin{cases} \alpha_k = A\cos\left(\dfrac{2\pi}{N}k\right) \\ \beta_k = A\sin\left(\dfrac{2\pi}{N}k\right) \end{cases} \tag{8}$$

where $N \in \mathbb{R}$ is defined in (2). This representation describes the grid voltage phasor movement referred to a stationary reference frame and can be employed to generate the in-phase and in-quadrature signals of the single phase SRF-PLL by assigning the sampled grid voltage (v_k) to α_k.

Then, three successive samples of α_k are related by

$$\begin{aligned} \alpha_{k-1} &= A\cos\left[\frac{2\pi}{N}(k-1)\right] \\ &= \alpha_k\cos\left(\frac{2\pi}{N}\right) + \beta_k\sin\left(\frac{2\pi}{N}\right) \end{aligned} \tag{9}$$

$$\begin{aligned} \alpha_{k+1} &= A\cos\left[\frac{2\pi}{N}(k+1)\right] \\ &= \alpha_k\cos\left(\frac{2\pi}{N}\right) - \beta_k\sin\left(\frac{2\pi}{N}\right) \end{aligned} \tag{10}$$

which, adding and subtracting (9) and (10), results in the following equations

$$\begin{cases} \alpha_{k-1} = \dfrac{\alpha_{k-2}+\alpha_k}{2\cos\left(\frac{2\pi}{N}\right)} \\ \beta_{k-1} = \dfrac{\alpha_{k-2}-\alpha_k}{2\sin\left(\frac{2\pi}{N}\right)} \end{cases} \tag{11}$$

From (8), the in-quadrature signal at $k+1$ can be written as

$$\begin{aligned} \beta_{k+1} &= A\sin\left[\frac{2\pi}{N}(k+1)\right] \\ &= \alpha_k\sin\left(\frac{2\pi}{N}\right) + \beta_k\cos\left(\frac{2\pi}{N}\right) \end{aligned} \tag{12}$$

From (12), and considering (11), the in-quadrature signal at k can be generated with three consecutive samples by applying

$$\begin{aligned} \beta_k &= \alpha_{k-1}\sin\left(\frac{2\pi}{N}\right) + \beta_{k-1}\cos\left(\frac{2\pi}{N}\right) \\ &= (\alpha_{k-2}+\alpha_k)\frac{\sin\left(\frac{2\pi}{N}\right)}{2\cos\left(\frac{2\pi}{N}\right)} + (\alpha_{k-2}-\alpha_k)\frac{\cos\left(\frac{2\pi}{N}\right)}{2\sin\left(\frac{2\pi}{N}\right)} \\ &= 2\alpha_k\frac{\sin^2\left(\frac{2\pi}{N}\right)-\frac{1}{2}}{\sin\left(\frac{4\pi}{N}\right)} + \alpha_{k-2}\frac{1}{\sin\left(\frac{4\pi}{N}\right)} \\ &= (\alpha_{k-2}-\alpha_k)\frac{1}{\sin\left(\frac{4\pi}{N}\right)} + \alpha_k\tan\left(\frac{2\pi}{N}\right) \\ &= (\alpha_{k-2}-\alpha_k)\,f_1(N) + \alpha_k f_2(N) \end{aligned} \tag{13}$$

which considers a constant N. Assuming that $\frac{1}{T_s} >> f_0$ and its integration within the single phase SRF-PLL structure as QSG, N can be dynamically adjusted to compensate grid frequency variations, resulting on

$$\beta_k = (\alpha_{k-2}-\alpha_k)\,f_1(N_k) + \alpha_k f_2(N_k), \tag{14}$$

where $\frac{2\pi}{N_k} = T_s\omega_k$ and ω_k is provided by the LF output feedback.

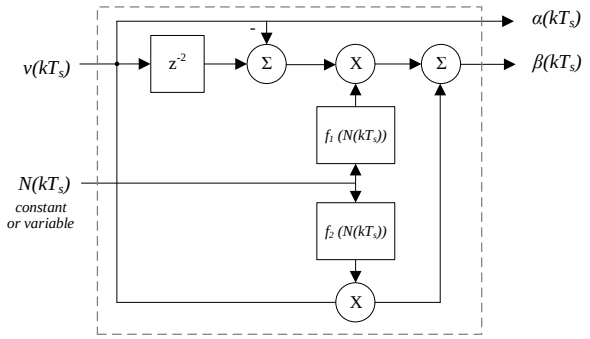

Fig. 6: Proposed PLL ($2S$-PLL) subsystem for quadrature signal generation.

Hence, two different approaches are possible: constant $N_k = N = \frac{2\pi}{T_s\omega_0}$, without grid frequency feedback and considering the nominal grid frequency ω_0, or a variable N_k provided by the PLL as an inner estimation of the actual grid frequency. The former leads to an implementation with a reduced number of FPGA resources, while the latter provides better performance in steady-state. The proposed quadrature signal generation subsystem based on these approaches is shown in Fig. 6. The corresponding discrete transfer function is $H(z)$, a high-pass FIR filter with two sample delays:

$$H(z) = \frac{1}{2}\left[\tan\left(\frac{2\pi}{N}\right) - \frac{1}{\tan\left(\frac{2\pi}{N}\right)}\right]\left[1 + z^{-2}\frac{\tan\left(\frac{2\pi}{N}\right) + \frac{1}{\tan\left(\frac{2\pi}{N}\right)}}{\tan\left(\frac{2\pi}{N}\right) - \frac{1}{\tan\left(\frac{2\pi}{N}\right)}}\right] \tag{15}$$

Evaluating the transfer function in the frequency domain with $z = e^{sT_s}$, gain and phase at the nominal grid frequency, unity gain ($|H(j2\pi f_0)| = 1$) and $90°$ phase lag are obtained. As a consequence, no gain and phase compensation are required, as occurs with HT. The drawback of the proposed approach, in comparison to HT, is that small gain and phase variations around the nominal frequencies are caused by grid frequency changes in the case of a constant N, as is shown in Fig. 7. This can reduce the PLL performance but, in applications with high accuracy requisites, the variable N would allow this effect to be compensated.

In order to simplify the implementation of both approaches, a further assumption can be made when $1/T_s >> f_0$ and, then, $f_1(N)$ and $f_2(N)$ can be approximated by their first order Taylor series, $\frac{N}{4\pi}$ and $\frac{2\pi}{N}$ respectively. As a consequence, the constant N approach requires one multiplication and division less than the variable N one. In this work, the cases of varying N and constant N are both studied, denominated $2S_v$-PLL and $2S_c$-PLL respectively. Fig. 8 shows the $2S_c$ implementation.

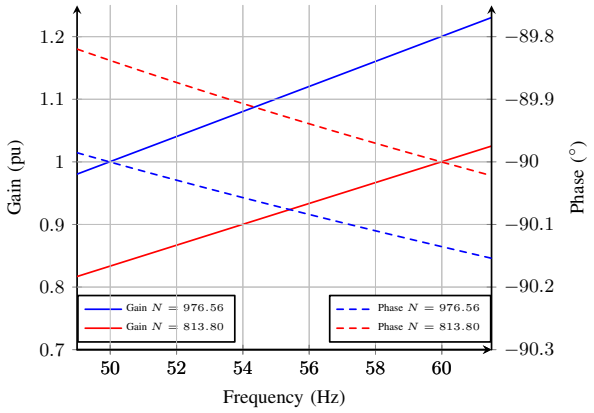

Fig. 7: Frequency response of $2S_c$-PLL.

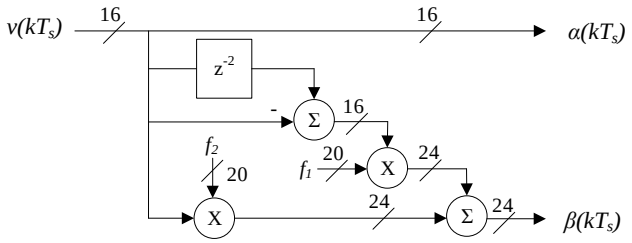

Fig. 8: QSG subsystem with $2S_c$ approach.

IV. Simulation Analysis of QSG Methods in SRF-PLLs

This section compares the performances of 12 QSG methods applied to the same SRF-PLL structure. The analyzed methods are TD, TD with phase correction (TD-PC), DSC with phase correction, inverse Park transformation (iPT), SOGI, HT, Kalman filters tracking the fundamental and 3^{rd} and 5^{th} harmonics, in both the standard (KFH) and Limiting (LKFH) approaches, the Limiting Kalman filter with only the fundamental (LKF1), and the proposed approaches with variable ($2S_v$) and constant ($2S_c$) N. All the discretized versions of these methods have been evaluated with MatLab/Simulink® in both, steady-state and dynamic response tests. The results obtained are compared in terms of phase error (voltage and PLL output phases) and, for comparison purposes, a phase error limit equal to 0.57 ° is depicted. This limit corresponds to the required precision in Phasor Measurement Units (PMUs) to obtain a Total Vector Error (TVE) less than 1 % [41], which ensures an accurate estimation of power system status by the utilities. In the case of transient response analysis, the measured response time (t_R) corresponds to *i)* the time over the PMU TVE 1 % limit (if it is crossed at least two times) or *ii)* the time needed to reach 5 % of the steady-state value after the transient. The measured phase error signals are depicted in Fig. 9 to 12. The measured t_R and maximum and minimum errors are given in Table I.

The inner PI controller, employed as PD, has been adjusted following the recommendations in [9] with $T_{settling} = 0.2$ s. The discretization has been carried out with $f_s = \frac{1}{T_s} = 48.83$ kHz, the sampling frequency at which the PLL operates in the FPGA development board used. This sampling frequency, with $f_0 = 50$ Hz and applying (2), results in $D = 244$ and $N = 976.56$ respectively. The $2S_c$ method employed has been implemented using a first-order Taylor series approach, which results in a 29 parts per million (ppm) maximum error in the frequency range $[49, 51]$ Hz.

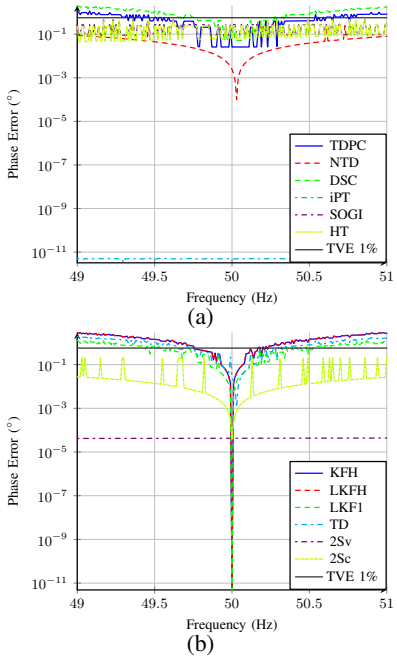

Fig. 9: Steady-state average phase errors of the SRF PLLs with the analyzed QSG. VCO central frequency $f_{0,PLL} = 50$ Hz, $T_{set} = 0.2$ s and $f_s = 48828.125$ Hz.

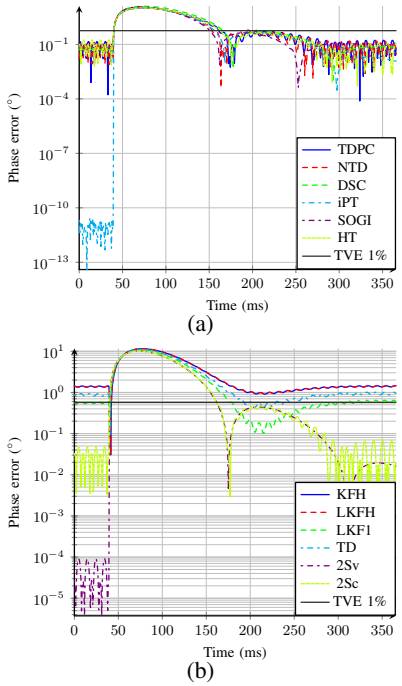

Fig. 10: Response to frequency steps (51 Hz → 49 Hz). VCO central frequency $f_{0,PLL} = 50$ Hz, $T_{set} = 0.2$ s and $f_s = 48828.125$ Hz.

A. Steady-State performance

The steady-state errors, due to the analyzed QSG methods inside the SRF-PLL structure and applying input signals with frequencies in the range $[49\ \text{Hz}, 51\ \text{Hz}]$, are shown in Fig. 9. All the QSG methods have been adjusted to operate with $f_0 = 50$ Hz and the results obtained show that all the PLLs provide an accurate phase tracking around the VCO central frequency, being below the PMU limit. The QSG method resulting in the lowest phase error is the iPT Transform and the DSC generates the worst results when the grid frequency moves from the central VCO frequency.

B. Frequency variations

Frequency steps, from 51 Hz to 49 Hz, have been applied to the analyzed SRF-PLLs at 40 ms. The results obtained are shown in Fig. 10. The methods with poorest performance are those based on KF due to the frequency mismatch at the fundamental frequency: both KFH and LKFH are always over the PMU TVE 1 % limit while LKF1 is on the limit before and after the transient. The TD method result in an equivalent performance. The HT method exhibits an error ripple which becomes worse during the transient. TD-PC, NTD, iPT, SOGI and the proposed method show a similar performance.

C. Harmonic distortion

The performance of the analyzed PLLs has been tested with harmonic voltage distortion (3 % and 2 % of 5^{th} and 7^{th} harmonics respectively, fundamental at 50 Hz). This distortion is applied at 40 ms. All the previously proposed QSGs keep the maximum phase error below 0.57 ° (the PMU TVE 1 % limit), the proposed methods exceed this value by 0.05 °.

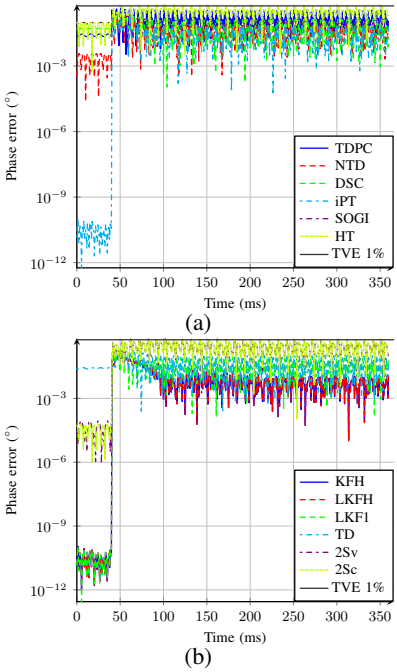

Fig. 11: Response to harmonic distortion at 40 ms (3 % and 2 % of 5^{th} and 7^{th} harmonics respectively, fundamental at 50 Hz). VCO central frequency $f_{0,PLL} = 50$ Hz, $T_{set} = 0.2$ s and $f_s = 48828.125$ Hz.

D. Voltage dips

Figure 12 shows the performance of the proposed PLLs under voltage dips. The initial grid frequency is 50 Hz and a 60 % voltage dip occurs at 40 ms. All the previously proposed methods result on a poor performance during the transient. The proposed methods operate below the PMU TVE 1 % limit.

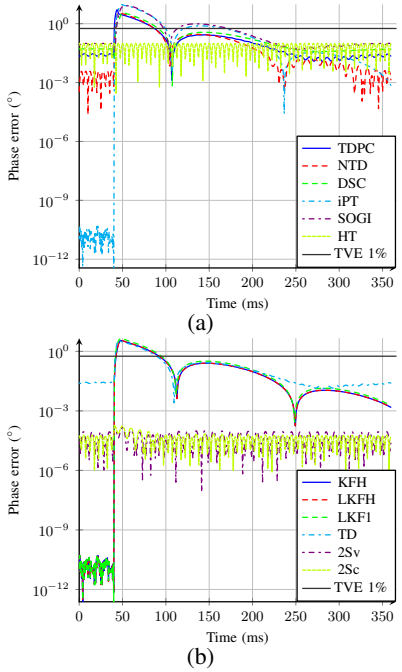

Fig. 12: Response to a voltage dip (60 %) at 50 Hz (The transient is applied at 40 ms). $T_{set} = 0.2$ s and $f_s = 48828.125$ Hz. VCO central frequency $f_{0,PLL} = 50$ Hz, $T_{set} = 0.2$ s and $f_s = 48828.125$ Hz.

V. Experimental results

The performance of the QSG methods has also been analyzed experimentally in a Xilinx FPGA (XC7A100T-1CSG324C). Grid voltage signals are provided by means of a programmable power source (Pacific Power Source 345-AMX). The selected sampling frequency is 48828.125 Hz. Therefore, according to (2), $N = \frac{f_s}{f_0} = 48828.125\ \text{Hz}/50\ \text{Hz} = 976.56 \approx 977$. The comparison of the analyzed implementations and the measurement of the phase tracking capability of each method is provided below. Since the phase angle of the input voltage is unknown, for clarification's sake, the input signal to the PI controller, i.e. phase error (q_k) will be employed for evaluation purposes.

A. Comparison of FPGA implementations

The number of bits utilized to represent the signals of the digital circuits that implement the different algorithms are selected according to the criteria described next. Optimization and later comparison of hardware resources affect only the QSG since the remaining stages are common in all the implemented solutions. A 16-bits input v_k signal resolution is adopted, obtained from a sigma-delta ADC.

Table I: Measured max/min phase errors and response times.

QSG	Steady state		Frequency var.		Harmonic dist.		Voltage Dip	
	ϵ_{max} $(^\circ)$	ϵ_{min} $(^\circ)$	ϵ_{max} $(^\circ)$	t_R (s)	ϵ_{max} $(^\circ)$	t_R (ms)	ϵ_{max} $(^\circ)$	t_R (ms)
TD-PC	1.2	0.026	10	0.12	0.44	120	5.2	46
NTD	0.27	≈ 0	11	0.11	0.17	172	3.5	45
DSC	2.0	0.052	13	0.13	0.23	282	3.7	48
iPT	≈ 0	≈ 0	11	0.12	0.15	69	9.3	57
SOGI	0.47	0.09	12	0.11	0.2	148	8.3	53
HT	0.46	0.046	10	0.12	0.65	60	0.1	10
KFH	2.9	≈ 0	12	0.26	0.1	82	3.5	49
LKFH	2.9	≈ 0	12	0.26	0.1	83	3.5	49
LKF1	1.3	≈ 0	11	0.26	0.13	65	4.4	53
TD	2.0	0.0011	11	0.26	0.19	259	3.4	47
$2S_v$	≈ 0	≈ 0	10	0.12	0.66	132	≈ 0	30
$2S_c$	0.21	≈ 0	10	0.12	0.62	125	≈ 0	60

All values below 10^{-3} have been rounded to ≈ 0 because the result is smaller than the acquisition and quantization error.

- TD-PLL Since it is based on a FIFO memory and, taking into account the memory configuration available in the FPGA (16-bits bus), no further optimization is needed.
- $2S_c$-PLL The number of bits used is based on the resolution needed to implement the constants f_1 and f_2 as described in Fig. 8.
- SOGI-PLL In this case, the resonant frequency, f_0, is a key factor that requires an accurate quantization to be carried out, as shown in Fig. 4. The following examples illustrate the relation between the number of bits and the accuracy of the target 50-Hz resonant frequency: for 22 bits, $f_0 = 49.7651\ Hz$, for 26 bits, $f_0 = 50.0176\ Hz$ and for 32 bits, $f_0 = 50.0002\ Hz$.
- iPT-PLL As represented in Fig. 3, the same number of bits as for the direct Park Transform, i.e. 20 bits, has been used. The guideline followed was to use the same resolution as with the direct Park transform (20 bits).
- HT-PLL The Hilbert transform implemented work outside the unity gain area (otherwise, a higher number of stages would be needed). Therefore, a compensation gain is mandatory and, as a consequence, a high resolution is needed. As is shown in Fig. 5, 32-bit word length is selected for $K = 5$.
- $2S_v$-PLL uses the same criterion as with the $2S_c$-PLL.
- The LKF1-PLL has been implemented with 32 bits word length, which is the size required to implement the Limiting Kalman filtering loop at the fundamental grid frequency with enough resolution. The number of bits can be reduced by including harmonics higher than the fundamental grid frequency in (4)-(7) but, as a result, the number of multipliers and registers would increase, without achieving significant accuracy improvement at the fundamental.

Finally, the resources used by all the analyzed solutions are compared. The results were obtained using the tool provided by *XILINX*® and are summarized in Table II.

B. Frequency step

The results obtained in the case of a frequency step from 49 Hz to 51 Hz are shown in Fig. 13 for both the TD-PLL and the proposed $2S_c$-PLL. In this case, the TD-PLL and the proposed $2S_c$-PLL were selected because of the small amount of resources used and their easy implementation. Taking into account the parameters used to tune the PI stage [9] (which is the same for all the implementations), both solutions show similar behavior. As a consequence of the conservative design of the PI stage and the superior speed of the $2S_c$-PLL compared to the TD-PLL in generating the new quadrature signals as a result of the new operating point (as will be shown in following subsections), the PI stage, which play the most significant role, slows down the whole system. Even though the TD-PLL, which is the slowest option, would need a quarter period to adjust the β to the new situation, the PI increments the time needed by the PLLs to adjust to the new frequency specification, hiding the performance of the QSG. Therefore, as can be seen in Fig. 13, both solutions show identical performance.

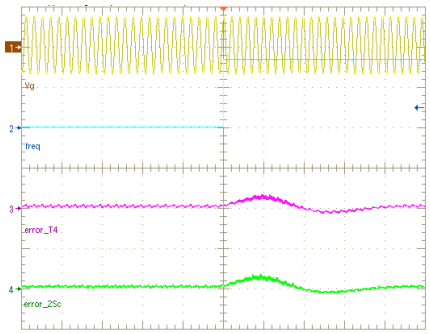

Fig. 13: Frequency step from 49 to 51 Hz.

C. Distorted input voltage

Initially, the grid voltage is composed of a pure sinusoidal waveform, whose amplitude is $50\sqrt{2}\ V$. At a certain time,

Table II: Summary of the FPGA resources used by different PLL implementations normalized respect to the TD-PLL solution.

Slice Logic Utilization	Implemented PLL												
	TD	$2S_c$		$SOGI$		iPT		HT		$2S_v$		$LKF1$	
	Tot.	Tot.	%	Tot.	%	Tot.	%	Tot.	%	Tot.	%	Tot.	%
Slice Registers	2187	2140	97.7	2407	110.1	2257	103.2	2617	119.7	2122	97.0	2196	100.4
Slice LUTs	2885	3069	106.4	4301	149.1	3352	116.2	3198	110.8	2893	100.3	3142	108.9
Occupied Slices	956	981	102.6	1427	149.3	1119	117.1	1052	110.0	942	98.5	979	102.4
LUT Flip Flop pairs	3069	3234	105.4	4576	149.1	3575	116.5	3418	111.4	3080	100.4	3293	107.3
Bonded IOBs	31	31	100.0	31	100.0	31	100.0	31	100.0	31	100.0	31	100.0
RAMB18E1/FIFO18E1s	3	2	66.7	2	66.7	2	66.7	2	66.7	2	66.7	2	66.7
BUFG/BUFGCTRLs	1	1	100.0	1	100.0	1	100.0	1	100.0	1	100.0	1	100.0
DSP48E1s	10	10	100.0	12	120.0	18	180.0	20	200.0	26	260.0	26	26.0

some harmonic distortion is added: 3 % of 5^{th} and 2 % of 7^{th}. Fig. 14 shows the performance of the $2S_c$-PLL compared to SOGI and HT PLL simultaneously. These implementations were selected in this case because:

- The proposed $2S_c$ and Hilbert PLL have similar frequency responses, eventhough the Hilbert Transformer has a higher immunity to high-frequency noise. However, this characteristic does not affect the performance of the complete system thanks to the low-pass effect of the PI stage. As expected, the results of both options obtained experimentally are very similar, in agreement with those obtained from the simulation results and the theoretical development, as can be seen in Fig. 14.
- The expected superior performance of the SOGI implementation compared to proposed one, is confirmed with the frequency response observed in the simulation results the frequency response of the simulation results. Again, as expected, SOGI has greater immunity to low-frequency harmonics, as shown in Fig. 14. However, this error corresponds to the 5^{th} and 7^{th} harmonic and does not affect the fundamental frequency of the grid voltage. Therefore, the phase accuracy of the proposed PLL is not affected, in consistency with the simulations results.

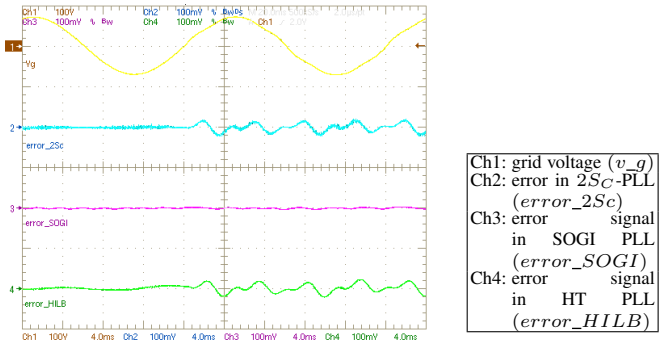

Fig. 14: Harmonic distortion step.

D. Voltage dip

Finally, a comparison of the proposed $2S_c$ against SOGI and iPT PLL is shown in Fig. 15. In this case, a voltage dip from 50 V_{rms} to 20 V_{rms} was applied at a certain time, comparing the response time needed by the three different options chosen. As can be seen in Fig. 15, SOGI and iPT have identical response times to a voltage dip of 60 % of v_g, agreeing with the simulation results and the theoretical development. However, as shown in Fig. 15, the proposed $2S_c$-PLL shows faster response and similar behaviour in steady state. Eventhough high-frequency noise can be appreciated in the error signal of the proposed PLL in Fig. 15 (*error_2Sc*), this characteristic does not affect the PLL accuracy thanks to the low-pass effect of the PI stage.

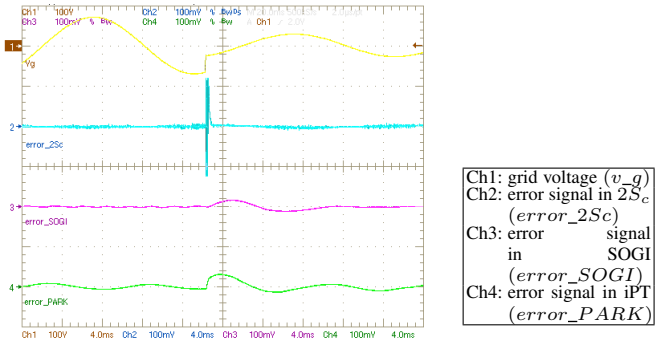

Fig. 15: Voltage dip (60 %).

VI. Conclusion

Active synchronization with the grid voltage improves noise immunity in the phase detection in bridgeless PFC. Present PLL techniques, oriented to matching the line phase in a broad frequency range, result in sophisticated algorithms that require complex and large digital circuits to implement operations with high-resolution signals and include many delay blocks. A novel approach for generation of the quadrature signal based on a high-pass filter in $1-\phi$ SRF-PLLs has been proposed. Around the central frequency, and considering the possible frequency deviation range of the line frequency, $\pi/2$ rad phase lag and unity gain are imposed and the amplitude deviation due to the $+20$ dB/dec gain slope results in minimum distortion. Using simulation models, two implementations of the proposed method have been analyzed and compared against consolidated SRF PLL algorithms. The test has included steady-state operation with ideal and distorted waveforms, together with frequency and voltage transients. For a fair comparison of the performance and hardware resources, the simulation models have been translated into a hardware description for a later implementation using standard synthesis

tools and the same FPGA device. Further optimization can be achieved with an "*ad hoc*" hardware description and further scaling, quantization and saturation of the digital variables. Experiments have been carried out with the consolidated algorithms, and a simplified version of the proposed algorithm using constant number of samples even under line frequency variations. The results obtained for zero-crossing detection are consistent with the simulations, showing that the proposed QSG achieves faster response and equivalent steady-state performance with only two samples. Hence, it results in a better overall trade-off considering performance and the digital circuit resources required for implementation in comparison to the consolidated approaches, in which the number of required samples is higher and depends on the grid frequency. For limited frequency deviation, the proposed PLL is implemented with a constant number of samples, N, leading to further simplification, without significantly affecting its performance.

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