Two-Sample PLL with Improved Frequency Response applied to Single-Phase Current Sensorless Bridgeless PFCs

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***Abstract*— A new implementation of the recently proposed fixed-frequency two-sample (2S) quadrature generation subsystem (QSG) digital Phase Locked Loop PLL, applicable to single-phase Power Factor Correction (PFC), is proposed. Its characteristics are high accuracy and low computational burden. The proposed PLL includes a frequency feedback loop to improve the synchronization under line frequency variations. Its performance within a digital controller of a current sensorless bridgeless PFC is evaluated by simulations and experimentally. The obtained results are compared with previously published PLLs in the literature.**

***Index Terms*—PLL, Bridgeless, converter, sensorless, synchronization, computational burden.**

I. INTRODUCTION

Power Factor Correction (PFC) stages are responsible for complying the standards regarding the current waveform on the grid side [1] and they are designed with the aim of obtaining high efficiency and power density [2]. At the same time, the PFC regulates the voltage level at the DC side under diverse grid and load conditions.

PFC stages have evolved to bridgeless topologies, where the power is directly converted with the aim of reducing the conduction losses, increasing the PFC efficiency [3]. As a drawback, the complexity of the current measurement circuitry increases [4], and makes the grid synchronization more difficult [5] due to the elimination of the diode bridge. Therefore, current sensorless solutions are interesting but also challenging, because the duty cycle in each switching period throughout the line period is estimated, either in advance or on-line; directly or through the estimation of the line current to be the input of a current controller, as in the with-sensor case. In that case, an active minimization of the estimation errors is required [6].

Here, an observer replaces the current sensor and a synchronization signal is employed to improve the current reconstruction. Simple synchronizations strategies such as Zero Crossing Detection (ZCD) may result in a low performance in weak electrical grids, where power quality events and variations frequently occurs [6], so Phase Looked Loops (PLL) are preferred for synchronization purposes [7]–[9]. The PLL synchronization signal is also used as a more robust reference for the linear current control [7].

The simplest structure of a PLL consists of a Phase Detector (PD), a Loop Filter (LF) and a Voltage Controlled Oscillator (VCO). The PD compares the inner synchronization signal generated by the PLL with the grid voltage measurement. The average error signal represents the phase error at the fundamental grid frequency while the LF, typically a PI controller, must filter out the PD output. The PI controller output is added to the central frequency of the PLL to adjust its inner frequency estimation, which matches the input one once the PLL is locked. Then, the VCO generates a per-unit sinusoidal signal, whose frequency and phase matches the grid one. In the case of single-phase PLLs with PD based on the Park transformation [10], a quadrature signal generator (QSG) subsystem is additionally required [11].

Selecting the most suitable PLL for each application requires assessing the steady-state and dynamic responses as well as the computational burden of the PLL under the operation conditions [12]. In the case of weak grids, with relatively large or fast frequency variations, ensuring an appropriate PLL performance requires to adjust its functional blocks to deal with such operation conditions [13].

A novel PLL, with low computational burden and fast and accurate response in the case of grid frequency steps and variations, is proposed in this work. The proposed PLL is designed to be embedded within the digital controller of a current sensorless bridgeless PFC and provides the required synchronization signal. The paper is organized as follows.

Section II compares the architecture of the proposed 2SC PLL with previously proposed PLLs applicable to bridgeless PFCs. In section III, the performance of the proposed PLL is compared by simulations while in Section IV the comparison is carried out experimentally. In both sections, harmonically distorted grid voltages and fundamental frequency steps or ramps are applied. Conclusions evaluating the applicability of the proposal to current sensorless Bridgeless PFCs are finally provided.

II. Low Computational Burden PLLs in Current Sensorless Bridgeless PFCs

According to the structure shown in Fig. 1, the PFC input and output voltages, v_g and v_{dc} respectively, are acquired for the digital controller generates input to the pulsewidth modulator (PWM). The sampled v_g is the input to the PLL, which generates a per-unit in-phase sinusoidal signal. A conventional linear current control, with a damped proportional resonant controller, is adopted. The outer, and slowest, control loop regulates the output voltage and provides the amplitude of the input current, which must be impressed by the inner current controller. Since the application is a current sensorless PFC, the inductor current is estimated through a current rebuilding algorithm. Finally, the gate signals are generated by means of the PWM and applied to the power devices through the appropriate driver circuits.

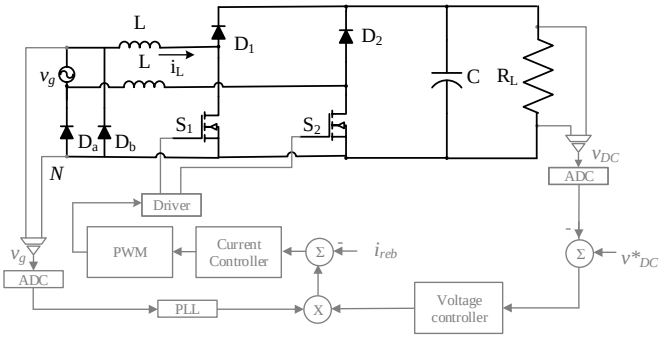

Fig. 1. Bridgeless PFC with the evaluated control structure and synchronization subsystem.

The following subsections describe the proposed PLL and the other architectures used for evaluation purposes. The PLLs employ a PD based on the Park transformation after a QSG: T/4 delay, the signal derivative and the two-samples (2S) strategy proposed in [14]. All of them are analyzed with and without FFB path. In this work, a new version of the derivative PLL, which includes a FFB path, has also been developed for comparison.

A. T/4 PLL

The conventional T/4 PLL, shown in Fig. 2, uses a quadrature signal, obtained in this work by means of a fixed-length memory buffer to minimize computational resources. Therefore, the memory buffer, allocates a constant number, N, of samples of v_g per grid period at the central frequency, T, [11], [15], that results in the in-phase signal α. The T/4 delay of α generates β. The fixed-length of the memory buffer is a limitation that makes this QSG to operate properly around the nominal grid frequency. If the grid frequency deviates sufficiently from the center one, the in-phase and in-quadrature signals would not be orthogonal, resulting in synchronization errors [11].

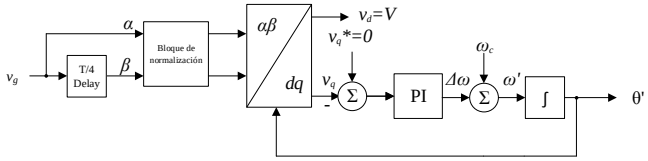

Fig. 2. Conventional T/4 PLL.

In [16], the evaluation of T/4 PLLs with a secondary control loop demonstrates that the inclusion of a frequency feedback loop (FFB) improves the T/4 PLL performance when grid frequency ramps are applied.

B. T/4 PLL with frequency feedback loop (T/4 FFB)

Also, in [16], the T/4 PLL with frequency feedback path obtained better performance under frequency steps. The structure is shown in Fig. 3, where the frequency feedback gain, v_{FB}, is defined as in [17],

$$v_{FB} = \mathrm{sgn}(\Delta\omega) \cdot k'_{FB} \tag{1}$$

with $\mathrm{sgn}(\Delta\omega)$ ensuring the stability of the system and k'_{FB} adjusting the dynamics.

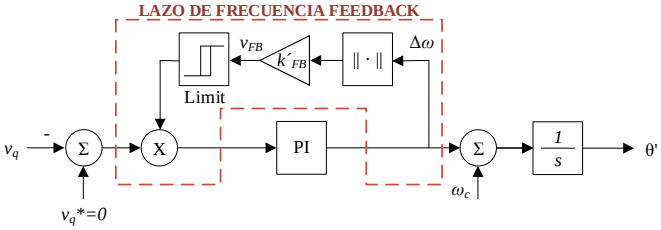

Fig. 3. Implementation detail of the frequency feedback loop.

C. Derivative PLL

Derivative QSGs in PLLs, shown in Fig. 4, have been widely applied in the continuous domain [18] [19]. Digital PLLs, based on this approach, provide an accurate synchronization signal, although to increase the QSG precision requires improving the numerical evaluation of the derivative, which increases the computational burden [20].

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Moreover, noisy inputs to these PLLs reduce the synchronization accuracy due to the noise amplification in the differentiator. Increasing the number of considered samples reduces this effect but, to compensate the delays in β, extra delays must also be included in α to maintain the orthogonality, which result in a phase-error, which requires later compensation.

TABLE I
APPROACHES TO THE DERIVATIVE FUNCTION WITH FIXED FREQUENCY

Method	α	$\beta = \frac{\dot{x}(t)}{\omega'(t)}$
Backward [21]	$x(t)$	$\frac{1}{\omega'}\frac{x(t)-x(t-T_s)}{T_s}$
Centered Differencing	$x(t-T_s)$	$\frac{1}{\omega'}\frac{x(t+T_s)-x(t-T_s)}{2T_s}$
Richardson's Extrapolation	$x(t-2T_s)$	$\frac{1}{\omega'}\frac{-x(t+2T_s)+8x(t+T_s)-8x(t-T_s)+x(t-2T_s)}{12T_s}$

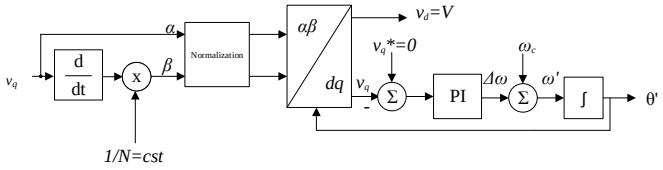


Fig. 4. Derivative PLL.

D. 2S PLL

The strategy proposed in [14] allows β to be obtained by applying finite differences around an operation point, which can be dynamically adjusted as a function of the PLL frequency ω'. Computational delays are compensated within the QSG. The in-quadrature signal at instant *k* (β_k) is generated with three consecutive samples of the grid voltage, minimizing the memory requirements of the QSG and keeping the orthogonality in the case of frequency variations:

$$\beta_k = (\alpha_{k-2} - \alpha_k)\frac{4\pi}{N} + \alpha_k \frac{2\pi}{N} \quad (2)$$

$$N = \frac{2\pi}{T_s \omega'} \quad (3)$$

Assuming a fast sampling frequency, (2) is simplified in [14] through the first term of the Taylor series of the trigonometric functions. Two approaches are possible: variable N (2SV-PLL), with N being dynamically adjusted by ω', or constant N (2SC-PLL). The first option provides a better stationary response, but for further computational reduction, a constant number of samples per period of the fundamental grid frequency, N, is adopted as shown in Fig. 5.

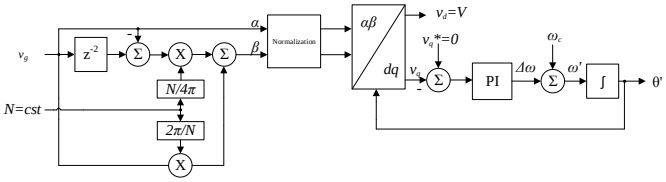


Fig. 5. 2SC PLL.

E. Proposed Two-Samples PLL with Frequency Feedback (2SC-FFB PLL)

To improve the performance of the 2SC-PLL first described in [6], in this work it is proposed to include a secondary feedback control path, as shown in Fig. 6. Due to the FFB action, it presents zero phase-error in steady-state under slow grid frequency variations, resulting in a fast signal tracking.

The detail of the FFB structure is the one shown in Fig. 3, where the frequency feedback gain, v_{FB}, is defined as in (1).

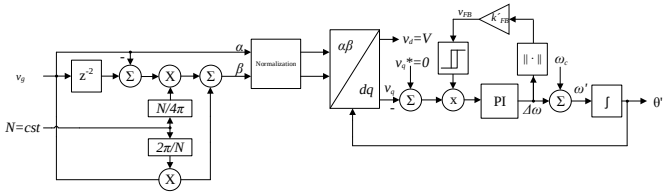


Fig. 6. Proposed 2SC PLL with feedback frequency loop.

III. SIMULATION RESULTS

The six PLLs described in the previous section are simulated using the same parameters for the PI controller, designed according to [7] and integrated in a single-phase bridgeless boost PFC. The simulation parameters are included in Table II.

TABLE II. SIMULATION PARAMETERS

PARAMETER	VALUE
Nominal frequency	50 Hz
K_p	45.25
K_i	1024
K_{FB}	0.5
Ts	$2.48 \cdot 10^{-5}$ s
N	$7.812 \cdot 10^{3}$

The results obtained in this section are compared in terms of phase error, a phase error limit equal to 0.57 % is also shown as a reference. This limit corresponds to the precision required in phasor measurements units (PMUs) to obtain a total vector error (TVE) less than 1 % [22].

In Fig. 7, it is presented a comparison among the derivative PLLs presented in Table I. Because all curves are quasi-coincident and the Backward PLL has a lower computational burden, henceforth the Backward PLL will be used as the

representative of its family in this work.

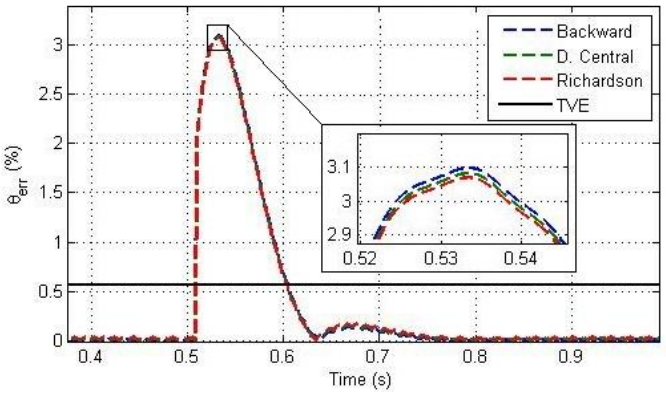


Fig. 7. Phase error due to a frequency step from 49 to 51 Hz in perceptual values.

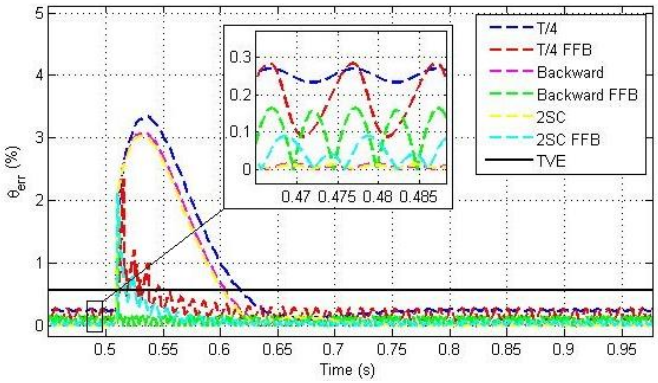


Fig. 8. Phase error due to a frequency step from 49 to 51 Hz in perceptual values.

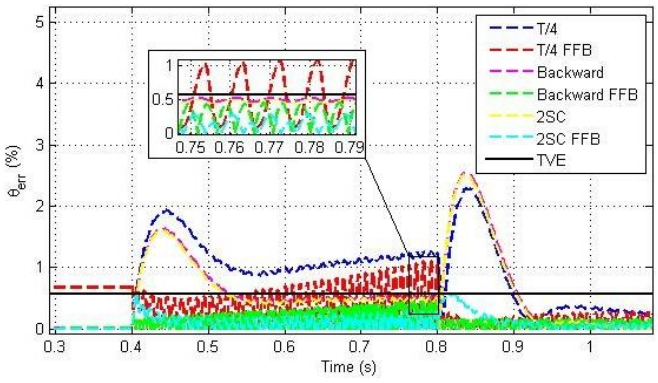


Fig. 9. Phase error due to a frequency ramp of 0.4 Hz/s during 0.5 s in perceptual values.

The response of the analyzed PLLs to a +2 Hz frequency step is shown in Fig. 8. The T/4 PLL exhibits the slowest response to the transient and the greatest overshoot, reaching a maximum phase error equal to 3.40 %. The 2SC and the derivative PLL performs similarly with and without FFB (the error of the derivative PLLs is 0.05 % higher than those of 2SC). The PLLs with frequency feedback loop perform better, being the 2SC FFB the best one with the phase error showing a 2.10 % overshoot and steady-state error similar than in the case without FFB. The solution with FFB have faster responses with 0.07 s of settling time. The 2S and Backward have a settling time of 0.24 s and the T/4 shown the worst results with 0.26 s.

In Fig. 9, the response to a frequency ramp of 0.4 Hz/s applied during 0.5 s is shown. All the tested PLLs, but the FFB ones, result in phase error overshoots at the beginning and end of the frequency ramp. Again, the 2SC FFB and the Backward with FFB perform better during the ramp. In contrast, the conventional T/4 and the T/4 PLLs with FFB increase the ripple and error as the ramp occurs due to the fixed-length buffer. Both the analyzed derivative PLLs perform similarly. The settling time is lower using PLLs with FFB path, achieving 0.42 s in the case of 2S and Backward. Again, the worst result is obtained by T/4 PLL, whose settling time reaches 0.59 s.

In Fig. 10, the phase error due to individual voltage harmonics is analyzed. The first 25 harmonics, with amplitudes according to the maximum limits fixed by the standards UNE 50160 and IEEE 519, are applied. The T/4, Backward and 2S PLL obtained values under the TVE limits, getting the best results with the last two. The solutions with FFB are the worst under distortion condition. All values of the Backward FFB PLL phase error are over the TVE. While the T/4 and 2S with FFB only exceeds that limit for the case of the 3rd, 5th, 7th, 11th and 13th harmonics, with the 2SC FFB with lower values.

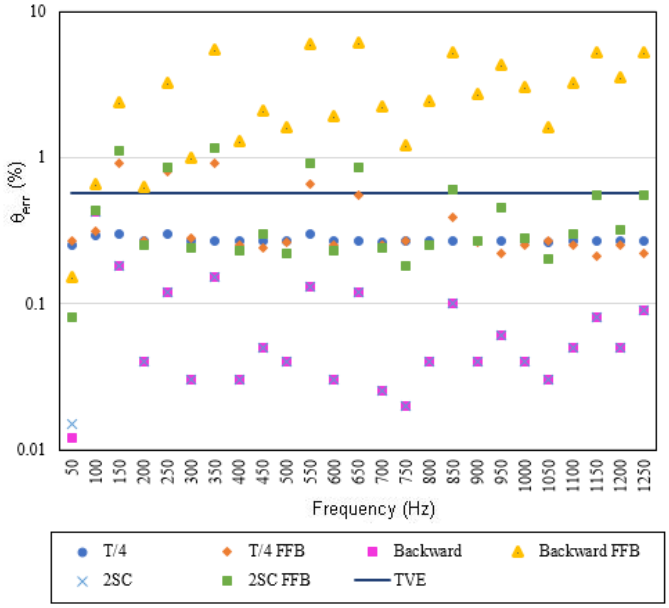


Fig. 10. Phase error due to a harmonic distortion.

IV. Experimental Results

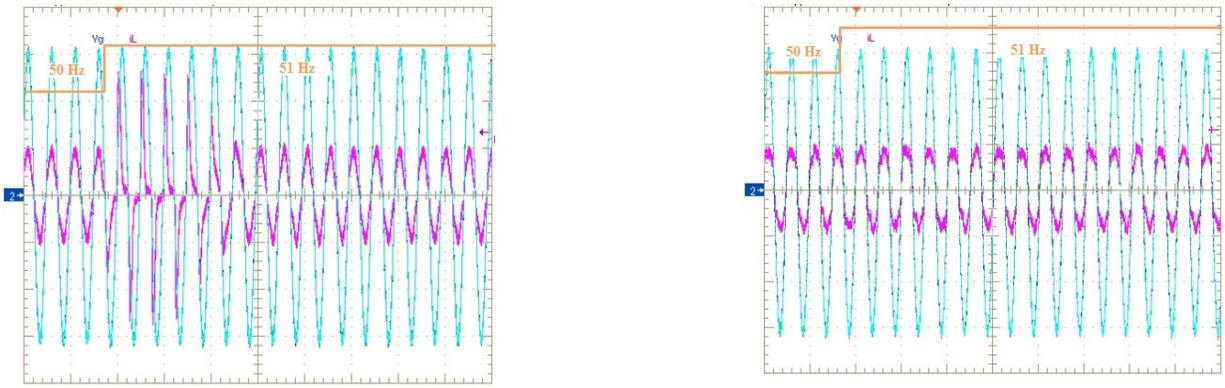
PLLs have been implemented in a FPGA to study their computational burden. In Table III, a summary of the resources used in the FPGA is presented for the different PLLs analyzed, comparing them with the simplest solution, the conventional T/4 PLL.

The behavior of the PLLs is also evaluated experimentally. The test bench consists of a bridgeless PFC with all active switches controlled by a FPGA, in which a linear current controller without current sensor is implemented. The synchronization signal is used to generate the current reference and to correct the estimated input current at the zero crossing points, compensating the accumulated estimation

TABLE III. Summary of the FPGA resources used by different PLLs analyzed

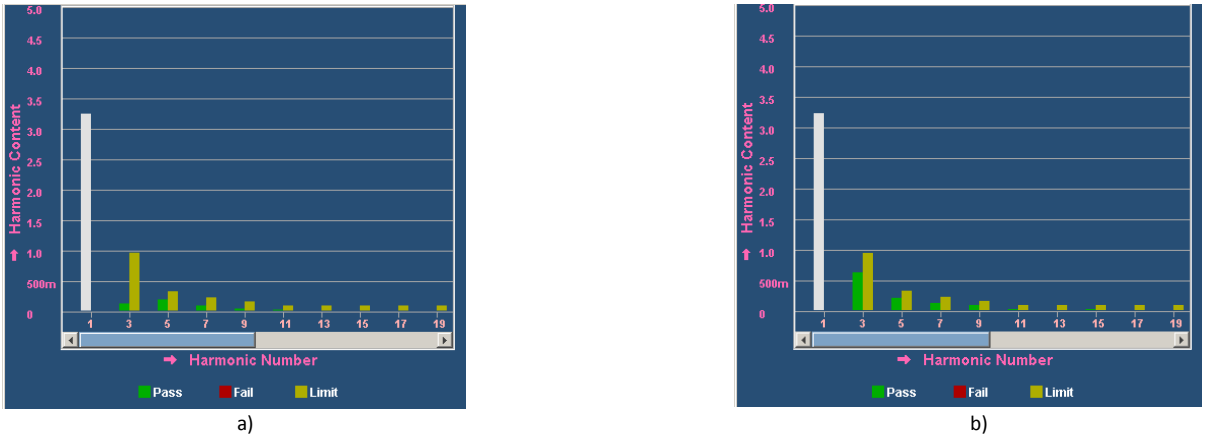
		T/4	T/4 FFB		Backward		Backward FFB		2S		2S FFB	
Slice Logic Utilization	**Available**	**Tot.**	**Tot.**	**%**	**Tot.**	**%**	**Tot.**	**%**	**Tot.**	**%**	**Tot.**	**%**
Slice Registers	126,800	2,776	2,705	97.4	2.654	95.6	2.618	94.3	2,668	96.1	2,690	96.9
LUTs	63,400	6,077	6,136	101.0	6.422	105.7	6.346	104.4	6,574	108.2	6,683	110.0
Occupied Slices	15,850	1,844	2,082	112.9	2.187	118.6	6.954	377.1	2,137	115.9	2,324	126.0
LUT Flip Flop pairs used	--	6,374	6,671	104.7	6.988	109.6	4.435	69.6	7,032	110.3	7,190	112.8
Bonded IOBs	210	20	20	100.0	20	100.0	20	100.0	20	100.0	20	100.0
RAMB36E1 /FIFO36E1s	135	0	0	-	1	-	1	-	0	-	0	-
RAMB18E1 /FIFO18E1s	270	1	2	200.0	1	100.0	1	100.0	1	100.0	1	100.0
DSP48E1s	240	11	13	118.2	11	100.0	13	118.2	10	90.9	12	109.1

The percent values of the resources used are compared with those obtained with the T/4 PLL.



a) b)

Fig. 11. Grid voltage and current waveforms using a) 2SC and b) 2SC FFB PLL under +1 Hz frequency step. Grid voltage V_g, blue, 115 V_{RMS}, 50 Hz, 50 V/div. Grid current: i_g, magenta, 5A/div. Time scale 50 ms/div.



a) b)

Fig. 12. Harmonic content of the line current shown in Fig. 11 compared with the limits set by the standard IEC 61000-3-2 Class C. a) 2SC and b) 2SC FFB PLL

errors each half-period of grid voltage.

The laboratory setup consists of a power stage built with a Vincotech Power MOSFET Module; a sensing Board to measure the DC-link and the grid voltages to estimate the line current; a Nexys 4 board from Digilent (based on Artix 7, XC7A100T-1CSG324C) to implement the digital control; and, Power MOSFET drivers based on Scale cores (2SC0650P).

The parameters used in the setup are shown in Table IV.

The laboratory prototype is supplied by a programmable AC source from Pacific (AC Power Source 345-AMX), which allows the test conditions to be dynamically adjusted.

TABLE IV. SETUP PARAMETERS

PARAMETER	VALUE
Nominal frequency	50 Hz
Grid voltage	115 V_{RMS}
Inductance	1.1 mH
DC-Link capacitance	560 µF
DC-Link voltage	250 V
SW Frequency	98 kHz

The performance of the most representative PLLs is analyzed under a frequency step from 49.5 to 50.5 Hz in Fig. 11. The frequency step is shorter than in the simulation section to reduce the effect of the non-compensated current estimation errors. The obtained results show that the 2SC FFB PLL is faster without overshoot under frequency steps. The 2SC PLL give an overshoot under the dynamic performance and its settling time is 0.11s. In Fig. 12, the harmonic content of the mains current obtained with the 2SC and 2SC FFB, which shows that complies with the standard IEC 61000-3-2 Class C. None of them exceeded the limits but the 2SC FFB obtained higher values in 3th harmonic.

V. CONCLUSION

Bridgeless PFC circuits require a noise tolerant synchronization system, especially if the current sensor is avoided. PLLs are an effective component to this type of situations, but the distortion and variations of the grid frequency can deteriorate their behavior. A novel two-sample PLL with feedback secondary path, applicable to single-phase sensorless Bridgeless PFC states has been proposed. The comparative analysis of similar PLLs show that the feedback loop path is an effective addition to improve the dynamic response under frequency variations, while some more current distortion is observed, implying little extra computational burden and therefore digital circuit resources.

ACKNOWLEDGMENT

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